PC95 Enhanced Super I/O with IrDA Transmission

Features

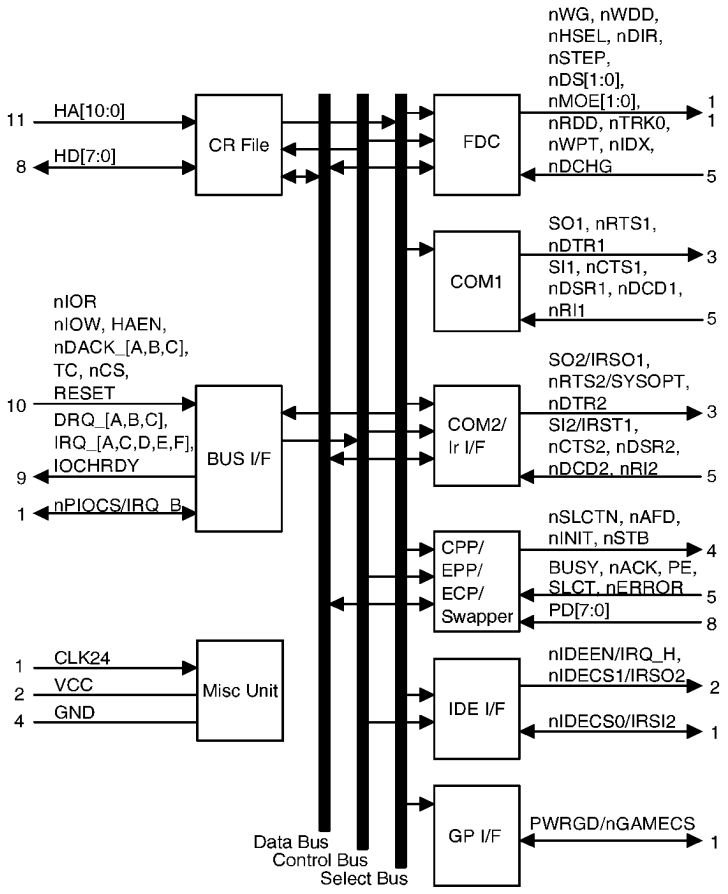
- On board Enhanced Super I/O Controller
- Provide Configurable area for each device on
  - Address mapping
  - IRQ channel routing
  - DMA channel routing
- Support the floppy disk upto 2.88MB
- FDD re-route to Parallel port
- Support 3-mode FDD
- Two high speed serial ports with the IrDA and ASKIr Supporting
- MIDI bit rate supporting on serial port
- Multi-mode parallel port supporting on ECP/EPP/SPP
- IDE/Game port interface decoder output
- Power Management supporting
- 100 PQFP

General Description

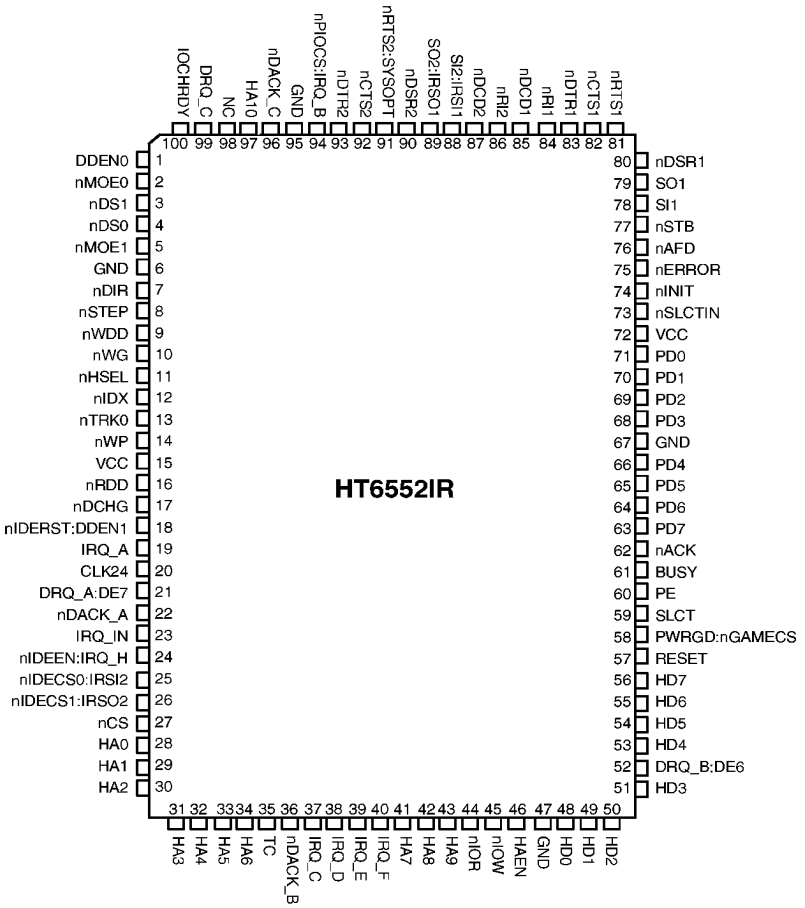
HT6552IR is a high integrated I/O device. It supports a floppy disk controller, a multi-mode printer port, two high speed serial communcation ports, one of which is enriched to support IrDA SIR and ASKIR transmission. By setting the different conf iguration, HT6552IR can also support IDE and game port interfaces.

There are some configuration register sets to reconfigure the ISA address, IRQ access channel, and DRQ channel for each device in order to support PC95 compatible function. The floppy disk controller supports the disk capacity upto 2.88MB with 3-mode floppy disk hardware interface. The disk interface can be re-routed to printer port for some specific applications. In the print port interface, it supports standard mode, PC/AT or PS/2 mode, Enhanced Parallel Port (EPP) 1.7/1.9, or Enhanced Capabilities Port (ECP). For the serial communication interface, there are two high speed ports for serial communication with the MIDI rate supports. One of which is expanded to support IrDA SIR or ASKIR transmission. By using the infrared interface, this device can support wireless communication easily.

Block Diagram



Pin Assignment



Pin Description

Host Interface

Pin No.	Pin Name	Type	Description
97,[43:41], [34:28]	HA[10:0]	I	Host I/O Address: For internal decoder use. The contents are latched internally by the leading edge of nIOR or nIOW.
[56:53], [51:48]	HD[7:0]	I/O24	Host I/O Data: For data accesses. These pins are Hi-Z when no output.
46	HAEN	I	Host Address Enable: For indicating DMA operation and internal address decode qualification.
44	nIOR	I	I/O Read: For host read operation.
45	nIOW	I	I/O Write: For host write operation.
100	IOCHRDY	OD8U	I/O Channel Ready: It is used to extend the host command in EPP mode. It is internal pull-up.
22 36 96	nDACK_A nDACK_B nDACK_C	I I I	DMA Acknowledgement: Host acknowledge the DMA request for transferring.
21 52 99	DRQ_A/ DRQ_B/ DRQ_C	O24ID O24ID O24	DMA Request: This pin is used to request host a DMA transferring. It will be cleared on the last data transfer by the nDACK/nIOR being low.
35	TC	I	Terminal Count: It indicates the DMA transfer is complete.
23	IRQ_IN	I	IRQ Input: An external IRQ input to the chip for IRQ router.
19 94 37 38 39 40 24	IRQ_A IRQ_B IRQ_C IRQ_D IRQ_E IRQ_F IRQ_H	O24 O24 O24 O24 O24 O24 O24	Interrupt Requests: The IRQ router outputs. Internal subsystems and IRQ_IN are connected to the router for re-configurable IRQ channels. When EPP or ECP mode is enable, the related IRQ output issues a low pulse for interrupt request.
27	nCS	I	Chip Select: External decoder input for selecting this device.
57	RESET	IS	System Reset: It is a reset input with a 500ns minimum active pulse for internal egisters reset. The configuration registers are unaffected.

FDD

Pin No.	Pin Name	Type	Description
16	nRDD	IS	Read Disk Data: Raw serial disk data coming from disk presents a flux transition on each falling edge.
9	nWDD	OD48	Write Disk Data: Encoded disk data stream for disk write.
10	nWG	OD48	Write Gate: For disk write head operation.
17	nDCHG	IS	Disk Changed: Indicate drive door is open.
14	nWP	IS	Write Protect: For disk status indication on write protection.
13	nTRK0	IS	Track 00: For disk status indication on track 0 being sensed.
12	nIDX	IS	Index Hole: For disk status indication on index hole being sensed.
11	nHSEL	OD48	Head Select: For disk head selection. A logic "1" means side 0 and a logic "0" means side 1.
7	nDIR	OD48	Direction Control: For disk head direction control. A logic "1" means inward motion and a logic "0" means outward motion.
8	nSTEP	OD48	Step Pulse: A pulse sequence output for track-to-track operation.
3,4	nDS[1:0]	OD48	Drive Selects: For disk driver selection.
5,2	nMOE[1:0]	OD48	Motor On: For disk motor control.
18 1	DDEN1 DDEN0	OD48 OD48	Driver Density(Reduce Write Current): Select drive and media. Refer to CR03, CR0B, and CR1F.

Serial port

Pin No.	Pin Name	Type	Description
78 88	SI1 SI2	I	Serial Data In: Received serial data input.
79 89	SO1 SO2	O4	Serial Data Out: Transmit serial data output.
81 91	nRTS1 nRTS2	O4 OT4	Request To Send: Handshake output signals notify modem that the UARTn is ready to transmit data. It can be programmed by writing to rts.CMn_MCR. It will be reset to inactive mode during hardware reset or forced to inactive during loop mode operation.
83 93	nDTR1 nDTR2	O4	Data Terminal Ready: Handshake output signals no tify modem that the UARTn is ready to setup data communication link. It can be programmed by writing to dtr.CMn_MCR. It will be reset to inactive mode during hardware reset or forced to inactive during loop mode operation.
82 92	nCTS1 nCTS2	I	Clear To Send: Han dshake input signals notify UARTn that the modem is ready to receive data. An nCTSn signal state change from low to high after the last CMn_MSR read will set dcts.CMn_MSR to "1". If emsi.CMn_IER is set, it will generate an interrupt when nCTSn changes sta te. The CPU can monitor the status of nCTSn by reading cts. CMn_MSR. The bit is the complement of nCTSn.
80 90	nDSR1 nDSR2	I	Data Send Ready: Handshake input signals notify UARTn that the modem is ready to setup the data communication link. An nDSRn signal stat change from low to high after the last CMn_MSR read will set ddsr. CMn_MSR to "1". If emsi.CMn_IER is set, it will generate an interrupt when nDSRn changes state. The CPU can monitor the status of nDSRn by reading dsr.CMn_MSR. The bit is the complement onDSRn.
85 87	nDCD1 nDCD2	I	Data Carrier Detect: Handshake input signals notify UARTn that carrier signal is detected by the modem. An nDCDn signal state change from low to high after the last CMn_MSR read will set ddcd.CMn_MSR to "1". If emsi.CMn_IER is set, i t will generate an interrupt when nDCDn changes state. The CPU can monitor the status of nDCDn by reading dcd.CMn_MSR. The bit is the complement of nDCDn.
84 86	nRI1 nRI2	I	Ring Indicator: Handshake input signals notify UARTn that the telephone ring signal is d etected by the modem. An nRIn signal state change from low to high after the last CMn_MSR read will set teri.CMn_MSR to "1". If emsi.CMn_IER is set, it will generate an interrupt when nRIn changes state. The CPU can monitor the status of nRIn by reading r i.CMn_MSR. The bit is the complement of nRIn.

Parallel port

Pin No.	Pin Name	Type	Description
[63:66], [68:71]	PD[7:0]	I/O24	Parallel Port Data I/O: The bi-directional parallel port data for data transfer between HOST and peripherals. It contents either address or data in EPP or ECP mode, the data may i nclude RLE data in ECP mode.
61	BUSY	I	Line Busy: A busy signal from printer to indicate printer is not available to receive the new data. The bit nbusy. SPP_SPR is the complement of this input. nWAIT(Wait): In EPP mode, it is active low to indicate the device is ready for the next transfer. BUSY/nPACK(Line Busy/Peripheral Acknowledge): In ECP mode, it is inactive low to indicate the peripheral is ready for the next transfer in the forward direction. It indicates the the data line is ECP command or data in the reverse direction.
62	nACK	I	Acknowledgment: A acknowledge signal from printer to indicate printer has received data and is ready to accept a new data. The bit nack. SPP_SPR directly reflects this signal. INTR(Interrupt): In EPP mode, it is active high with the positive edge triggered for the interrupt signal. nPACK(Peripheral Acknowledgment): In ECP mode, it is active low to indicate valid data being driven by peripheral.
60	PE	I	Paper End: A status signal from printer to indicate the printer is out of paper. The bit pe.SPP_SPR directly reflects this signal. (Same definition as SPP in EPP mode) PERROR/nACKR(PError/nAckReverse): In ECP mode, peripheral uses it to acknowledge a transfer direction change for nRREQ. The direction is forward when asserted, host is then permitted to drive the bus.
59	SLCT	I	Printer Selected Status: A status signal from p inter to indicate the printer has powered on. The bit slct. SPP_SPR directly reflects this signal. (Same definition as SPP in EPP mode) SLCT(Printer Selected Status): In ECP mode, A status signal from printer to indicate it is on-line.
75	nERROR	I	Printer Port Error: A status signal from printer to indicate an error status at the printer. The bit nerr.SPP_SPR directly reflects this signal. (Same definition as SPP in EPP mode) nFAULT/nPREQ(Fault/Peripheral Request): In ECP mode, peripheral uses it to indicate an error interrupt. It is valid only in forward mode. Occasionally, it can be used as a request for reverse transfer.

Pin No.	Pin Name	Type	Description
73	nSLCTIN	OD24 O24	Printer Select Input: This output is the complement of the bit slctin. SPP_CPR to select the printer. nASTB(Address Strobe): This output is used to indicate an address port access in EPP mode.nSLCTIN(Printer Select Input): In ECP mode, it is always deasserted.
74	nINIT	OD24 O24	Printer Initial Output: This output reflects the bit ninit.SPP_CPR to initiate the printer. (Same definition as SPP in EPP mode) nINIT/nRREQ(Initial Output/Reverse Request): In ECP mode, it sets the transfer direct ion. The transfer direction is reversed when it is asserted.
76	nAFD	OD24 O24	Printer Autofeed Output: This output is the complement of the bit autofd.SPP_CPR to control the printer for the auto line feed after each line is printed. nDSTB(Data Strobe): This output is used to indicate a data port access in EPP mode. nAFD/HACK(Autofeed Output/Host Acknowledge): In ECP mode, it is asserted to request a byte from the peripheral by the handshaking with nPACK in the reverse direction. In the forward direction, it indicates the data contents is address or data.
77	nSTB	OD24 O24	Printer Strobe Output: This output is the complement of the bit stb.SPP_CPR to strobe the data into printer. nWRITE(Write): In EPP mode, this output is used to indicate a write operation. nSTB(Strobe Output): In ECP mode, it is used to strobe the address or data into the peripheral on the asserting edge during write operation.

Infra-red interface

Pin No.	Pin Name	Type	Description
88	IRSI1	I	IR Receive Data In 1: IR Receive data input.
89	IRSO1	O4	IR Transmit Data Out 1: IR Transmit data output.
25	IRSI2	I	IR Receive Data In 2: An alternative IR Receive data input.
26	IRSO2	O24	IR Transmit Data Out 2: An alternative IR Transmit data output.

Game port interface

Pin No.	Pin Name	Type	Description
58	nGAMECS	O4	Game Port Select: This is a select signal for game port I/O address corresponding to the setup of CR1E when game port is enabled.

IDE interface

Pin No.	Pin Name	Type	Description
18	nIDERST	OD48	IDE Reset Output: An inverted RESET output for IDE interface.
24	nIDEEN	O24	IDE Enable: This signal is active when the IDE port is enabled and the system is accessing an IDE register.
25	nIDECS0	O24	IDE Chip Select 0: This is a select signal for IDE base address corresponding to the setup of CR21 when IDE port is enabled.
26	nIDECS1	O24P	IDE Chip Select 1: This is a select signal for IDE alternate base address corresponding to the setup of CR22 when IDE port is enabled.

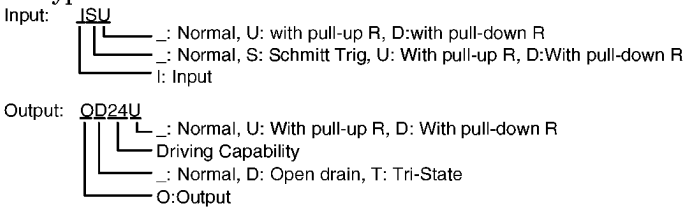
Misc

Pin No.	Pin Name	Type	Description
58	PWRGD	I	Power Good: This signal indicates the power (Vcc) is valid. When it is inactive, all inputs are disconnected, all outputs are tri-stated, and the contents of registers are kept if the Vcc is valid. It sets system into standby mode.
20	CLK24	ICLK	Clock 24MHz: A clock input for whole chip.
94	nPIOCS	OD24U	Programmable I/O Address Decode: This is a select signal for a 1, 8, or 16 byte I/O address corresponding to the setup of CR08 and CR09 when p94s[1:0].CR03 is set to decode mode.
52	DE6	ID	DE6: HT6552 supports an internal pull down input for ISA mode power on setup. System can use an external pull-up resistor to determine the operation mode. At the rising edge of PWRGD, the DE6 input is latched for the mode selection: 0: Normal mode, On-board with no device being active after hardware reset. 1: ISA mode, Adapter based design with default active value after hardware reset.
21	DE7	ID	DE7: HT6552 supports an internal pull down input for Ir mode power on setup. System can use an external pull-up resistor to determine the operation mode. At the rising edge of PWRGD, the DE7 input is latched for the mode selection: 0: Normal mode, polarity of IR receive signal is normal. 1: Inverted mode, polarity of IR receive signal is inverted.
91	SYSOPT	I	Index Base I/O Address Selection: HT6552 supports an input for configuration access setup. System can use an external pull-up/down resistor to determine the address. At the trailing edge of hardware reset, the SYSOPT input is latched for the address selection: 0: Index base I/O address is 3F0h. 1: Index base I/O address is 370h.

Power

Pin No.	Pin Name	Type	Description
15,72	VCC	Power	Vcc Power:
6,47,67,95	GND	Power	Ground:

Note: Pin type definition:



Register Definition

FDC register set

There are status registers, data register, and control registers being built in the FDC subsystem. The address map and the short form of these registers are shown below:

Base I/O Address	Attribute	Abbreviation	Description
fdc+00h			Reserved
fdc+01h			Reserved
fdc+02h	W/R	FDC_DOR	Digital output register
fdc+03h			Reserved
fdc+04h	W R	FDC_DSR FDC_MSR	Data rate select register Main status register
fdc+05h	W/R	FDC_MDR	Main data register
fdc+06h			Reserved
fdc+07h	W R	FDC_CCR FDC_DIR	Configuration control register Digital input register

Default	Reg	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
00	DOR	0	0	moten[1:0]		dmaen	nreset	dvsel[1:0]	
02	DSR	sreset	fdchpd	0	pcomp[2:0]			drsel[1:0]	
—	MSR	rqm	dio	nondma	cmdbsy	dubsy[3:0]			
—	MDR	hd[7:0]							
10b	CCR	—	—	—	—	—	—	drsel[1:0]	
–	DIR	dskchg	—	—	—	—	—	—	—