

MSAN-210 MVTX260x Port Mirroring

Application Note

October 2002

Contents

1.0 Purpose

2.0 Scope

3.0 Features

3.1 Unmanaged mode

3.2 Managed Mode

4.0 Flexible Port Mirroring Support

1.0 Purpose

This application note describes the port mirroring usage on the MVTX260x chipsets.

2.0 Scope

This document will cover Port Mirroring for the MVTX260x device. The reader should be familiar with the MVTX260x data sheet before reading this application note

3.0 Features

This application note describes the port mirroring usage on the MVTX260x chipsets. The MVTX260x chips provide port-mirroring function on the 10/100M ports. The traffic can be mirrored from either receive or transmit stream except on ports 7 (8th), 15 (16th), and 23 (24th). Ports 7, 15, and 23 take advantage of the Zarlink security mirroring feature which allows the mirrored data to be viewed by the CPU through the software steps outlined in this application note. For the unmanaged switches, port 23 is the designated mirror-to port. The MVTX260x supports two such mirrored source-destination pairs. A mirror port cannot also serve as a data port.

3.1 Unmanaged mode

The port mirroring functionality may be set by external pins on the MVTX260x. If this option is selected, then there can only be one mirroring pair, and the destination port must be port 23. There are 6 pins (PM_CT[5:0]). The first 5 bits select the port to be mirrored. The last bit selects either ingress or egress data. Again the unmanaged mode port mirroring function does not apply to port 7 and 15. The port mirroring control via external pins can be applied to the managed mode as well.

Issue 1

3.2 Managed Mode

In management mode, the port mirroring is set via four registers:

- MIRROR1_SRC: Sets the source port for the first port mirroring pair. Bits [4:0] select the source port to be mirrored. An illegal port number is used to disable mirroring (which is the default setting). Bit [5] is used to select between ingress (Rx) or egress (Tx) data. Bit [7] is used to select between external pin controls and register control for port mirroring.
- MIRROR1_DEST: Sets the destination port for the first port mirroring pair. Bits [4:0] select the destination port to be mirrored. The default is port 23.
- MIRROR2_SRC: Sets the source port for the second port mirroring pair. Bits [4:0] select the source port to be mirrored. An illegal port number is used to disable mirroring (which is the default setting). Bit [5] is used to select between ingress (Rx) or egress (Tx) data.
- MIRROR2_DEST: Sets the destination port for the second port mirroring pair. Bits [4:0] select the destination port to be mirrored. The default is port 0.

Zarlink products and associated documents marked "Eng" ("ENGineering Samples") are or relate to products in development and not released to production. All ENGineering Samples are supplied only for testing and on the express understanding that (i) they have not been fully tested or characterized under intended modes of operation and may contain defects; (ii) Zarlink makes no representation or warranty regarding them; and (iii) Zarlink disclaims any liability for claims, demands and damages, including without limitation special, indirect and consequential damages, resulting from any loss arising out of the application, use or performance of them. ENGineering Samples may be changed or discontinued by Zarlink at any time without notice.

4.0 Flexible Port Mirroring Support

This section describes a flexible software solution to selectively mirror the incoming or outgoing traffics of a given MAC. If all MACs for the ingress and egress packets of a port are mirrored, then the function is similar to port mirroring. The main approach is to utilize the secure mode hardware, which forwards the monitored traffics of a given port to the CPU only. The driver then sets up the MAC entries that point the return traffics to the CPU port, so the traffic can be captured.

In the MVTX260x driver, the port mirroring function for ports 7, 15, and 23 are provided as an option. The software port mirroring implemented in the driver is described below.

First, the following MVTX2604 register needs to be program as follow:

 The ECR2 register for the mirror source port need the Security Enabled field to be set to Send Packet to CPU Only. Also for this register, the Learning Disable field needs to be set to 1. Setting these fields will cause all ingress packets to be forwarded to the CPU.

The driver then needs to be modified to perform the following functions:

- Ingress packets that have an unknown source MAC address needs to be learned by the driver. The driver
 must also send a control frame to the MVTX2604 to have this new source MAC address added to the CPU
 port.
- Forward all ingress packets of the mirror source port to the destination port if the destination MAC address
 has been learned. If the destination MAC address is unknown then flood the packet to the VLAN domain
 ports. Also, forward the ingress packets to the mirror destination port.
- Receive all packets destined for the mirror source port and forward it to the mirror source port.

If mirroring is disabled then the Security Enabled and Learning Disable field in the ECR2 register must be set to its default value and the driver functions to support this solution must not be executed.

Note: This software solution may not provide line rate traffic between the mirror source port and any mirror-to port. The actual line rate depends on the type and speed of the processor.



For more information about all Zarlink products visit our Web Site at

www.zarlink.com

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. trading as Zarlink Semiconductor or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I²C components conveys a licence under the Philips I²C Patent rights to use these components in an I²C System, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Zarlink and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright 2002, Zarlink Semiconductor Inc. All Rights Reserved.

TECHNICAL DOCUMENTATION - NOT FOR RESALE