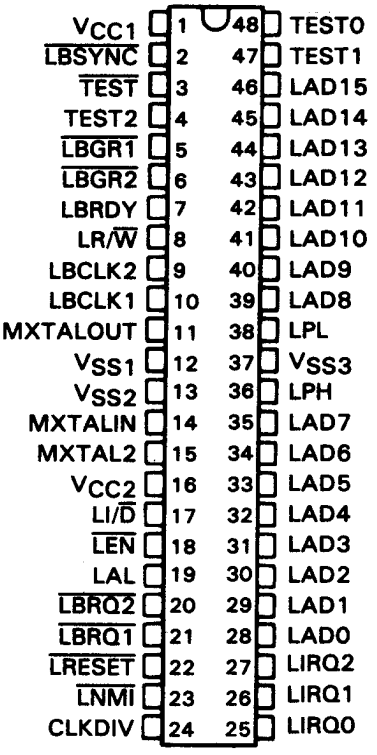
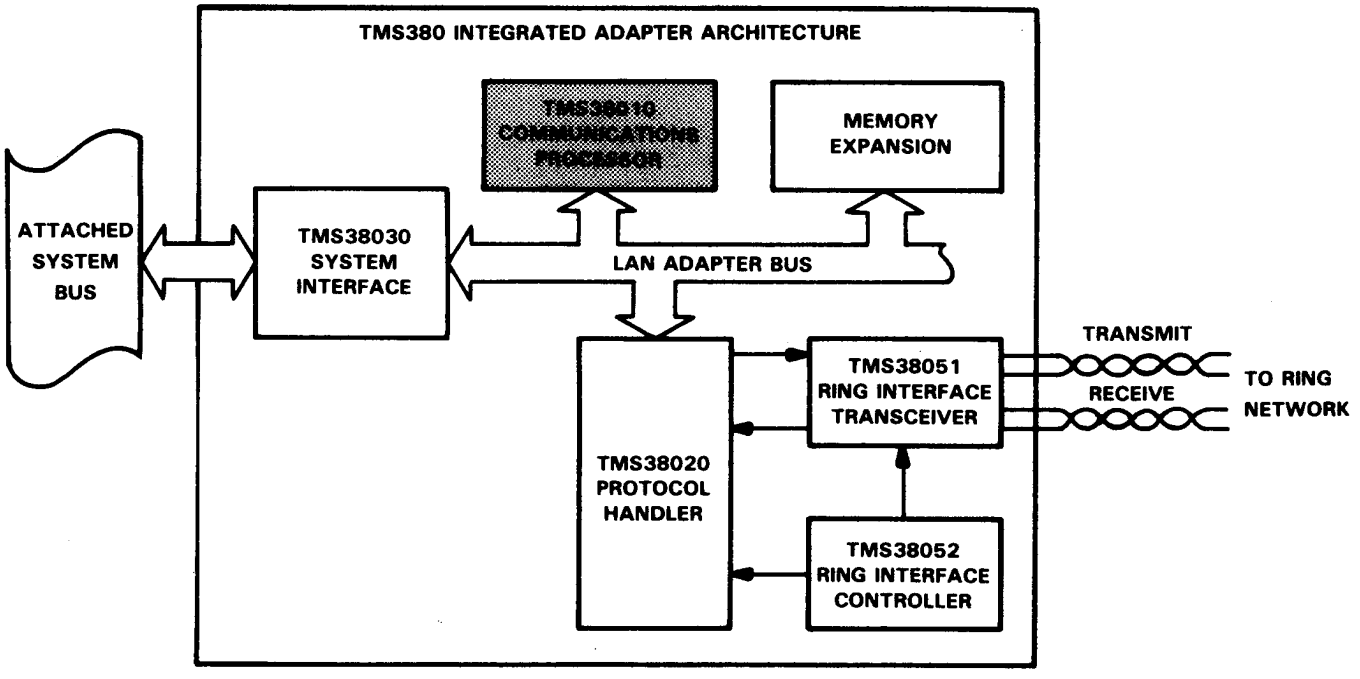
SEPTEMBER 1985 – REVISED MAY 1986

- **High-Performance 16-Bit CPU for Processing Communications Protocols**
  - **–333-ns Machine and Bus Cycle Time**
  - **–Single Cycle Pipelined Bus Arbitration**
  - **–9 Interrupt Priority Levels**
  - **–8-Bit General Purpose Timer**
- **On-Chip 2.75K-Byte RAM for Buffering Network Data**
  - **–1408 x 18-Bit Organization**
  - **–Byte Parity Protection**
  - **–6 Megabyte per Second Data Transfer Rate**
- **Expandable Program and Data Memory Space up to 256K Bytes**
- **Built-in Real Time Error Detection**
- **Test Pins for Hi-Z, Module-in-Place Testing**
- **Single 5-V Supply**
- **24-MHz Crystal Oscillator or Crystal Input (Internal Oscillator Option)**
- **Low-Power Scaled-NMOS Technology**

JD PACKAGE
(TOP VIEW)



token ring LAN application diagram



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pin descriptions

NAME	I/O	DESCRIPTION
$\overline{\text{LRESET}}$	I	TMS38010 Reset
LBCLK1, LBCLK2	O	Bus Clocks
$\overline{\text{LBSYNC}}$	I	Bus Synchronization. This pin is reserved and should be left unconnected.
LAL	I/O	Address Latch Enable
$\overline{\text{LEN}}$	I/O	Data Enable
LBRDY	I	Bus Ready. Used to force wait states on bus read/write cycles.
LIRQ0, LIRQ1, LIRQ2	I	Interrupt Request Level Request
$\overline{\text{LNMI}}$	I	Non-Maskable Interrupt (NMI) Request
$\overline{\text{LBRQ1}}$, $\overline{\text{LBRQ2}}$	I	Bus Request 1 and 2. Used by bus masters to request control of the bus.
$\overline{\text{LBGRI}}$, $\overline{\text{LBGR2}}$	O	Bus Grant 1 and 2
LAD0 - LAD15	I/O	Address/Data bus. LAD0 is the most-significant bit and LAD15 is the least-significant bit. LAD15 serves as a "Page Select" during the address phase of memory cycles.
LPH, LPL	I/O	Parity High Byte and Low Byte. Parity for data carried over LAD0-LAD15.
LI/$\overline{\text{D}}$	O	Instruction Fetch/Data Transfer Status Code
LR/$\overline{\text{W}}$	I/O	Read/Write signal
CLKDIV	I	This pin is reserved and should be tied to V_{CC}.
MXTALIN	I	Input to internal oscillator from crystal or external clock
MXTAL2	O	Connection to internal oscillator from crystal
MXTALOUT	O	Crystal Frequency Output. This frequency is MXTALIN/3.
$\overline{\text{TEST}}$, TEST0-TEST2	I	TMS38010 Test Pins. These pins should be left unconnected.
V_{CC}	I	5-V supply pins
V_{SS}	I	Ground pins

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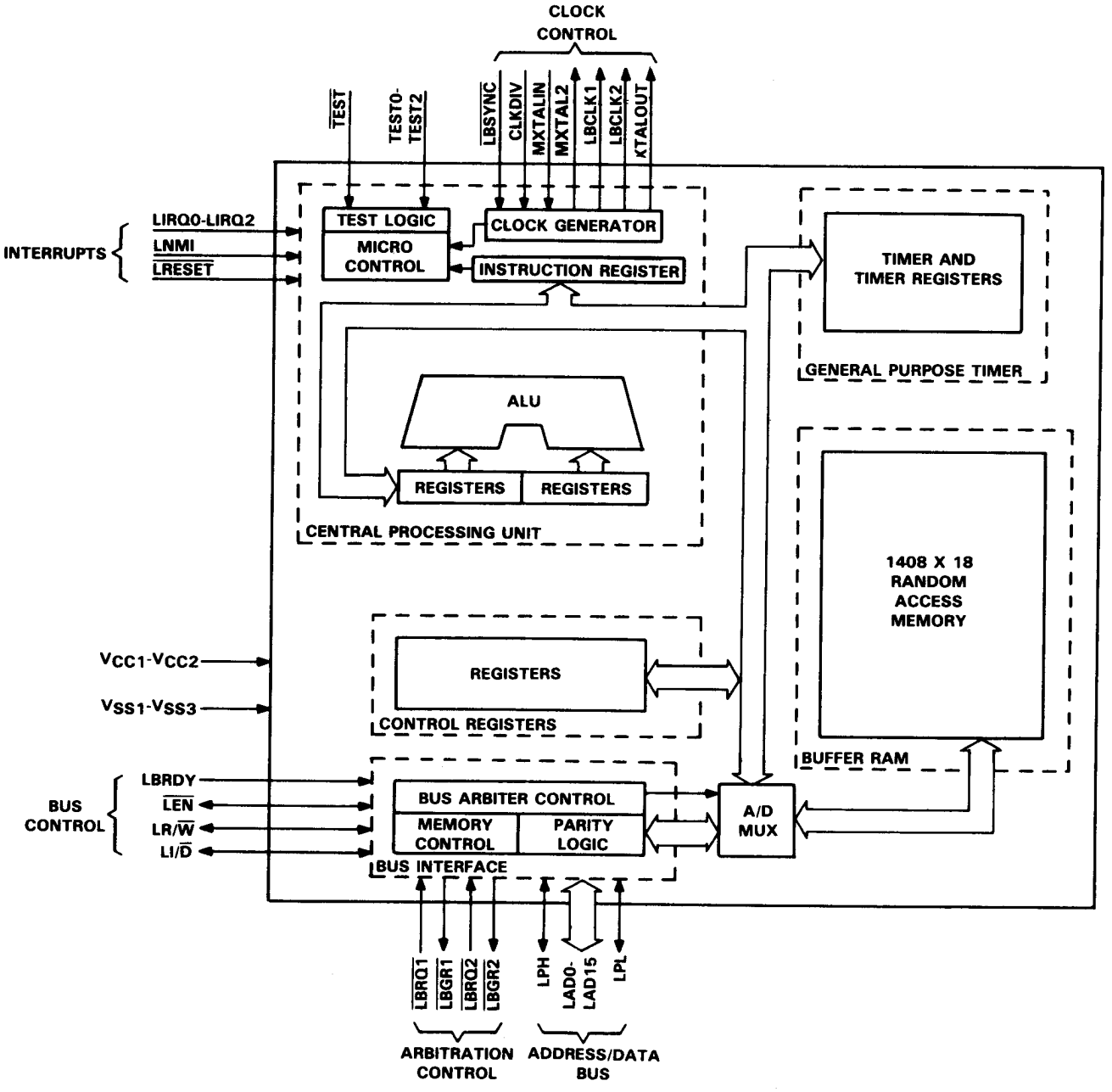
functional block diagram



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description

The TMS38010 Communications Processor is a member of the TMS380 family of VLSI components which form a highly integrated Adapter used for attaching to a token ring local area network (LAN). The TMS38010 provides a high-performance CPU ideal for processing communications protocols. The TMS38010 provides 63 instructions, a 1408 x 18-bit RAM for communications data buffering and CPU workspace, and a general purpose timer for implementing software protocol timers. The TMS38010's architecture features hardware and software interrupts, memory-based registers for fast response to hardware and software interrupts, and a 333-ns machine cycle time. Bus arbitration is provided internal to the TMS38010 Communications Processor.

The TMS38010 Communications Processor, when coupled with the TMS38020 Protocol Handler, the TMS38030 System Interface, and the TMS38051 and TMS38052 Ring Interface Pair, forms a complete, integrated token ring LAN Adapter fully compatible with the IEEE Std 802.5-1985 Token Ring Access Method and Physical Layer Specifications for token ring networks.

architecture

The architecture of the TMS38010 Communications Processor consists of a 16-bit CPU, a LAN Adapter bus interface, a general purpose timer, control registers, and a 2.75K-byte buffer RAM.

central processing unit

The central processing unit (CPU) of the TMS38010 contains the arithmetic-logic unit (ALU), registers, and control store. This CPU features memory-to-memory architecture which can address up to 256K bytes of memory, logically divided into 128K bytes of data memory and 128K bytes of instruction memory. Using paging techniques, both the instruction and data spaces are paged into two 64K byte regions. This paging is accomplished via a page select output on the LAD15 pin during the address phase of memory cycles. The state of this pin is controlled through the CPU's status register.

arithmetic-logic unit (ALU)

The arithmetic-logic unit of the TMS38010 is 16 bits wide. The ALU performs all arithmetic and logical operations required during instruction execution. The ALU is partitioned into two 8-bit halves to accommodate byte operations. The bus interface only performs 16-bit wide transfers on the LAN Adapter bus, thus, the byte being operated upon may be modified while the unaffected byte is passed through unchanged.

internal registers

The CPU contains three registers used for programming: the Program Counter (PC), the Status Register (ST), and the Workspace Pointer (WP). The Program Counter contains the memory address of the next instruction word. The Status Register contains bits which signify the results of program comparisons, indicate program status conditions, and supply the interrupt mask to the interrupt priority circuits. The Workspace Pointer contains a memory address which defines the first word of a block of 16 words which define the Workspace Registers. These workspace registers are memory-resident working registers and are used as scratch and index registers similar to the internal registers of register-based architectures. By changing the value of the Workspace Pointer (as may occur when an interrupt occurs), a new set of registers is defined for efficient program context switches.

interrupts

Interrupts are presented to the TMS38010 via the LIRQ0, LIRQ1, and LIRQ2 interrupt request pins. These pins, when any one is active low for an entire LBCLK cycle, cause an interrupt request to be posted to the TMS38010's CPU. LIRQ0 (the most-significant bit) through LIRQ2 (the least-significant bit) present an interrupt level of one (all low) through level seven. When LIRQ0 through LIRQ2 are all high, no interrupt is requested. The prioritization of interrupts is done external to the TMS38010. In the TMS380 LAN Adapter, this function is performed by the TMS38030 System Interface.

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When an interrupt is accepted (by one or more of the LIRQ lines being low for a full LBCLK cycle), the CPU performs a context switch by fetching a new Program Counter value and a new Workspace Pointer value from predefined memory locations in the first 32 bytes of memory. Three interrupt levels are specially defined for the TMS38010. The first is interrupt level 10. This interrupt level is used by the TMS38010's internal general purpose timer when the count has decremented to zero. The level ten interrupt is also used for a special "software interrupt" initiated by a request bit in the CPCTL (CP Control) register. This bit allows higher level software routines to activate lower-level routines such as a task scheduler. The second interrupt level specially defined for the TMS38010 is the level-2 interrupt. The level-2 interrupt is used to report several error conditions of the TMS38010. These include arithmetic fault, illegal opcode, and LAN Adapter bus parity errors. The third interrupt level defined for the TMS38010 is the level-0 interrupt. This interrupt is asserted when the $\overline{\text{LRESET}}$ or the $\overline{\text{LNMI}}$ pin is taken active low.

LAN adapter bus interface

The TMS38010 provides a high-speed interface to the TMS380 family LAN Adapter bus. This bus interface allows the TMS38010's CPU to communicate to external memory and peripherals and allows external LAN Adapter Bus masters unrestricted access to the internal Buffer RAM of the TMS38010. A full description of the bus cycles and their timing may be found in the electrical specifications.

The LAN Adapter bus is a multiplexed bus with address and data multiplexed on the LAD0-LAD15 pins. All transfers on the LAN Adapter bus consist of 16-bit words. Parity is checked and generated on each data byte transfer on the LAN Adapter bus. Detection of a parity error by the TMS38010 causes a level-2 interrupt to occur.

Each cycle on the LAN Adapter bus extends for at least one LBCLK1/LBCLK2 period (333 ns). External devices may extend the bus transfer in increments of one LBCLK1/LBCLK2 period (wait states) by driving LBRDY low before the falling edge of LBCLK2. The bus transfer extends until the bus master samples LBRDY high at the falling edge of LBCLK2. When accessing the internal buffer RAM, neither the CPU nor external bus masters incur wait states.

The LI/$\overline{\text{D}}$ pin is driven high or low at the beginning of each memory cycle to indicate whether data is being accessed or an instruction is being fetched. This information may be used to partition the memory map of the TMS38010 into a data space and an instruction space. Also, LAD15 will display the inverted value of status bit 8 of the Status Register during the address phase of the cycle which may be used to "page" the memory for extended memory applications. Note, however, that the TMS38010 does not decode either the LI/$\overline{\text{D}}$ pin nor the LAD15 (page select) for accesses to internal buffer RAM or registers.

general purpose timer

The TMS38010 contains a general purpose timer which can be programmed to provide an interrupt to the TMS38010 CPU at regular intervals. This timer is intended as the hardware base for all protocol timers implemented in software.

The general purpose timer is controlled by the CPU through two registers: the GPTLATCH register and the GPTDATA register. The GPTLATCH register is an 8-bit register loaded by the CPU as the initial timer value. It is read and written by the CPU as the most-significant byte of the word at address >0096 (">" designates a hexadecimal number). A second register, GPTDATA, is an 8-bit decrementer that the CPU may read as the most-significant byte of the word at address >0098. GPTDATA is loaded with the contents of GPTLATCH when either the GPTDATA register is decremented to zero or the timer start bit of CPCNTL is toggled from 0 to 1.

The general purpose timer decrements the value in GPTDATA by a signal derived from LBCLK (3 MHz) divided by 512. When GPTDATA decrements to zero, the GPTINT bit of the CPSTS (CP Status) register is set. If the interrupt was enabled by setting the GPTIEN bit of the CPCTL (CP Control) register, a level-10 interrupt will be asserted to the CPU. The decrementer will be reloaded with the value in GPTLATCH on the next LBCLK cycle following the decrement to zero. Hence, the period of timer interrupts is $(512)t_c$(GPTLATCH) where t_c is the machine cycle time (333 ns).

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control registers

In addition to the GPTLATCH and GPTDATA register, the TMS38010 Communications Processor contains two additional 16-bit registers: the CP Control (CPCTL) register and the CP Status (CPSTS) register. These 16-bit registers are used by the CPU as follows: 1) to control the operation of the general purpose timer, 2) to test the parity of the LAN Adapter bus, and 3) to store status information with respect to the CPU. These registers are shown in Figure 1.

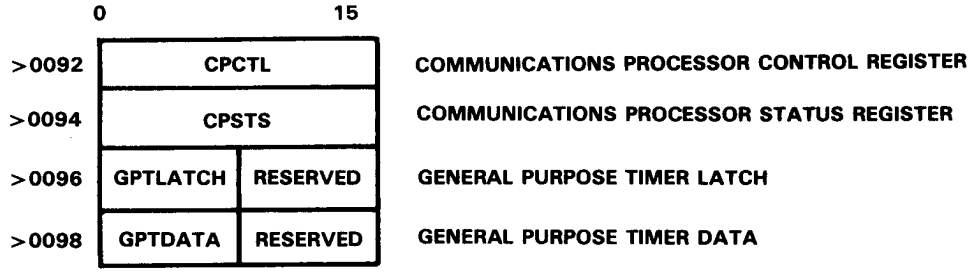

FIGURE 1. TMS38010 CONTROL REGISTERS

CPCTL register

The CPCTL register controls the general purpose timer and the LAN Adapter bus parity checker/generator. Four bits are defined; the remaining bits are reserved. These bits are defined in Table 1.

TABLE 1. CONTROL REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	LPIEN	Local Parity Interrupt Enable
1	LPTST	Local Parity Test
2	GPTIEN	General Purpose Timer Interrupt Enable
3	GPTSTART	General Purpose Timer Start
4	RFLAG	Reset Flag. Cleared upon hardware reset.

CPSTS register

The CPSTS register provides additional status for the CPU, the status of the parity checkers, and the status of the general purpose timer. The bits of the CPSTS register are shown in Table 2.

TABLE 2. CPSTS REGISTER BIT VALUES

BIT	NAME	DESCRIPTION
0	ILLOP	Illegal Operation Interrupt Request
1	AFI	Arithmetic Fault Indicator
2	LPE	Local Parity Error
3	GPTINT	General Purpose Timer Interrupt
4	SWINT	Software Interrupt Indicator
5-11		Reserved
12	TEST0	Test 0 pin value
13	TEST1	Test 1 pin value
14	TEST2	Test 2 pin value
15	CLKDIV	CLKDIV pin value

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buffer RAM

The TMS38010 contains 1408 x 18-bits of random-access memory on chip. The RAM is implemented with a dynamic cell. Refresh is performed transparently to bus operation. The buffer RAM features single cycle access (no wait states) when accessed by either the CPU of the TMS38010 or external bus masters.

The buffer RAM is intended for storage of incoming and outgoing frame data as well as additional CPU software working storage. The RAM occupies addresses >0000 through >007E and >0580 through >0FFE in the memory space of the CPU.

test mode

The TMS38010 reatures a module-in-place test mode for board-level testing with the TMS38010 in circuit. This facilitates testing by bed-of-nails testers. This test mode is enabled by tying pins $\overline{\text{TEST}}$, TESTO, TEST1 and TEST2 to ground and maintaining the clock input on MXTALIN. This has the effect of driving all outputs of the TMS38010 to the high-impendance state except MXTAL2. These pins may also be used to disable the on-chip buffer RAM. Table 3 illustrates the modes selectable through the test pins. All pin state combinations are reserved and should only be configured as shown in Table 3. When not used for these purposes, these pins should be left unconnected. An internal pullup drives these pins high when not externally connected.

TABLE 3. TEST PIN MODES

$\overline{\text{TEST}}$	TEST0	TEST1	TEST2	MODE SELECTED
NC	NC	NC	NC	Normal Operation
LOW	LOW	LOW	LOW	Module-In-Place Test
NC	LOW	NC	NC	On-Chip RAM Disabled

NC denotes no-connect

CPU instruction set summary

DUAL-OPERAND INSTRUCTIONS — GENERAL SOURCE AND DESTINATION		
MNEMONIC	**MEANING**	**DESCRIPTION**
A	Add Words	(SA) + (DA) → (DA)
AB	Add Bytes	(SA) + (DA) → (DA)
C	Compare Words	Compare (SA) to (DA) and set appropriate status bits.
CB	Compare Bytes	Compare (SA) to (DA) and set appropriate status bits.
S	Subtract Word	(DA) − (SA) → (DA)
SB	Subtract Byte	(DA) − (SA) → (DA)
SOC	Set Ones Corresponding	(DA) OR (SA) → (DA)
SOCB	Set Ones Corresponding Byte	(DA) OR (SA) → (DA)
SZC	Set Zeros Corresponding	(DA) AND (SA) → (DA)
SZCB	Set Zeros Corresponding Byte	(DA) AND (SA) → (DA)
MOV	Move Word	(SA) → (DA)
MOVB	Move Byte	(SA) → (DA)

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CPU instruction set summary (continued)

DUAL-OPERAND INSTRUCTIONS – REGISTER DESTINATION		
MNEMONIC	**MEANING**	**DESCRIPTION**
COC	Compare Ones Corresponding	Test (D) to determine if 1's are in each bit position where 1's are in (SA). If so, set appropriate bits in status register.
CZC	Compare Zeros Corresponding	Test (D) to determine if 0's are in each bit position where 1's are in (SA). If so, set appropriate bits in status register.
XOR	Exclusive OR	(D) XOR (SA) → (D)
MPY	Multiply	Multiply unsigned (D) by unsigned (SA) and place unsigned 32-bit product in D (most significant) and D + 1 (least significant).
DIV	Divide	If unsigned (SA) is less than or equal to (D), perform no operation and set status register bit 4. Otherwise, divide unsigned (D) and (D + 1) by unsigned (SA). Quotient → (D), remainder → (D + 1)
SIGNED MULTIPLY AND DIVIDE		
MNEMONIC	**MEANING**	**DESCRIPTION**
MPYS	Signed Multiply	Multiply signed 2's complement integer in register 0 by signed 2's complement integer in (SA) and place signed 32-bit product in register 0 (most significant) and register 1 (least significant).
DIVS	Signed Divide	If the quotient cannot be expressed as a signed 16-bit quantity (hex 8000 is a valid negative number), set the appropriate status register bits, otherwise, divide the signed 2's complement integer in register 0 and register 1 by the signed 2's complement integer at SA and place the signed quotient in register 0 and the signed remainder in register 1. The sign of the quotient is determined by algebraic rules. The sign of the remainder is the same as the sign of the dividend, and |REMAINDER| < |DIV|.
EXTENDED OPERATION		
MNEMONIC	**MEANING**	**DESCRIPTION**
XOP	Extended Operation	Performs a context switch. The address of the trap vector is calculated by (>0040 + 4 × D).
SINGLE-OPERAND INSTRUCTIONS		
MNEMONIC	**MEANING**	**DESCRIPTION**
B	Branch	SA → (PC)
BL	Branch and Link	(PC) → (WR11), SA → (PC)
BLWP	Branch and Load Workspace Pointer	(SA) → (WP), (SA + 2) → (PC), (old WP) → (new WR13), (old PC) → (new WR14), (old ST) → (new WR15). The LIRQ inputs are not tested upon completion of the BLWP instruction.
CLR	Clear	0 → (SA)
SETO	Set to Ones	FFFF → (SA)
INV	Invert	(SA) inverted → (SA)
NEG	Negate	− (SA) → (SA)
ABS	Absolute Value	|(SA)| → (SA)
SWPB	Swap bytes	Bits 0-7 of (SA) → bits 8-15 of (SA); bits 8-15 of (SA) → bits 0-7 of (SA)
INC	Increment	(SA) + 1 → (SA)
INCT	Increment by 2	(SA) + 2 → (SA)
DEC	Decrement	(SA) − 1 → (SA)
DECT	Decrement by 2	(SA) − 2 → (SA)
X	Execute	Execute instruction at SA

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CPU instruction set summary (concluded)

SHIFT INSTRUCTIONS		
MNEMONIC	**MEANING**	**DESCRIPTION**
SLA	Shift Left Arithmetic	Shift (W) left. Fill vacated bit positions with 0.
SRA	Shift Right Arithmetic	Shift (W) right. Fill vacated bit positions with original MSB of (W).
SRC	Shift Right Circular	Shift (W) right. Shift previous LSB into MSB.
SRL	Shift Right Logical	Shift (W) right. Fill vacated bit positions with zeros.
JUMP INSTRUCTIONS		
MNEMONIC	**MEANING**	**DESCRIPTION**
JEQ	Jump Equal	Jump if ST2 = 1.
JGT	Jump Greater Than	Jump if ST1 = 1.
JH	Jump High	Jump if ST0 = 1 and ST2 = 0.
JHE	Jump High or Equal	Jump if ST0 = 1 or ST2 = 1.
JL	Jump Low	Jump if ST0 = 0 and ST2 = 0.
JLE	Jump Low or Equal	Jump if ST0 = 0 or ST2 = 1.
JLT	Jump Less Than	Jump if ST1 = 0 and ST2 = 0.
JMP	Jump	Jump unconditional.
JNC	Jump No Carry	Jump if ST3 = 0.
JNE	Jump Not Equal	Jump if ST2 = 0.
JNO	Jump No Overflow	Jump if ST4 = 0.
JOC	Jump on Carry	Jump if ST3 = 1.
JOP	Jump Odd Parity	Jump if ST5 = 1.
IMMEDIATE REGISTER INSTRUCTIONS		
MNEMONIC	**MEANING**	**DESCRIPTION**
AI	Add Immediate	(W) + IOP → (W)
ANDI	AND Immediate	(W) AND IOP → (W)
CI	Compare Immediate	Compare (W) to IOP and set appropriate status bits.
LI	Load Immediate	IOP → (W)
ORI	OR Immediate	(W) OR IOP → (W)
INTERNAL REGISTER LOAD-IMMEDIATE INSTRUCTIONS		
MNEMONIC	**MEANING**	**DESCRIPTION**
LWPI	Load Workspace Pointer Immediate	IOP → (W), no status bits affected.
LIMI	Load Interrupt Mask Immediate	IOP bits 12 through 15 → ST12 through ST15.
INTERNAL REGISTER LOAD-AND-STORE INSTRUCTIONS		
MNEMONIC	**MEANING**	**DESCRIPTION**
STST	Store Status Register	ST → (W)
LST	Load Status Register	(W) → (ST)
STWP	Store Workspace Pointer	(WP) → (W)
LWP	Load Workspace Pointer	(W) → (WP)
RETURN		
MNEMONIC	**MEANING**	**DESCRIPTION**
RTWP	Return to Workspace Pointer	WR15 → ST, WR14 → PC, WR13 → WP.

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TERMS USED IN INSTRUCTION SUMMARY TABLES

TERM	DEFINITIONS
SA	Source Address
DA	Destination Address
W	Workspace Register
a → b	a is transferred to b
|n|	Absolute value of n
ST	Status Register
STn	Bit n of Status Register
PC	Program Counter
(SA)	Contents of source address
(DA)	Contents of destination address
(W)	Contents of workspace register
WP	Workspace Pointer
IOP	Immediate operand
LSB	Least-significant bit (byte)
MSB	Most-significant bit (byte)
WRn	Workspace Register n

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range . . . . . −0.3 V to 20 V
Output voltage range . . . . . −2 V to 7 V
Operating free-air temperature range (see Note 2) . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES 1. Voltage values are with respect to V_{SS}.
2. Devices are tested in an environment in excess of 70°C to guarantee operation at 70°C. Case temperatures should be maintained at or below 90°C.

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recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	MXTALIN	2.4			V
		CLKDIV, TEST0-TEST2, $\overline{\text{LBSYNC}}$	V_{CC}			V
		All other inputs	2			V
V_{IL}	Low-level input voltage	MXTALIN			0.6	V
		CLKDIV, TEST0-TEST2, $\overline{\text{LBSYNC}}$			V_{SS}	V
		All other inputs			0.8	V
I_{OH}	High-level output current	All outputs			0.15	mA
I_{OL}	Low-level output current	All outputs			−1.7	mA
C_L	Load capacitance	MXTALOUT (Note 3)			80	pF
		All other outputs (Note 4)			100	pF
T_A	Operating free-air temperature (Note 2)		0		70	°C

NOTES: 2. Devices are tested in an environment in excess of 70°C to guarantee operation at 70°C. Case temperatures should be maintained at or below 90°C.
3. High-frequency outputs on a printed-circuit card should be routed to minimize the inductance between the signal and system ground. All V_{SS} pins should also be routed to minimize inductance to system ground.
4. The difference in load capacitances on LBCLK1 and LBCLK2 must not exceed 10 pF.

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	LBCLK1, LBCLK2	V_{CC} = 4.5 V, I_{OH} = 0.15 mA	4			V
		All other outputs		2.4			V
V_{OL}	Low-level output voltage	All outputs	V_{CC} = 5.5 V, I_{OL} = 1.7 mA			0.45	V
I_{OH}	High-level output current	All outputs	V_{CC} = 4.5 V, V_{OH} = 2.4 V			0.15	mA
I_{OL}	Low-level output current	All outputs	V_{CC} = 4.5 V, V_{OL} = 0.45 V			−1.7	mA
I_{OZL}	Off-state (high-impedance state) output current with low-level voltage applied		V_O = 0.45 V			−20	μA
I_{OZH}	Off-state (high-impedance state) output current with high-level voltage applied		V_O = 2.4 V			20	μA

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted) (concluded)

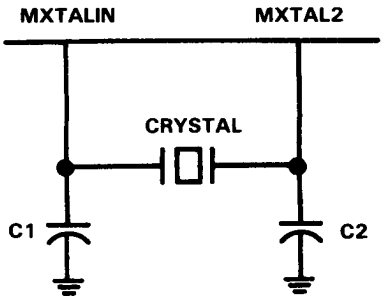
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Low-level input current	$\overline{LEN}$, TEST0-TEST2, $\overline{TEST}$, $\overline{LBSYNC}$ (Notes 5 and 6)	V_I = 0.45 V			−700	μA
		All other inputs				−20	μA
I_{IH}	High-level input current		$V_I = V_{CC}$			20	μA
I_{CC}	Supply Current		V_{CC} = 5 V, T_A = 25° C		150		mA
			V_{CC} = 5.5 V, T_A = 0° C			305	mA
			V_{CC} = 5.5 V, T_C = 90°C			240	mA
C_I	Input capacitance	All inputs	f = 1 MHz, all other inputs at 0 V			15	pF

NOTES: 5. $\overline{LEN}$, TEST0-TEST2, and $\overline{LBSYNC}$ have internal pullups. They may be left unconnected, in which case they function as being high.
6. $\overline{LBSYNC}$ and $\overline{TEST}$ should be left unconnected.

CLOCK REQUIREMENTS AND TIMING

internal clock option

The internal oscillator is enabled by connecting a parallel-resonant crystal across MXTALIN and MXTAL2 (see Figure 2). MXTALOUT is one-third the crystal fundamental frequency. C1 and C2 should be chosen such that C2 is always equal to or greater than C1.



NOTE 7: C1 and C2 represent the total capacitance on these pins including strays and parasitics, but not the input capacitance of the device pins.

FIGURE 2. EXTERNAL CRYSTAL CONNECTIONS

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Crystal frequency, fx	0°C to 70°C		24		MHz
Crystal frequency tolerance				0.006	%
C1, C2		10	15	20	pF

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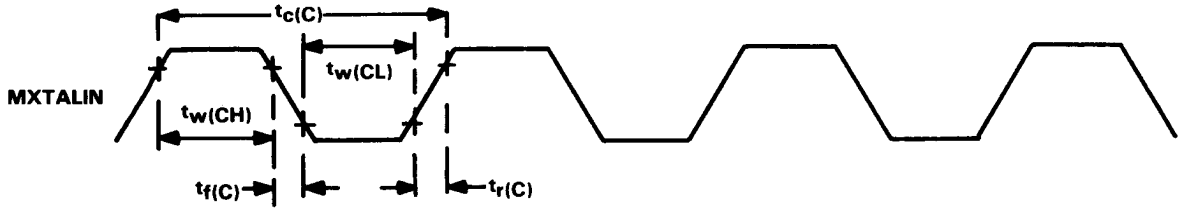
external clock option

An external frequency source can be used by injecting the frequency directly into MXTALIN with MXTAL2 left unconnected. The external source must conform to the following specification.

timing requirements over recommended operating conditions

	PARAMETER	MIN	NOM	MAX	UNIT
f_{ext}	External clock frequency		24		MHz
	External clock tolerance			0.006	%
$t_{c(C)}$	Input clock cycle time		41.7		ns
$t_{r(C)}$	Input clock rise time		5	15	ns
$t_{f(C)}$	Input clock fall time		5	15	ns
$t_{w(CH)}$	Input clock pulse duration high	$½t_{c(C)}-t_{r(C)}$			ns
$t_{w(CL)}$	Input clock pulse duration low	$½t_{c(C)}-t_{f(C)}$			ns

clock timing



LAN ADAPTER BUS CLOCK PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 3)

	PARAMETER	MIN	MAX	UNIT
$t_{c(LA)}$	LAN Adapter bus cycle time (Note 8)	333	333.7	ns
t_{d1}	Delay time, LBCLK2 low to LBCLK2 no longer low in next cycle	4Q − 2	4Q + 2	
t_{d2}	Delay time, LBCLK2 rise to LBCLK2 high in next cycle		4Q + 9	
t_{d3}	Delay time, LBCLK2 no longer low to LBCLK1 no longer low	Q − 3	Q + 3	
t_{d4}	Delay time, LBCLK2 rise to LBCLK1 high		Q + 9	
t_{d5}	Delay time, LBCLK2 no longer low to LBCLK2 no longer high	2Q − 2	2Q + 7	
t_{d6}	Delay time, LBCLK2 rise to LBCLK2 low		2Q + 12	
t_{d7}	Delay time, LBCLK2 no longer low to LBCLK1 no longer high	3Q − 15	3Q − 1	
t_{d8}	Delay time, LBCLK2 rise to LBCLK1 low		3Q	
t_{d9}	Delay time, LBCLK1 low to LBCLK2 high	Q		
t_{d10}	Delay time, LBCLK2 high to LBCLK1 high	Q − 4		
t_{d11}	Delay time, LBCLK1 high to LBCLK2 low	Q − 4		
t_{d12}	Delay time, LBCLK2 low to LBCLK1 low	Q − 16		

NOTES: 8. The LAN Adapter bus cycle time is 333.3 ns ± 0.1%. This value shall be used for calculations requiring the time between successive rising edges of LBCLK2.
9. Q = 0.25 $t_{c(LA)}$.

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LAN ADAPTER BUS READ AND WRITE PARAMETERS

switching characteristics/timing requirements over recommended supply voltage range and operating free-air temperature range (see Figure 3)†

	PARAMETER	MIN	MAX	UNIT
t_{d13}	Delay time, LBCLK2 rise to LI/$\overline{D}$ valid		47	ns
t_{d14}	Delay time, LBCLK2 rise to LAL high		47	
t_{d15}	Delay time, LBCLK2 rise to address valid		47	
t_{d16}	Delay time, LBCLK2 rise to LR/$\overline{W}$ valid		47	
t_{wH1}	Pulse duration, LAL high	Q – 50		
t_{d17}	Delay time, address valid to LAL no longer high	Q – 50		
t_{d18}	Delay time, LAL fall to 1.3 V to address no longer valid	7		
t_{d19}	Delay time, LBCLK1 high to address no longer valid	7		
t_{d20}	Delay time, LBCLK2 rise to LAD, LPH, LPL high impedance in read cycle		Q + 74	
t_{d21}	Delay time, LAD, LPH, LPL high impedance to $\overline{LEN}$ no longer high in read cycle	0		
t_{d22}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in read cycle		Q + 84	
t_{d23}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in write cycle		Q + 47	
t_{d24}	Delay time, LBCLK1 low to $\overline{LEN}$ no longer low in read cycle	0		
t_{d25}	Delay time, LBCLK2 rise to $\overline{LEN}$ high in read cycle		3Q + 47	
t_{d26}	Delay time, LBCLK2 rise to LAL low		2Q – 12	
t_{d27}	Delay time, LBCLK1 low to LAD, LPH, LPL no longer high impedance in next cycle	80		
t_{d28}	Delay time, LBCLK2 rise to write data valid		3Q – 70	
t_{d29}	Delay time, LBCLK1 low to LI/$\overline{D}$, LR/$\overline{W}$ no longer valid	20		
t_{d30}	Delay time, LBCLK1 low to write data no longer valid	20		
t_{d31}	Delay time, LBCLK1 low to $\overline{LEN}$ no longer low in write cycle	20		
t_{d32}	Delay time, LBCLK1 low to $\overline{LEN}$ high in write cycle		80	
t_{d33}	Delay time, LBCLK2 rise to $\overline{LEN}$ no longer high in write cycle	Q – 4		
t_{su1}	Setup time, Read data valid to LBCLK1 no longer high	20		
t_{h1}	Hold time, read data valid after LBCLK1 low if t_{h2} not met	15		
t_{h2}	Hold time, read data valid after $\overline{LEN}$ no longer low if t_{h1} not met	0		
t_{d34}	Delay time, LBCLK2 rise to LBRDY high		2Q – 41	
t_{d35}	Delay time, LBCLK2 rise to LBRDY low		2Q – 21	
t_{h3}	Hold time, LBRDY valid after LBCLK2 low	80		

†This table is entitled switching characteristics/timing requirements because several of the parameters specified can be classified as characteristics or requirements depending on the mode of operation: bus slave or bus master. The values given are valid for both modes.

NOTE 9: Q = $0.25t_{c(LA)}$.

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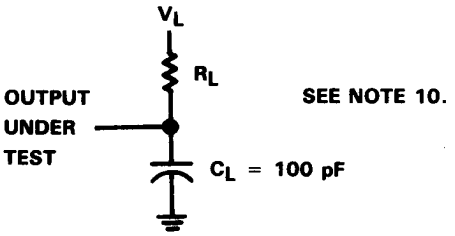
PARAMETER MEASUREMENT INFORMATION



NOTE 10: R_L and V_L are chosen as follows:

$$R_L = \frac{V_{OH} - V_{OL}}{|I_{OL} - I_{OH}|} \qquad V_L = V_{OH} - (I_{OH})(R_L)$$

FIGURE 3. LOAD CIRCUIT

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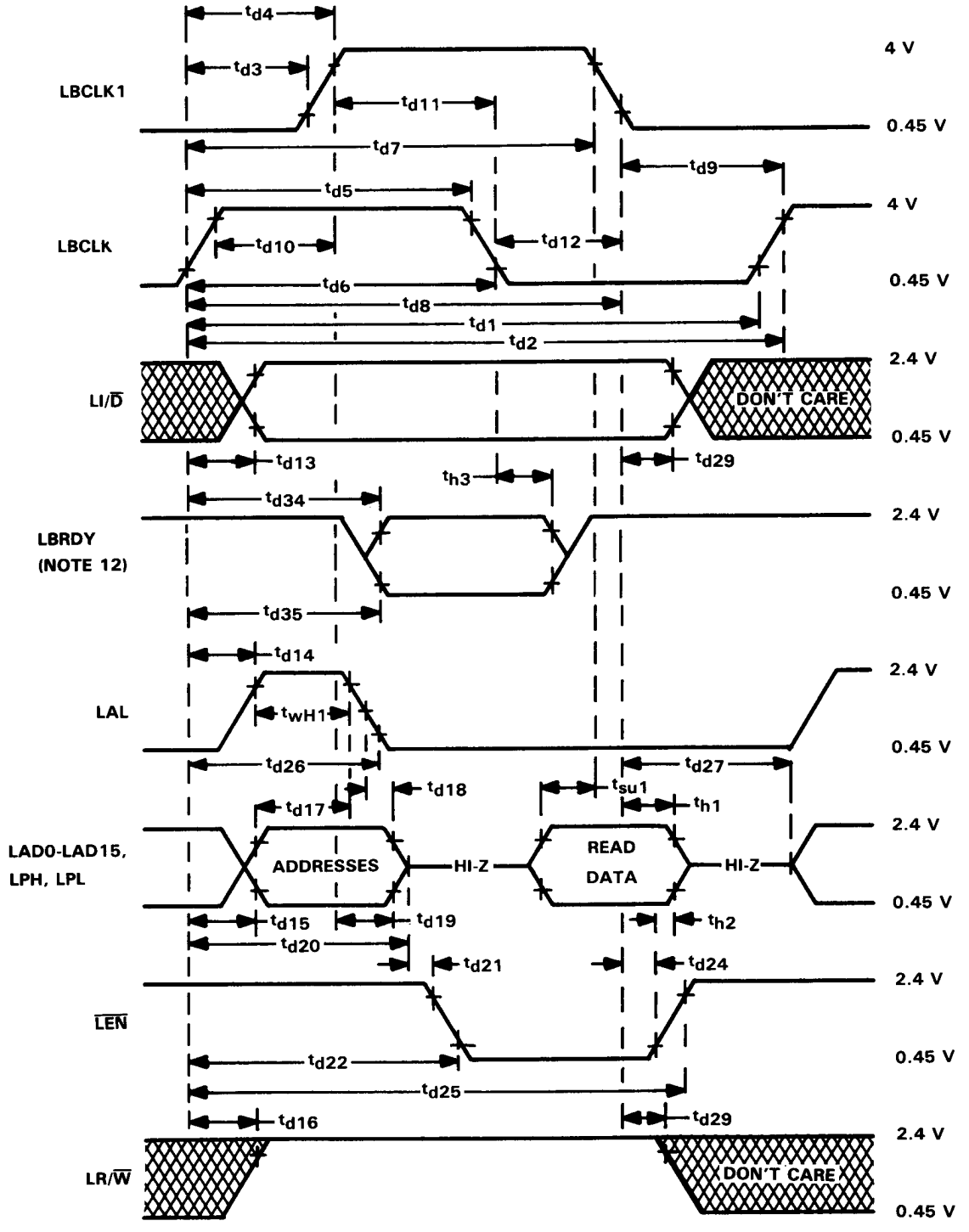
LAN Adapter bus read timing



NOTES: 11. The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V. The intermediate reference point for LAL is 1.3 V.
12. LBRDY should be maintained at a high state unless wait states are required.

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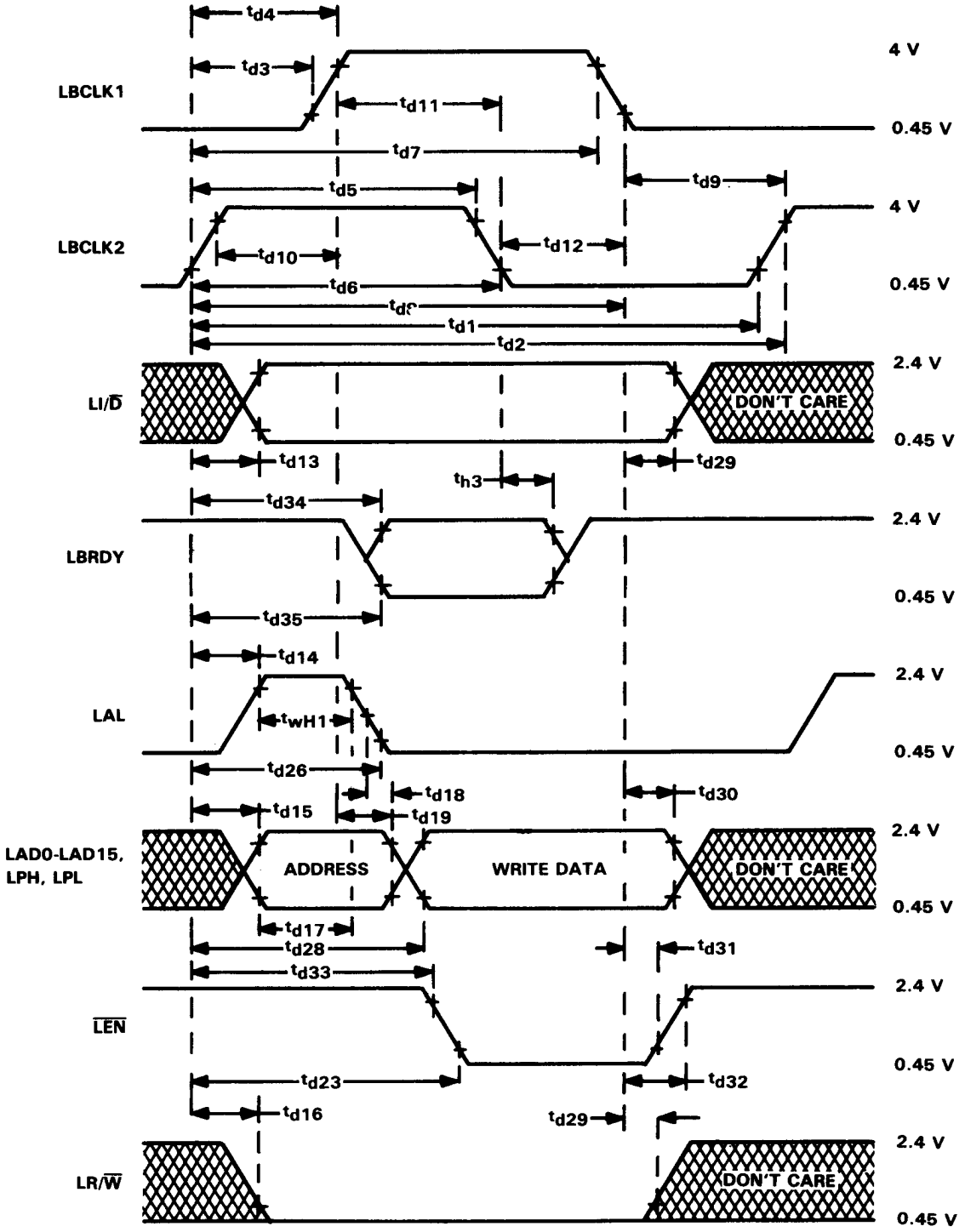
LAN Adapter bus write timing



NOTE 11: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V. The intermediate reference point for LAL is 1.3 V.

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LAN ADAPTER BUS ARBITRATION PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 3)

	PARAMETER	MIN	MAX	UNIT
t_{d36}	Delay time, LBCLK2 rise to $\overline{\text{LBGR1}}$, $\overline{\text{LBGR2}}$ valid		57	ns
t_{d37}	Delay time, LBCLK2 rise to $\overline{\text{LBGR1}}$, $\overline{\text{LBGR2}}$ no longer valid	−6		
t_{d38}	Delay time, LBCLK2 rise to LAL no longer driven low, TMS38010 releases bus	3Q − 15		
t_{d39}	Delay time, LBCLK2 rise to LAL high impedance, TMS38010 releases bus		4Q − 2	
t_{d40}	Delay time, LBCLK2 rise to LAL no longer high impedance, TMS38010 acquires bus	2Q − 9		
t_{d41}	Delay time, LBCLK2 rise to LAL driven low, TMS38010 acquires bus		3Q − 15	
t_{d42}	Delay time, LBCLK2 rise to $\overline{\text{LEN}}$ high impedance, TMS38010 releases bus		74	
t_{d43}	Delay time, LBCLK1 low to $\overline{\text{LEN}}$ no longer high impedance, TMS38010 acquires bus	80		
t_{d44}	Delay time, LBCLK2 rise to $\overline{\text{LEN}}$ driven high, TMS38010 acquires bus		74	
t_{d45}	Delay time, LBCLK1 low to LR/$\overline{\text{W}}$, LI/$\overline{\text{D}}$, LAD0-LAD15, LPH, and LPL high impedance, TMS38010 releases bus		80	
t_{d46}	Delay time, LBCLK1 low to LR/$\overline{\text{W}}$, LI/$\overline{\text{D}}$, LAD0-LAD15, LPH, and LPL no longer high impedance, TMS38010 acquires bus	80		

NOTE 9: Q = 0.25 $t_{c(LA)}$

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{d47}	Delay of $\overline{\text{LBRQ1}}$, $\overline{\text{LBRQ2}}$ from LBCLK1 low		56	ns
t_{h4}	Hold of $\overline{\text{LBRQ1}}$, $\overline{\text{LBRQ2}}$ after LBCLK1 rise	0		

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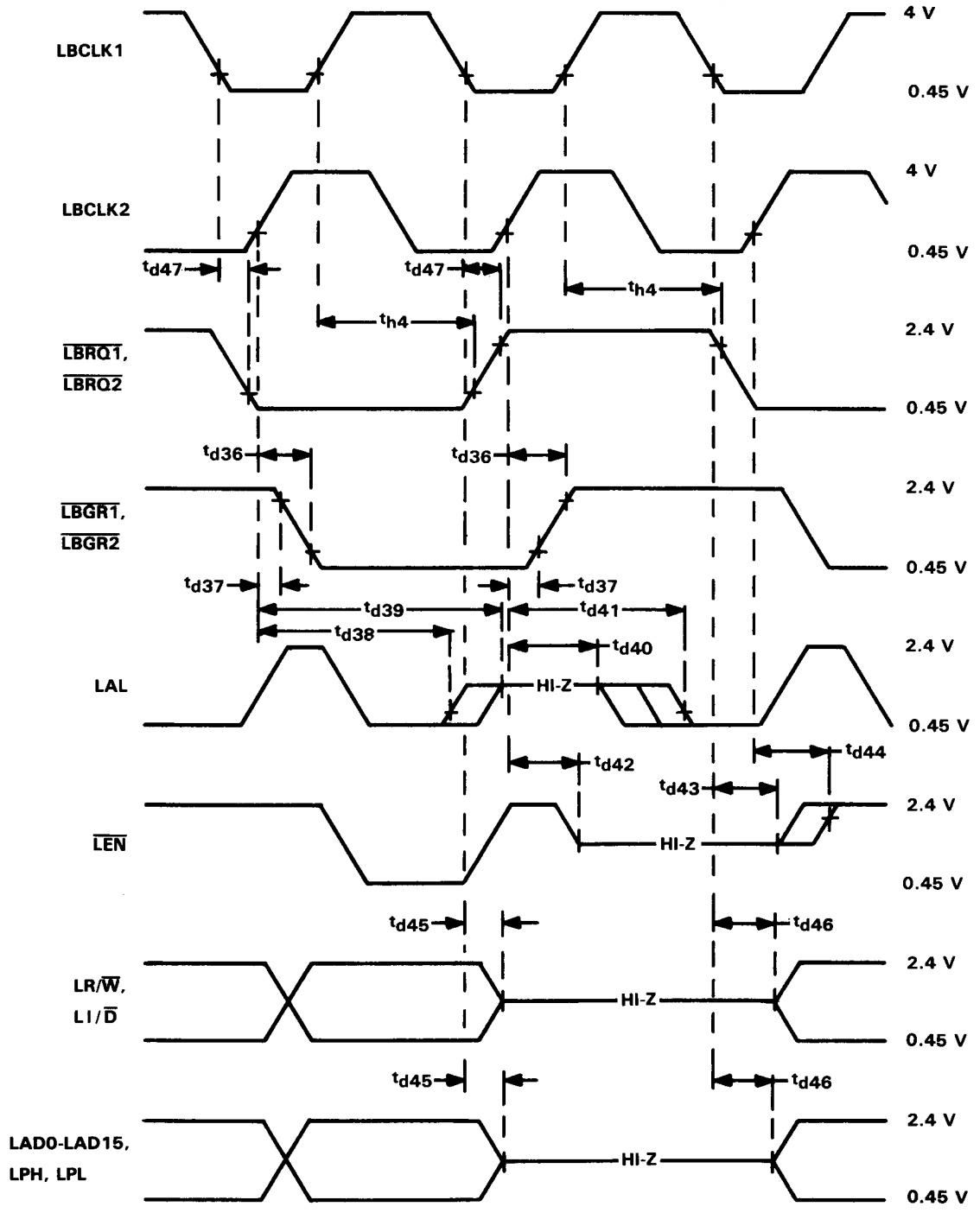
LAN Adapter bus arbitration



NOTE 13: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V.

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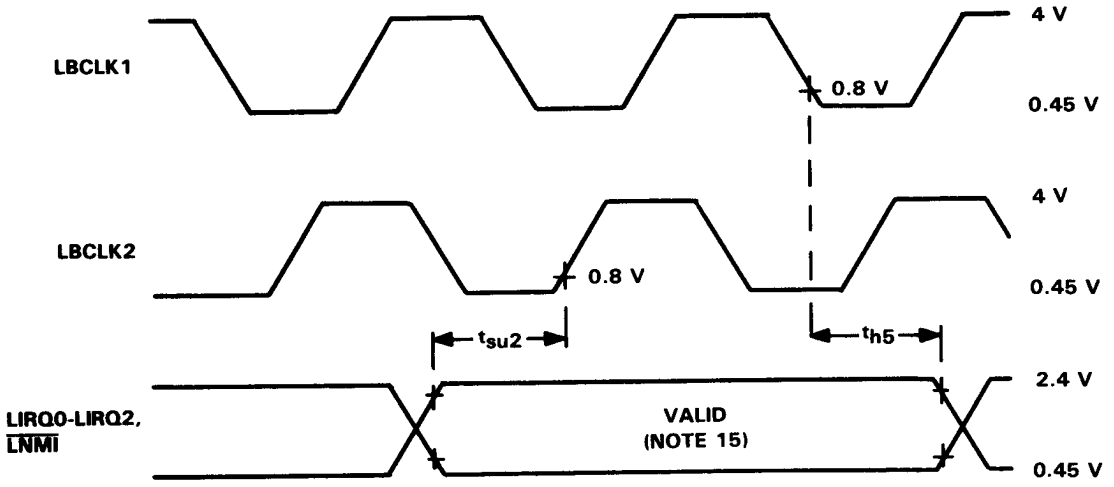
MISCELLANEOUS LAN ADAPTER BUS PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{su2}	Setup time, $\overline{\text{LNMI}}$ or LIRQ0-LIRQ2 valid prior to LBCLK2 rise to guarantee recognition	40		ns
t_{h5}	Hold time, $\overline{\text{LNMI}}$ or LIRQ0-LIRQ2 after LBCLK1 low to guarantee recognition	40		

interrupt timing



NOTES: 14. The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for LIRQ0-LIRQ2 and $\overline{\text{LNMI}}$ are 2 V and 0.8 V.

15. Inputs LIRQ0-LIRQ2 should not change state except during the window when LBCLK1 and LBCLK2 are BOTH low. To meet this requirement, a latch, clocked by the falling edge of LBCLK1, should be added between the LIRQOUT0-LIRQOUT2 outputs of the TMS38030 and the LIRQ0-LIRQ2 inputs of the TMS38010.

MISCELLANEOUS TIMING PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{d48}	Delay from reading minimum V_{CC} during power-up to valid LBCLK1, LBCLK2 with $\overline{\text{LRESET}}$ active		90	ms

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timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
$t_{w(LRS)}$	$\overline{\text{LRESET}}$ pulse duration, asserted with minimum V_{CC} or greater applied, and valid LBCLK1 and LBCLK2	14		μs
$t_{r(LRS)}$	$\overline{\text{LRESET}}$ rise time		100	ns
$t_{r(VCC)}$	V_{CC} rise time from 1.2V to V_{CC} minimum	1		ms

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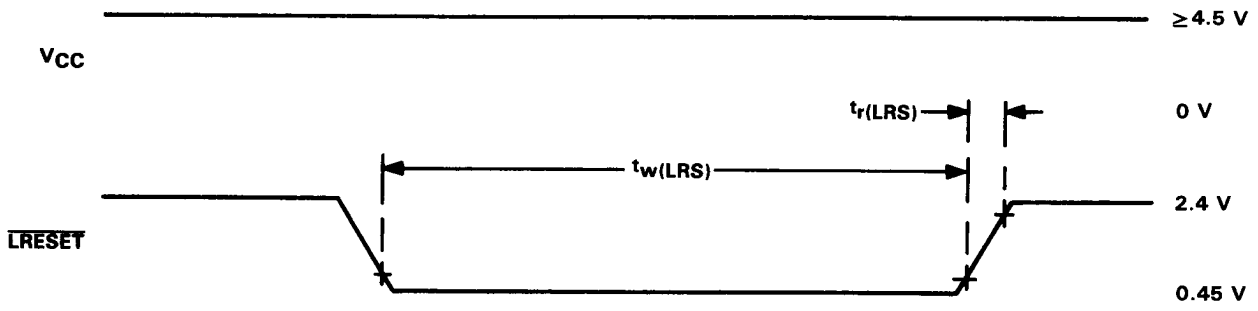
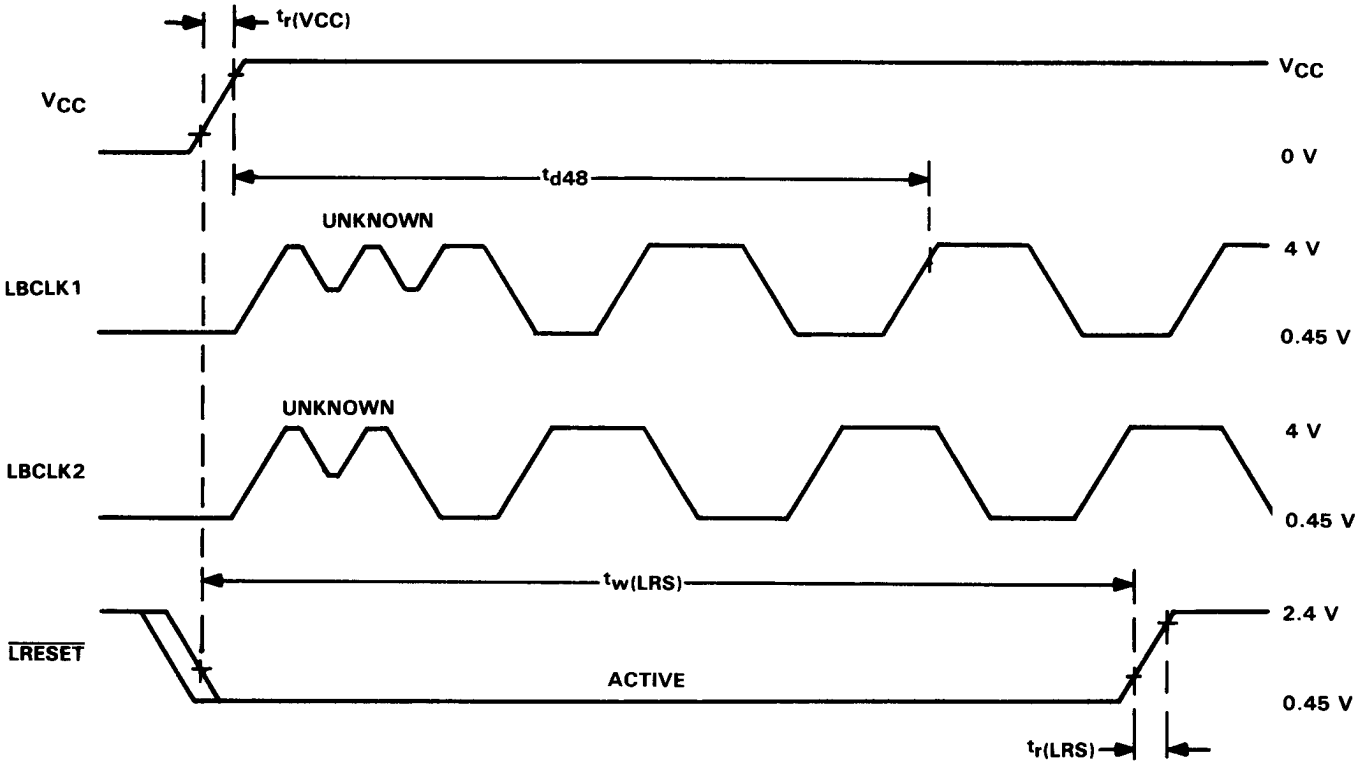
$\overline{\text{LRESET}}$ timing



NOTE 16: The timing reference points are 2 V and 0.8 V.

power-up, LBCLK, and $\overline{\text{LRESET}}$ timing



NOTE 17: The timing reference points for V_{CC} are 4.5 V and 1.2 V. The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for $\overline{\text{LRESET}}$ are 2 V and 0.8 V.

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