Arithmetic Logic Unit for Digital Signal Processing Applications

Description

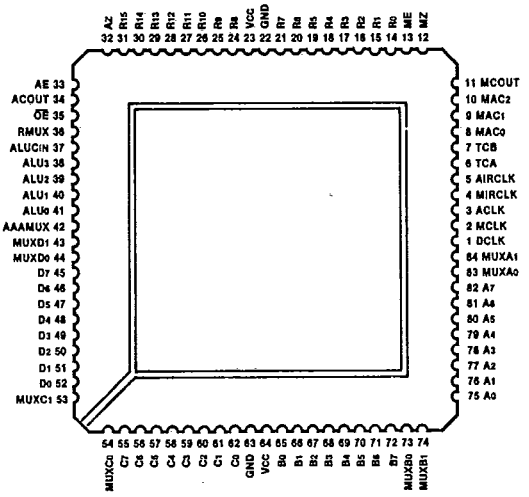
The 'AC/'ACT705 is a high-speed arithmetic processing integrated circuit which is packaged in an 84-pin leadless chip carrier. It features separate input busses that provide data and instruction codes to a high-speed single-cycle 16-bit ALU and an 8-bit by 8-bit parallel multiplier/accumulator.

The ALU is a 16-bit parallel design which supports sixteen arithmetic and logic functions, as well as carry-in/out and borrow-in/out. The multiplier/accumulator, which offers a full 16-bit product, provides for unsigned, signed, mixed mode and imaginary number multiplication. Product accumulation with sum and difference arithmetic is available in each multiplier operating mode.

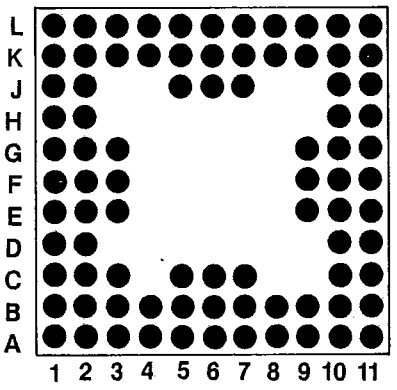
The 16-bit results of the ALU and multiplier/accumulator are multiplexed to a single set of 3-state output buffers. The two ALU and multiplier/accumulator carry-out bits, as well as the 4-bit status field indicating ALU and multiplier/accumulator error conditions make up the remaining six bits of the entire 22-bit output.

- **84-Pin PCC, CPGA**
- **Outputs Source/Sink 8 mA**
- **'ACT705 has TTL-Compatible Inputs**
- **High Throughput Achieved with High Degree of Parallelism in the Architecture**
- **Pipelined Stages**
- **High-Speed 16-Bit ALU and an 8 x 8 Complex Multiplier**
- **31.0 ns (Typical at 25°C, 5.0 V) Cycle 16-Bit Full ALU Performs Sixteen Boolean and Arithmetic Functions with Carry-In and Carry-Out**
- **50.0 ns (Typical at 25°C, 5.0 V) Cycle 8 x 8 Parallel Multiplier Supports Unsigned, Signed, Complex or Mixed Mode Multiplications, Produces 16-Bit Result with Carry-Out**
- **Separate Data and Instruction Busses Allow Instruction Fetches in Parallel with Execution — Single Cycle Operation**
- **Accepts 8- or 16-Bit Data and Delivers a 16-Bit Output**
- **Data Register Bank Configured to Accept a Combination of 8- or 16-Bit Data**

Connection Diagrams



Pin Assignment for PCC



Pin Assignment for CPGA

- **Separate Clocks for ALU Instruction, Multiplier Instruction, Data, ALU Accumulator and Multiplier Accumulator Registers**
- **Clustered Clock Pins for Ease of Board Design**
- **16-Bit ALU/Accumulator with Feedback to ALU Input**
- **Status of Accumulator Inputs is Monitored: Conditions Monitored Include Twos Complement Overflow, Underflow or Equal-to-Zero**

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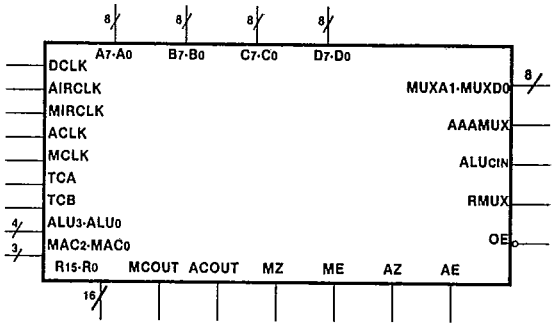
Applications

- Voice-Band Signal Processing
- Discrete Fourier Transform Applications:
  - FIR Filters
  - IIR Filters
- Fast Fourier Transform Applications:
  - Spectrum Analysis
  - Speech Recognition

Ordering Code: See Section 6

Logic Symbol



Pin Names

A_7 - A_0	Data Inputs
B_7 - B_0	Data Inputs
C_7 - C_0	Data Inputs
D_7 - D_0	Data Inputs
DCLK	Data Register Clock
AIRCLK	ALU Instruction Register Clock
MIRCLK	Multiplier Instruction Register Clock
ACLK	ALU Accumulator Register Clock
MCLK	Multiplier Accumulator Clock
TCA, TCB	Multiplier Opcode Input
ALU_3 - ALU_0	ALU Opcode Input
MAC_2 - MAC_0	Multiplier Opcode Input
$MUXA_1$ - $MUXD_0$	Data Configuration Field Inputs
AAAMUX	Multiplier Accumulator Path Enable Input
$ALUC_{IN}$	ALU Carry-In/Borrow-Out Input
RMUX	Multiplexing Input
$\overline{OE}$	Output Enable Input
R_{15} - R_0	Result Output
MCOUT, ACOUT	Carry-Out Outputs
MZ, ME, AZ, AE	Error Status Flag Outputs

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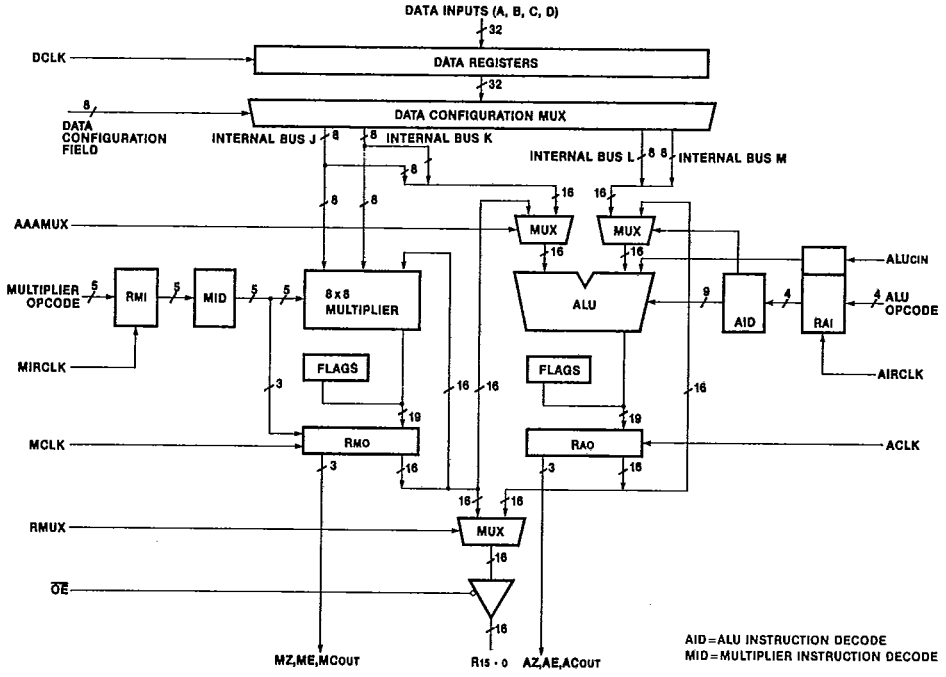
Block Diagram



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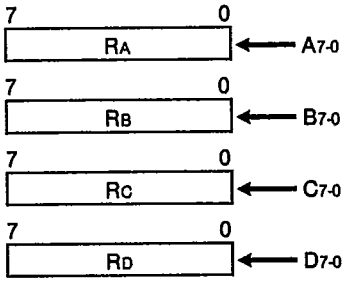
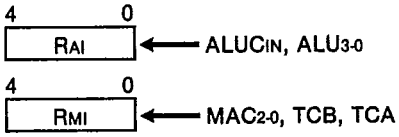
Functional Description

On-Chip Registers

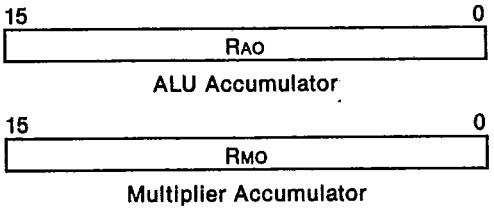
1. Data



2. Instruction

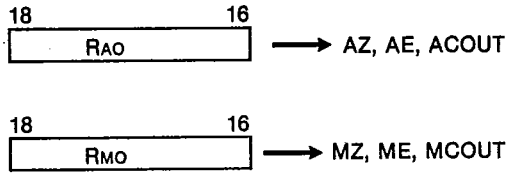


3. Accumulator



Status

4. Flags and Carry-Out



Signal Descriptions

Data Inputs
ALUCIN, A_7 - A_0, B_7 - B_0, C_7 - C_0, D_7 - D_0: Data inputs.

Input Clocks
DCLK, AIRCLK, MIRCLK: Input data is loaded on the rising edge of these clocks.

Outputs
R_{15} - R_0: Result
MCOUT: Multiplier/Accumulator Carry-Out
ACOUT: ALU Carry-Out
MZ, ME, AZ, AE: Error Status Flags

Output Clocks
ACLK, MCLK: Output data is loaded into the output register on the rising edge of this clock.

Other Signals
ALU_3 - ALU_0: ALU Instruction Input
MAC_2 - MAC_0, TCA, TCB: Multiplier Instruction Input
$MUXA_0$, A_1, B_0, B_1, C_0, C_1, D_0, D_1: Multiplexer Select Signals for Input Data

Control Signals

Clock Signals
Dedicated signals for controlling the five sets of positive edge-triggered on-chip registers.
- DCLK: Data Registers (R_A, R_B, R_C, R_D)
- AIRCLK: ALU Instruction Register (R_{AI})
- MIRCLK: Multiplier Instruction Register (R_{MI})
- ACLK: ALU Accumulator Register (R_{AO})
- MCLK: Multiplier/Accumulator Register (R_{MO})

Control Signals, cont'd

ALUCIN
Clocked ALU Carry-In/Borrow-Out Signal.
1 → Carry-In to ALU
0 → Borrow from ALU

MUXA1, MUXA0 . . . MUXD0 (Data Configuration Field, see Table A)
Level signals for configuring the ALU and multiplier operands in 256 possible ways with the contents of RA, RB, RC, RD.
MUXA1, MUXA0: Control the state of internal bus J7 - J0
MUXB1, MUXB0: Control the state of internal bus K7 - K0
MUXC1, MUXC0: Control the state of internal bus L7 - L0
MUXD1, MUXD0: Control the state of internal bus M7 - M0

AAAMUX
Level signal for enabling/disabling the 16-bit multiplier/accumulator path to the ALU.
0 → Path enabled. ALU takes operand from RM0.
1 → Path disabled. ALU takes operand from internal buses J7 - J0 and K7 - K0.

ALU3 - ALU0
Clocked ALU opcode. See Table B.

MAC2 - MAC0, TCB, TCA
Clocked multiplier opcode. See Table C.

RMUX
Level signal for multiplexing the contents of RM0 and RA0.
0 → Output RM015 - RM00
1 → Output RA015 - RA00

$\overline{OE}$
Active LOW Enable signal for making available the 16-bit result, R15 - R0.

Instruction Format

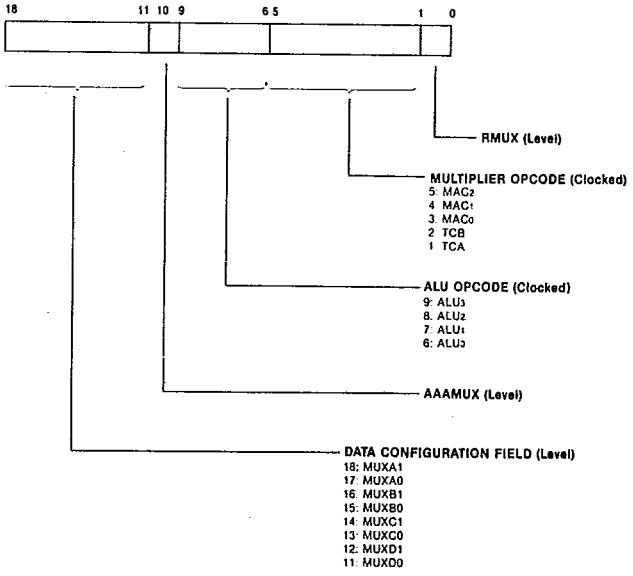


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Table A: Data Input Configuration

Data Configuration Field								Internal Buses			
$MUXA_1$	$MUXA_0$	$MUXB_1$	$MUXB_0$	$MUXC_1$	$MUXC_0$	$MUXD_1$	$MUXD_0$	$J_7 - J_0$	$K_7 - K_0$	$L_7 - L_0$	$M_7 - M_0$
0	0							$R_{A7} - R_{A0}$			
0	1							$R_{B7} - R_{B0}$			
1	0							$R_{C7} - R_{C0}$			
1	1							$R_{D7} - R_{D0}$			
		0	0						$R_{A7} - R_{A0}$		
		0	1						$R_{B7} - R_{B0}$		
		1	0						$R_{C7} - R_{C0}$		
		1	1						$R_{D7} - R_{D0}$		
				0	0					$R_{A7} - R_{A0}$	
				0	1					$R_{B7} - R_{B0}$	
				1	0					$R_{C7} - R_{C0}$	
				1	1					$R_{D7} - R_{D0}$	
						0	0				$R_{A7} - R_{A0}$
						0	1				$R_{B7} - R_{B0}$
						1	0				$R_{C7} - R_{C0}$
						1	1				$R_{D7} - R_{D0}$

Table B: Arithmetic and Logic Operations

Signal										Function
AAAMUX	ALU_3	ALU_2	ALU_1	ALU_0	MAC_2	MAC_1	MAC_0	TCB	TCA	
X	0	0	0	0	X	X	X	X	X	Clear ALU Output
0	0	0	0	1	X	X	X	X	X	$(L_8 - L_0 \parallel M_8 - M_0)$ minus $R_{MO16} - R_{MO0}$
0	0	0	1	0	X	X	X	X	X	$R_{MO16} - R_{M00}$ minus $(L_8 - L_0 \parallel M_8 - M_0)$
0	0	0	1	1	X	X	X	X	X	$R_{MO16} - R_{MO0}$ plus $(L_8 - L_0 \parallel M_8 - M_0)$
0	0	1	0	0	X	X	X	X	X	$R_{MO16} - R_{MO0}$ XOR $(L_8 - L_0 \parallel M_8 - M_0)$
0	0	1	0	1	X	X	X	X	X	$R_{MO16} - R_{MO0}$ OR $(L_8 - L_0 \parallel M_8 - M_0)$
0	0	1	1	0	X	X	X	X	X	$R_{MO16} - R_{MO0}$ AND $(L_8 - L_0 \parallel M_8 - M_0)$
0	0	1	1	1	X	X	X	X	X	$R_{MO16} - R_{MO0}$ plus $\{0\}_{16-0}$
X	1	0	0	0	X	X	X	X	X	Preset ALU Output
0	1	0	0	1	X	X	X	X	X	$R_{AO16} - R_{AO0}$ minus $R_{MO16} - R_{MO0}$
0	1	0	1	0	X	X	X	X	X	$R_{MO16} - R_{MO0}$ minus $R_{AO16} - R_{AO0}$
0	1	0	1	1	X	X	X	X	X	$R_{MO16} - R_{MO0}$ plus $R_{AO16} - R_{AO0}$

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Table B: Arithmetic and Logic Operations, cont'd

Signal										Function
AAAMUX	ALU_3	ALU_2	ALU_1	ALU_0	MAC_2	MAC_1	MAC_0	TCB	BCA	
0	1	1	0	0	X	X	X	X	X	$R_{MO16} - R_{MO0}$ XOR $R_{AO16} - R_{AO0}$
0	1	1	0	1	X	X	X	X	X	$R_{MO16} - R_{MO0}$ OR $R_{AO16} - R_{AO0}$
0	1	1	1	0	X	X	X	X	X	$R_{MO16} - R_{MO0}$ AND $R_{AO16} - R_{AO0}$
0	1	1	1	1	X	X	X	X	X	$R_{MO16} - R_{MO0}$ XOR $\{0\}_{16-0}$
1	0	0	0	1	X	X	X	X	X	$(L_8 - L_0 \parallel M_8 - M_0)$ minus $(J_8 - J_0 \parallel K_8 - K_0)$
1	0	0	1	0	X	X	X	X	X	$(J_8 - J_0 \parallel K_8 - K_0)$ minus $(L_8 - L_0 \parallel M_8 - M_0)$
1	0	0	1	1	X	X	X	X	X	$(J_8 - J_0 \parallel K_8 - K_0)$ plus $(L_8 - L_0 \parallel M_8 - M_0)$
1	0	1	0	0	X	X	X	X	X	$(J_8 - J_0 \parallel K_8 - K_0)$ XOR $(L_8 - L_0 \parallel M_8 - M_0)$
1	0	1	0	1	X	X	X	X	X	$(J_8 - J_0 \parallel K_8 - K_0)$ OR $(L_8 - L_0 \parallel M_8 - M_0)$
1	0	1	1	0	X	X	X	X	X	$(J_8 - J_0 \parallel K_8 - K_0)$ AND $(L_8 - L_0 \parallel M_8 - M_0)$
1	0	1	1	1	X	X	X	X	X	$(J_8 - J_0 \parallel K_8 - K_0)$ plus $\{0\}_{16-0}$
1	1	0	0	1	X	X	X	X	X	$R_{AO16} - R_{AO0}$ minus $(J_8 - J_0 \parallel K_8 - K_0)$
1	1	0	1	0	X	X	X	X	X	$(J_8 - J_0 \parallel K_8 - K_0)$ minus $R_{AO16} - R_{AO0}$
1	1	0	1	1	X	X	X	X	X	$(J_8 - J_0 \parallel K_8 - K_0)$ plus $R_{AO16} - R_{AO0}$
1	1	1	0	0	X	X	X	X	X	$(J_8 - J_0 \parallel K_8 - K_0)$ XOR $R_{AO16} - R_{AO0}$
1	1	1	0	1	X	X	X	X	X	$(J_8 - J_0 \parallel K_8 - K_0)$ OR $R_{AO16} - R_{AO0}$
1	1	1	1	0	X	X	X	X	X	$(J_8 - J_0 \parallel K_8 - K_0)$ AND $R_{AO16} - R_{AO0}$
1	1	1	1	1	X	X	X	X	X	$(J_8 - J_0 \parallel K_8 - K_0)$ XOR $\{0\}_{16-0}$

Note: Combination of ALU and multiplier opcodes allowed.

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Table C: Multiplication Operations

Signal										Function
AAAMUX	ALU_3	ALU_2	ALU_1	ALU_0	MAC_2	MAC_1	MAC_0	TCB	TCA	
X	X	X	X	X	0	0	0	0	0	(J_8 - J_0 x K_8 - K_0)
X	X	X	X	X	0	0	0	0	1	(J'_8 - J'_0 x K_8 - K_0)
X	X	X	X	X	0	0	0	1	0	(J_8 - J_0 x K'_8 - K'_0)
X	X	X	X	X	0	0	0	1	1	(J'_8 - J'_0 x K'_8 - K'_0)
X	X	X	X	X	0	0	1	0	0	(J_8 - J_0 x K_8 - K_0) plus RMO'_{16} - RMO'_0
X	X	X	X	X	0	0	1	0	1	(J'_8 - J'_0 x K_8 - K_0) plus RMO'_{16} - RMO'_0)
X	X	X	X	X	0	0	1	1	0	(J_8 - J_0 x K'_8 - K'_0) plus RMO'_{16} - RMO'_0
X	X	X	X	X	0	0	1	1	1	(J'_8 - J'_0 x K'_8 - K'_0) plus RMO'_{16} - RMO'_0
X	X	X	X	X	0	1	0	X	X	Clear RMO_{16} - RMO_0
X	X	X	X	X	0	1	1	0	0	Undefined
X	X	X	X	X	0	1	1	0	1	(J'_8 - J'_0 x K_8 - K_0) minus RMO'_{16} - RMO'_0)
X	X	X	X	X	0	1	1	1	0	(J_8 - J_0 x K'_8 - K'_0) minus RMO'_{16} - RMO'_0
X	X	X	X	X	0	1	1	1	1	(J'_8 - J'_0 x K'_8 - K'_0) minus RMO'_{16} - RMO'_0
X	X	X	X	X	1	0	0	0	0	Undefined
X	X	X	X	X	1	0	0	0	1	(-J'_8 - J'_0 x K_8 - K_0)
X	X	X	X	X	1	0	0	1	0	(-J_8 - J_0 x K'_8 - K'_0)
X	X	X	X	X	1	0	0	1	1	(-J'_8 - J'_0 x K'_8 - K'_0)
X	X	X	X	X	1	0	1	0	0	Undefined
X	X	X	X	X	1	0	1	0	1	(-J'_8 - J'_0 x K_8 - K_0) plus RMO'_{16} - RMO'_0
X	X	X	X	X	1	0	1	1	0	(-J_8 - J_0 x K'_8 - K'_0) plus RMO'_{16} - RMO'_0
X	X	X	X	X	1	0	1	1	1	(-J'_8 - J'_0 x K'_8 - K'_0) plus RMO'_{16} - RMO'_0
X	X	X	X	X	1	1	0	X	X	Preset RMO_{16} - RMO_0
X	X	X	X	X	1	1	1	0	0	Undefined
X	X	X	X	X	1	1	1	0	1	(-J'_8 - J'_0 x K_8 - K_0) minus RMO'_{16} - RMO'_0
X	X	X	X	X	1	1	1	1	0	(-J_8 - J_0 x K'_8 - K'_0) minus RMO'_{16} - RMO'_0
X	X	X	X	X	1	1	1	1	1	(-J'_8 - J'_0 x K'_8 - K'_0) minus RMO'_{16} - RMO'_0

Notes: Combination of ALU and multiplier opcodes allowed.
' stands for twos complement representation of a number.

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DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74AC/ACT 25°C	54AC/ACT	74AC/ACT	Units	Conditions
		Typ	Guaranteed Limit			
I_{IN}	Maximum Input Current		0.1	10.0	1.0	μA	V_{CC} = Max V_{IN} = V_{CC}
I_{OZ}	Maximum 3-State Current		0.5	10.0	5.0	μA	High Z, V_{CC} = Max V_{OUT} = 0 to V_{CC}
I_{CCQ}	Supply Current, Quiescent	50.0	2.0	10.0	10.0	mA	V_{CC} = Max, V_{IN} = 0 V
V_{OH}	Minimum HIGH Level Output	4.49	4.4	4.4	4.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		5.49	5.4	5.4	5.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			3.86	3.70	3.76	V	I_{OH} = −8 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = −8 mA, V_{CC} = 5.5 V
V_{OL}	Maximum HIGH Level Output	0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 4.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 5.5 V
I_{OLD}	Minimum Dynamic Output Current			32	32	mA	V_{CC} = 5.5 V V_{OLD} = 2.2 V
I_{OHD}	Minimum Dynamic Output Current			−32	−32	mA	V_{CC} = 5.5 V V_{OHD} = 3.3 V

Note 1: Test Load 50 pF, 500 ohm to Ground

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_A	Arithmetic Operation Time	3.3 5.0		31.0						ns	1
t_L	Logic Operation Time	3.3 5.0		24.0						ns	1
t_M	Multiply Time	3.3 5.0		50.0						ns	2
t_D	Output Delay	3.3 5.0		7.0						ns	1,2
t_{ENA}	3-State Output Enable Delay	3.3 5.0		7.0						ns	1,2
t_{DIS}	3-State Output Disable Delay	3.3 5.0		8.5						ns	1,2
t_s	Input Register Setup Time	3.3 5.0		3.0						ns	1,2
t_h	Input Register Hold Time	3.3 5.0		0						ns	1,2
t_w	Clock Pulse Width	3.3 5.0		5.0						ns	1,2

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

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Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_A	Arithmetic Operation Time	5.0		31.0						ns	1
t_L	Logic Operation Time	5.0		24.0						ns	1
t_M	Multiply Time	5.0		50.0						ns	2
t_D	Output Delay	5.0		7.0						ns	1,2
t_{ENA}	3-State Output Enable Delay	5.0		7.0						ns	1,2
t_{DIS}	3-State Output Disable Delay	5.0		8.5						ns	1,2
t_s	Input Register Setup Time	5.0		3.0						ns	1,2
t_h	Input Register Hold Time	5.0		0						ns	1,2
t_w	Clock Pulse Width	5.0		5.0						ns	1,2

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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Waveforms

Figure 1: Arithmetic Logic Operation

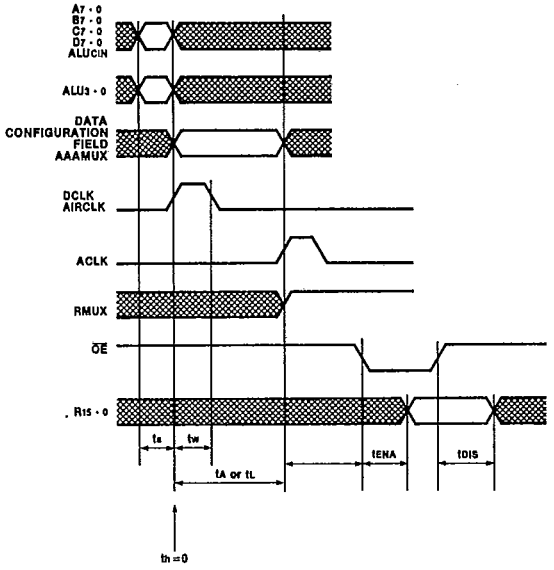
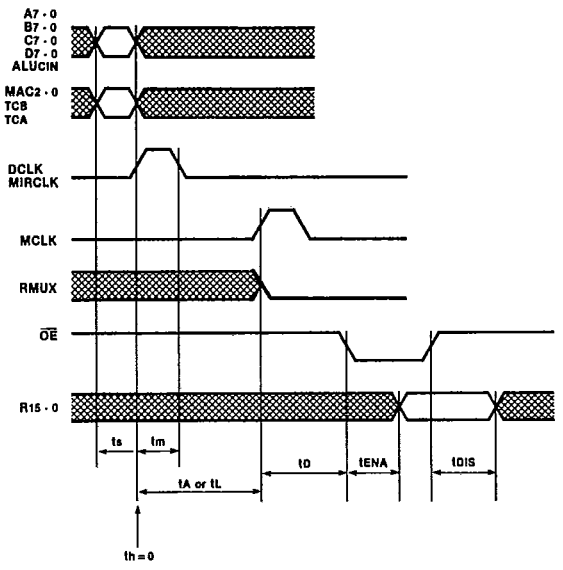


Figure 2: Multiplication



CPGA Pinout

T-49-11

Pinout to Signal

Pinout	Signal	Pinout	Signal
A1	MCOUT	F3	GND_2
A2	MAC_1	F9	VCG_1
A3	MAC_0	F10	C_2
A4	TCA	F11	B_0
A5	ACLK	G1	R_8
A6	MCLK	G2	R_9
A7	$MUXA_0$	G3	VCC_2
A8	A_5	G9	GND_1
A9	A_3	G10	C_1
A10	A_2	G11	C_0
A11	$MUXB_1$	H1	R_{11}
B1	R_0	H2	R_{12}
B2	MZ	H10	C_4
B3	MAC_2	H11	C_3
B4	TCB	J1	R_{13}
B5	MIRCLK	J2	R_{15}
B6	A_6	J5	ALU_2
B7	A_7	J6	$MUXD_1$
B8	A_4	J7	$MUXD_0$
B9	A_1	J10	C_7
B10	A_0	J11	C_5
B11	B_7	K1	R_{14}
C1	R_1	K2	AE
C2	ME	K3	ACOUT
C3	NO CONNECTION	K4	$ALUC_{IN}$
		K5	ALU_1
C5	AIRCLK	K6	AAAMUX
C6	DCLK	K7	D_6
C7	$MUXA_1$	K8	D_3
C10	$MUXB_0$	K9	D_0
C11	B_6	K10	$MUXC_0$
D1	R_3	K11	C_6
D2	R_2	L1	$\overline{AZ}$
D10	B_5	L2	$\overline{OE}$
D11	B_4	L3	RMUX
E1	R_6	L4	ALU_3
E2	R_5	L5	ALU_0
E3	R_4	L6	D_5
E9	B_3	L7	D_7
E10	B_2	L8	D_4
E11	B_1	L9	D_2
F1	R_{10}	L10	D_1
F2	R_7	L11	MUXC1

Signal to Pinout

Signal	Pinout	Signal	Pinout
MZ	B2	$MUXC_0$	K10
ME	C2	C_7	J10
R_0	B1	C_6	K11
R_1	C1	C_5	J11
R_2	D2	C_4	H10
R_3	D1	C_3	H11
R_4	E3	C_2	F10
R_5	E2	C_1	G10
R_6	E1	C_0	G11
R_7	F2	GND_1	G9
GND_2	F3	VCC_1	F9
VCC_2	G3	B_0	F11
R_8	G1	B_1	E11
R_9	G2	B_2	E10
R_{10}	F1	B_3	E9
R_{11}	H1	B_4	D11
R_{12}	H2	B_5	D10
R_{13}	J1	B_6	C11
R_{14}	K1	B_7	B11
R_{15}	J2	$MUXB_0$	C10
AZ	L1	$MUXB_1$	A11
AE	K2	A_0	B10
ACOUT	K3	A_1	B9
$\overline{OE}$	L2	A_2	A10
RMUX	L3	A_3	A9
$ALUC_{IN}$	K4	A_4	B8
ALU_3	L4	A_5	A8
ALU_2	J5	A_6	B6
ALU_1	K5	A_7	B7
ALU_0	L5	$MUXA_0$	A7
AAAMUX	K6	$MUXA_1$	C7
MUXD1	J6	DCLK	C6
$MUXD_0$	J7	MCLK	A6
D_7	L7	ACLK	A5
D_6	K7	MIRCLK	B5
D_5	L6	AIRCLK	C5
D_4	L8	TCA	A4
D_3	K8	TCB	B4
D_2	L9	MAC_0	A3
D_1	L10	MAC_1	A2
D_0	K9	MAC_2	B3
$MUXC_1$	L11	MCOUT	A1

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