



AWT921S11

Integrated High Power Amp 900 MHz
Advanced Product information
Rev. 6

DESCRIPTION

The AWT921 is a monolithic amplifier for use in communication systems that require high gain and output intercept point. This device has been specifically designed for multi carrier and micro cell base station applications.

FEATURES

- High output power levels
- High Efficiency
- True Surface Mount Package with Integrated Heat Slug
- Internal Bias Circuit Requiring Nominal Input Voltages $\pm 10\%$
- Low Cost
- Off Chip Output Matching Circuit Allows Application Optimization



S11
SSOP-28 Wide Body
28 Pin Wide Body w/ Heat Slug

ABSOLUTE MAXIMUM RATINGS

PIN	SIGNAL	MAX RATING	PIN	SIGNAL	MAX RATING
2	V_{DD}	$+7V_{DC}$	11	V_{REF}	$+7 V_{DC}$
3	RF_{IN}	$+20 \text{ dBm}$	12	V_{SS}	$-7 V_{DC}$
4,5	V_{D1}	$+10 V_{DC}$	18,19,20,21,22,23,24,25	V_{D3}	$+10 V_{DC}$
8,9	V_{D2}	$+10 V_{DC}$			

Operating Temperature: -30 to $+85^\circ \text{C}$

Storage Temperature: -55 to $+100^\circ \text{C}$

ELECTRICAL SPECIFICATIONS: ⁽¹⁾(Pin +12 dBm, fo = 925-960 MHz, V_{DS1} = V_{DS2} = V_{DS3} = 8.5V, V_{SS} = -3V, V_{REF} = +5V, V_{DD} = +5V, Tc=25°C, 50Ω System ⁽²⁾)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Frequency	fo	925	-	960	MHz
Power Output	P _{OUT}	-	+39	-	dBm
Power Added Efficiency	η _{Eff}	-	40	-	%
Gain @ P _{OUT} = +39 dBm @ P _{OUT} = +30 dBm	PG	-	29 30	-	dB
Harmonics ⁽³⁾ 2nd 3rd 4th	-	-	37 47 50	-	dBc
Stability: -60 dBc all spurious outputs relative to desired signal	-	-	3:1	-	VSWR load, all phase angles
Bias supply currents	I _{SS} I _{REF} I _{DD}	-	8 1.2 8	-	mA mA mA
Quiescent Currents	I _{DQ1} I _{DQ2} I _{DQ3}	-	100 250 200	-	mA mA mA
Input Return Loss		10	-	-	dB
Gain Flatness vs. Frequency @ P _{out} = +39 dBm @ P _{out} = +30 dBm	ΔPG	±0.5 ±0.5	-	-	dB dB
Thermal Resistance ⁴	-	-	4.5	-	C/W

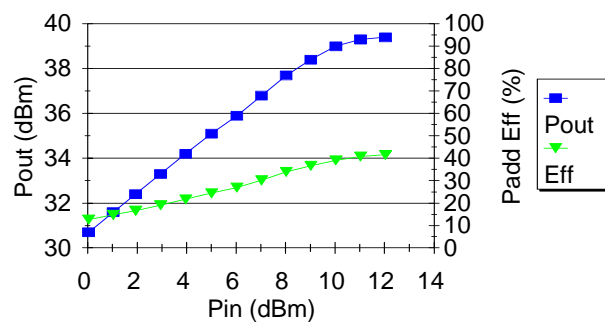
NOTES:

- As measured in ANADIGICS test fixture, see application section
- 50Ω Measurement system after off chip matching circuit, input terminated in 50Ω
- Measured at P_{out} = +39 dBm
- Thermal resistance for junction to bottom of slug. Q_{jc} = (T_j - T_c) / ((I_{D1} + I_{D2} + I_{D3}) * V_{SUP} - P_{OUT})

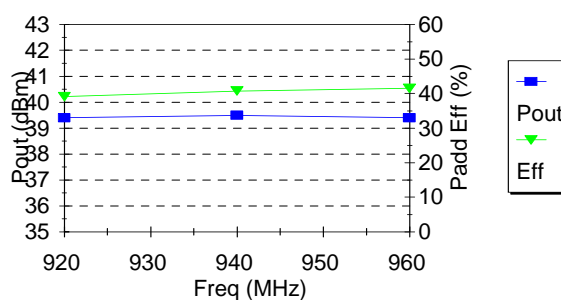
CHARACTERIZATION DATA ⁽¹⁾ -

Conditions unless otherwise stated (Pin +12 dBm, fo = 925-960 MHz, V_{DS1} = V_{DS2} = V_{DS3} = 8.5V, V_{SS} = -3V, V_{REF} = +5V, V_{DD} = +5V, Tc=25°C, 50 W system ⁽²⁾)

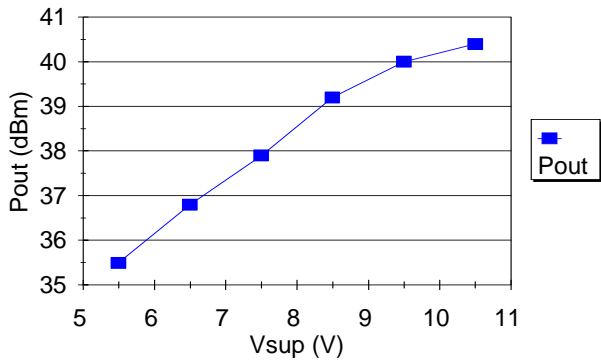
Pout & Eff vs. Pin



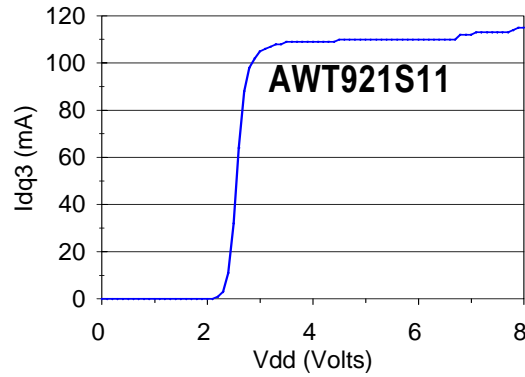
Pout & Eff vs. Frequency



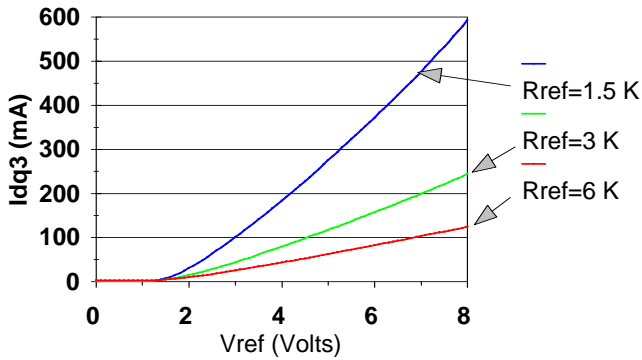
Pout vs. Supply Voltage



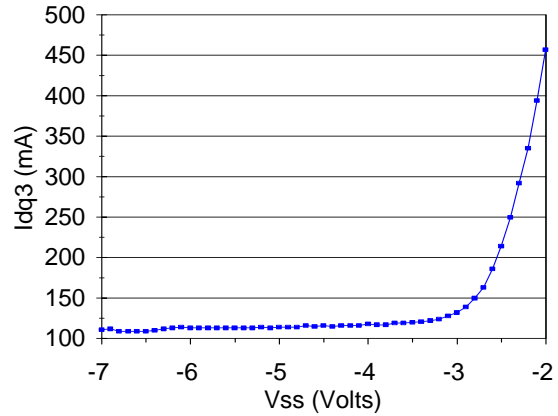
Idq3 vs Vdd



Idq3 vs Vref



Idq3 vs Vss



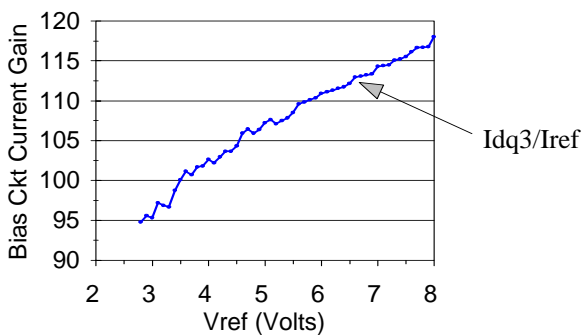
Notes:

- 1: As measured in ANADIGICS test fixture, see application section
- 2: 50Ω Measurement system after off chip matching circuit, input terminated in 50Ω

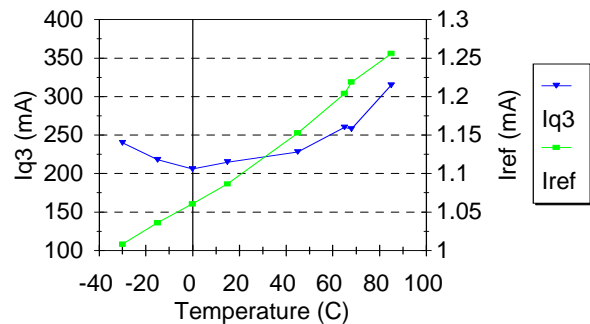
CHARACTERIZATION DATA: ⁽¹⁾

Conditions unless otherwise stated (Pin +12 dBm, fo = 925-960 MHz,
 $V_{DS1} = V_{DS2} = V_{DS3} = 8.5V$, $V_{SS} = -3V$, $V_{REF} = +5V$, $V_{DD} = +5V$, $T_c = 25^\circ C$, 50Ω system) ⁽²⁾

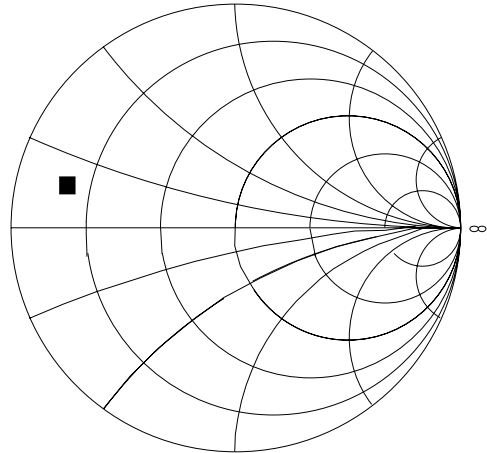
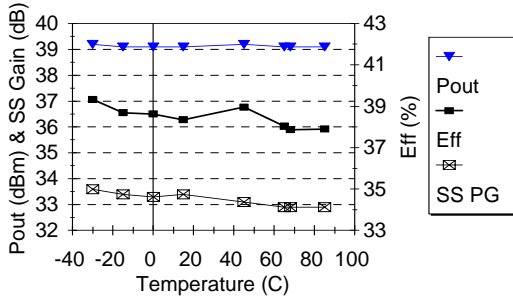
Bias Ckt Gain vs Vref



Iq3 & Iref vs Temperature

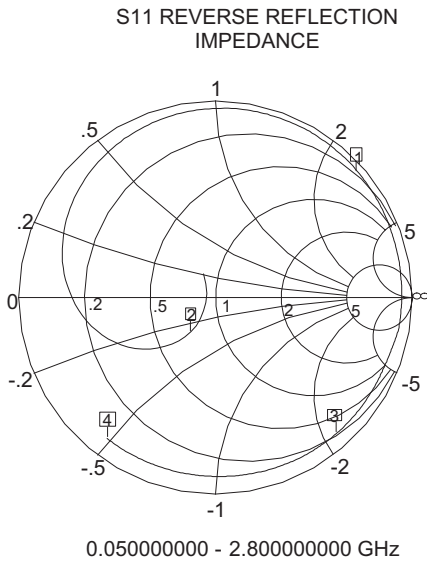


Pout,PG,& Eff vs Temperature



Load + 3.7 + 3.9 jΩ

Output Load Impedance as seen by the device



CH 4 - S11
REFERENCE PLANE
9.0821 cm

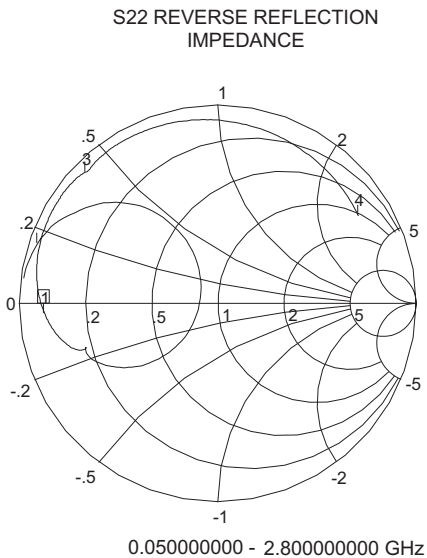
MARKER 1
0.957500000 GHz
7.074 Ω
131.906 jΩ

MARKER TO MAX
MARKER TO MIN

- 2 0.098125000 GHz
36.919 Ω
-13.501 jΩ
- 3 1.920000000 GHz
11.446 Ω
-111.641 jΩ
- 4 2.800000000 GHz
3.133 Ω
-24.550 jΩ

MARKER READOUT
FUNCTIONS

Impedance as seen by V_{DS1}



TRACE MEMORY
DISK OPERATIONS

CHANNEL 4

SAVE MEMORY
TO HARD DISK

SAVE MEMORY
TO FLOPPY DISK

RECALL MEMORY
FROM HARD DISK

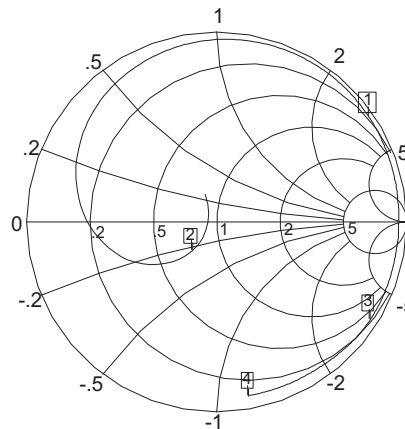
RECALL MEMORY
FROM FLOPPY DISK

PRESS<ENTER>
TO SELECT

0.050000000 - 2.800000000 GHz

Output Impedance as seen by V_{DS3}

S11 REVERSE REFLECTION
IMPEDANCE



CH 4 - S11

REFERENCE PLANE
9.0821 cm

MARKER 1
0.957500000 GHz
7.659 Ω
161.181 jΩ

MARKER TO MAX
MARKER TO MIN

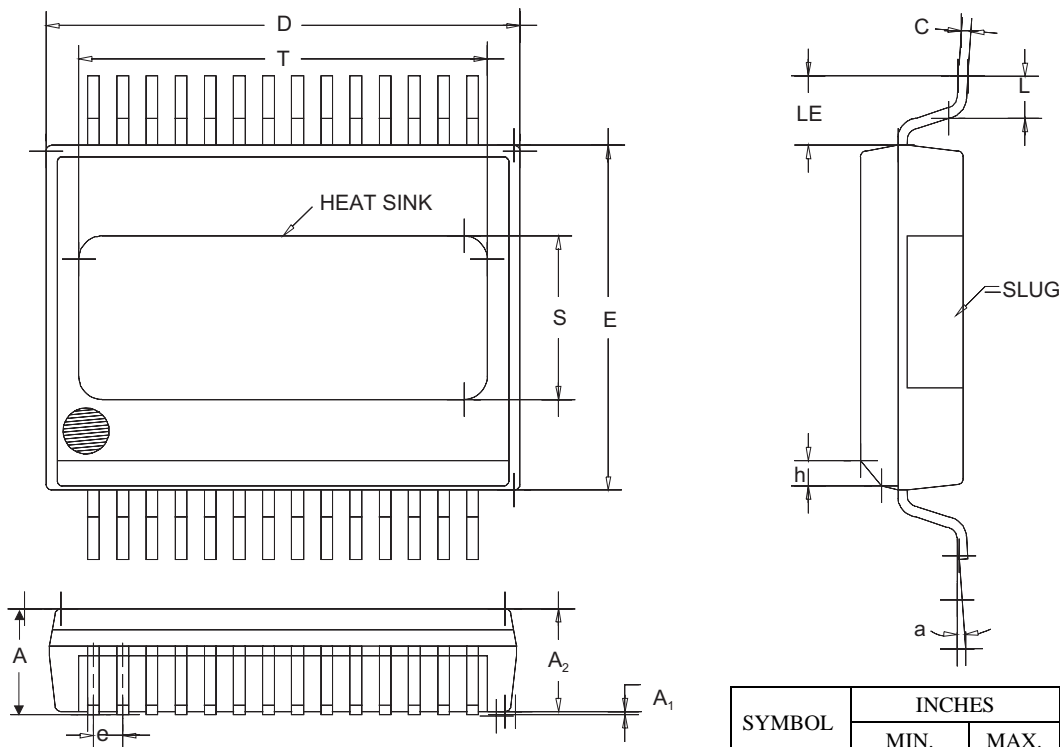
- 2 0.098125000 GHz
37.237 Ω
-11.817 jΩ
- 3 1.920000000 GHz
13.308 Ω
-171.126 jΩ
- 4 2.800000000 GHz
4.466 Ω
-60.044 jΩ

MARKER READOUT
FUNCTIONS

0.050000000 - 2.800000000 GHz

Impedance as seen V_{DS2}

PACKAGE OUTLINE DRAWING



Notes:

1. Controlling dimensions : inches.
2. Dimension "d" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.006 (0.16mm).
3. Dimension "e" does not include inter-lead or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 (0.25mm) per side.
4. Maximum lead twist/skew to be 0.002 (0.05mm).
5. Mold flash shall not extend more than 0.010 (0.25mm) on any edge of heat slug.

SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.087	0.093	2.21	2.36	
A ₁	0.000	0.004	0.00	0.10	
A ₂	0.087	0.089	2.21	2.25	
B	0.008	0.012	0.36	0.46	
C	0.007	0.009	0.18	0.25	
D	0.400	0.408	10.16	10.36	2
E	0.292	0.296	7.42	7.52	2
e	0.025	BSC	0.64	BSC	4
H	0.410	0.418	10.41	40.62	
h	0.018	0.024	0.48	0.61	
L	0.034	0.038	0.86	0.97	
LE	0.84		1.37		
a	0	8	0	8	
S	0.139	0.141	3.54	3.55	5
T	0.349	0.351	8.86	8.92	5

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