CHRONTEL

Dual Programmable Clock Generator

Features

- Generates 15 preset video clock frequencies and 3 preset memory clock frequencies
- Two independently programmable video and memory clock outputs
- Supports output frequencies up to 130 MHz
- Draws less than 1 μA while in power down mode for "Green PC" applications
- Requires only four external components: one 14.318 MHz crystal and three 0.1 μF capacitors
- Proprietary VCO design for low-phase jitter
- Supports graphics standards such as EGA, VGA, Super-VGA, XGA™, and 8514
- Pin compatible to CH920x series and ICS1394
- CMOS technology in 20-pin PDIP and SOIC
- 5V or 3.3V supply. For specific details on the 3.3V version, please consult Chrontel.

Description

CH9203 is a dual PLL clock generator designed for low power and high performance applications, such as graphics systems based on the VGA, Super-VGA, XGA™, and 8514 formats. CH9203 has a power down mode that typically draws less than 1 μA of supply current, making it ideal for notebook, palmtop, and other portable applications. It is also well-suited for applications requiring multiple clocks, such as disk drives, CD-ROM systems, and modems.

CH9203 provides separate memory (MCLK) and video (VCLK) clocks. The minimum and maximum frequencies of both clock outputs can be as low as 8 MHz, and as high as 130 MHz. The reference frequency is 14.318 MHz, which is derived from either a crystal or an external reference frequency. Other input frequencies can be used to obtain different output frequencies.
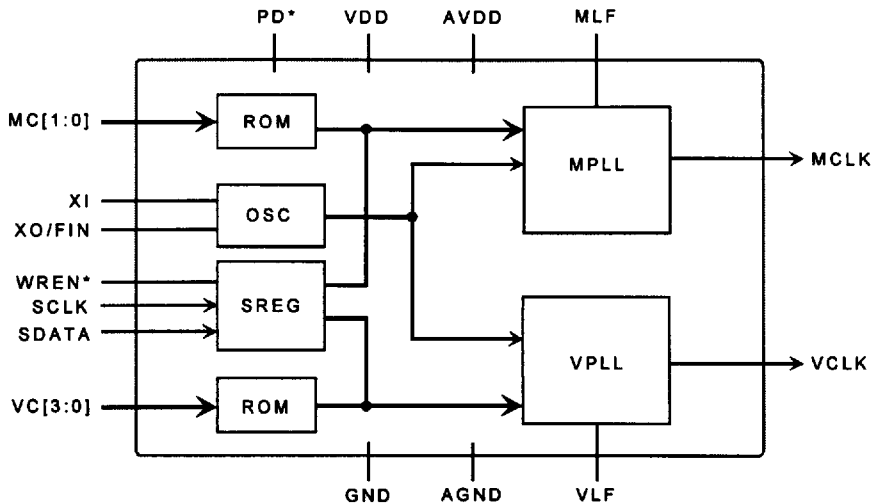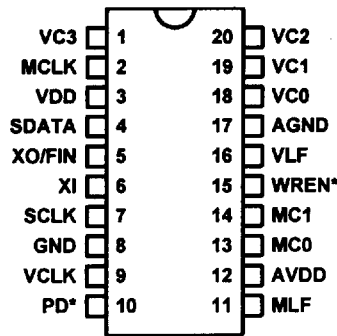
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Figure 1: Block Diagram

Figure 2: CH9203CL

Table 1 • Pin Description CH9203CL

Pin	Type	Symbol	Description
1, 18, 19, 20	In	VC3, VC0, VC1, VC2	Video clock select inputs (internal pull-up)
2	Out	MCLK	Memory clock output
3	Power	VDD	5V supply
4	In	SDATA	Serial data input (internal pull-up)
5	Out / In	XO / FIN	Crystal output or external FREF input
6	In	XI	Crystal input
7	In	SCLK	Serial clock input (positive edge triggered, internal pull-down)
8	Power	GND	Ground
9	Out	VCLK	VCLK clock output
10	In	PD*	Power down input (active low)
11	In	MLF	Memory loop filters
12	Power	AVDD	Analog 5V supply
13, 14	In	MC0, MC1	Memory clock select inputs (internal pull-up)
15	In	WREN*	Serial data write enable (active low, internal pull-up)
16	In	VLF	Video loop filters
17	Power	AGND	Analog ground

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Table 1 • Frequencies for CH9203CL (in MHz)

Video Clock

VC3	VC2	VC1	VC0	VCLK
0	0	0	0	25.175
0	0	0	1	28.322
0	0	1	0	40.0
0	0	1	1	Serial Prog
0	1	0	0	50.0
0	1	0	1	77.0
0	1	1	0	36.0
0	1	1	1	44.9
1	0	0	0	130.0
1	0	0	1	120.0
1	0	1	0	80.0
1	0	1	1	31.5
1	1	0	0	110.0
1	1	0	1	65.0
1	1	1	0	75.0
1	1	1	1	94.5

Memory Clock

MC1	MC0	MCLK
0	0	50.0
0	1	55.0
1	0	Serial Prog
1	1	60.0

Power Down Mode

When power down is active (logic low), CH9203 is placed in standby mode, drawing less than 1 µA of current. All outputs are tristated and both internal PLLs are disabled to minimize power consumption. After power up, CH9203 typically requires 40 milliseconds for the PLLs to stabilize.

Variable Output Drive Current

For output frequencies less than 50 MHz, the output source current is typically 4.0 mA and the sink current is 6.0 mA. When the output frequency is higher than 50 MHz, the output source and sink currents automatically increase to 6.0 mA and 8.0 mA respectively. This feature adjusts the output rise and fall times for different applications. In some cases, fast rise and fall times may cause excessive electromagnetic interference.

CH9203 Advantages and Compatibility

The pinout diagrams of Chrontel's CH920x-series are based on those of CH9201 and ICS1394. If a board was originally designed for CH9201 or ICS1394, only the following minor changes are required in the board layout to upgrade to CH9203:

1. Instead of using a separate oscillator for the VGA controller memory clock (MCLK), CH9203 provides the MCLK output at pin 2.

2. By connecting the CH9203 AVDD directly to the 5V supply, the zener diode necessary for CH9201 and ICS1394 designs is eliminated and further power consumption is reduced.

3. MC0 – MC1 jumpers may be required for proper MCLK frequency selection. The MCLK frequency defaults to 60 MHz if MC0-MC1 are left open (internal pull-up).

4. Two 0.1 µF capacitors are needed: one between pins 11 and 12 for the memory loop filter, and the other between pins 16 and 12 for the video loop filter.

5. WREN*, SDATA and SCLK can be used to serially program CH9203.

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Table 2 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
VDD	Power supply voltage with respect to GND	−0.5 to +7.0	V
VIN	Input voltage on any pins with respect to GND	−0.5 to VDD +0.5	V
TSTOR	Storage temperature	−55 to +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 3 • DC Specifications (Operating Conditions: $T_A = 0°C - 70°C$, $V_{DD} = 5V \pm 5\%$)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 4.75V, IOH = 4mA	2.4			V
VOL	Output low voltage	VDD = 4.75V, IOL = 8mA			0.4	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current			5	20	μA
ILK	Input leakage current		−10		10	μA
ISTBY	Standby current	PD* = low		1	10	μA
IDD	Operating current	VDD = 5V VCLK = 50MHz MCLK = 55MHz		45		mA

Table 4 • AC Specifications (Operating Conditions: $T_A = 0°C - 70°C$, $V_{DD} = 5V \pm 5\%$)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
FIN	Crystal / FREF input			14.318		MHz
VCLK	Video clock frequency		8		130	MHz *
MCLK	Memory clock frequency		8		130	MHz *
TR	Output clock rise time	CL = 25pF, VOL − VOH		2		ns
TF	Output clock fall time	CL = 25pF, VOL − VOH		2		ns
TDC	Output clock duty cycle	VDD = 5V @VDD / 2	40	50	60	%

Note: * Output levels are guaranteed up to 90 MHz. Please consult Chrontel for suggested circuit implementations for frequencies higher than 90 MHz.

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Serial Interface Specifications

The serial interface requires a 19-bit data stream containing coefficients for the three programmable counters in each PLL synthesizer and three control signals.

1. A 1-bit control signal (S) to select either the VCLK or the MCLK registers

2. A 1-bit control signal (T) for factory use only, should be set to zero for normal operations

3. An 8-bit binary value (N) for the feedback frequency divider

4. A 1-bit control signal (D) to select output driving capability

5. A 2-bit value (K) for the output divider

6. A 6-bit binary value (M) for the reference frequency divider

7. The formula for calculating the output frequency is achieved by:

$$F_{OUT} = F_{REF} \times \frac{n}{m \times k}$$

where:
$F_{REF} = 14.318$ MHz (for normal operation)
$m = M + 2$
$n = N + 8$
$k = 2^K$

Note: There are restrictions in determining the values of M, N, and K. M cannot be 0.
The following values are not valid for N: 0-7, 9-15, 18-23, 27-31, 36-39, 45-47, 54, 55, 63.

Bit Definitions

Bit 18-13 A 6-bit reference frequency divider (M) where B18 = MSB, B13 = LSB

Bit 12-11 A 2-bit output divider (K)

B12	B11	Definition
0	0	No divide (divide by 1)
0	1	Divide by 2
1	0	Divide by 4
1	1	Divide by 8

Bit 10   Output current drive (D)   0 : high sink and source current capabilities
                                            1 : low sink and source current capabilities

Bits 9-2   An 8-bit feedback counter (N)   B9 = MSB and B2 = LSB

Bit 1   (T) should be always set to zero

Bit 0   Programming register select (S) 0 : Video clock programming register
                                             1 : Memory clock programming register

18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
M	M	M	M	M	M	K	K	D	N	N	N	N	N	N	N	N	T	S

→ Bit 00 is the first bit to be shifted in.

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Table 5 • Serial Interface Timing

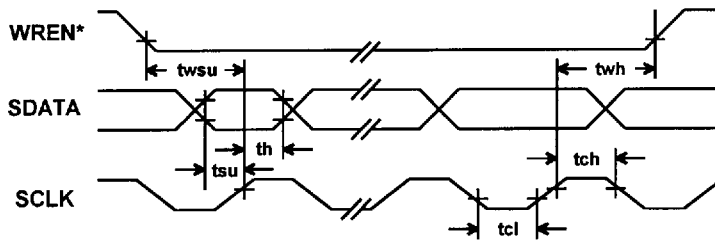| Symbol	Description	Min	Typ	Max	Unit
tsu	Serial data setup time	20			ns
th	Serial data hold time	20			ns
twsu	Write enable setup time	30			ns
twh	Write enable hold time	30			ns
tcl	SCLK low pulse width	20			ns
tch	SCLK high pulse width	20			ns

Figure 3: Serial Interface Timing Diagram
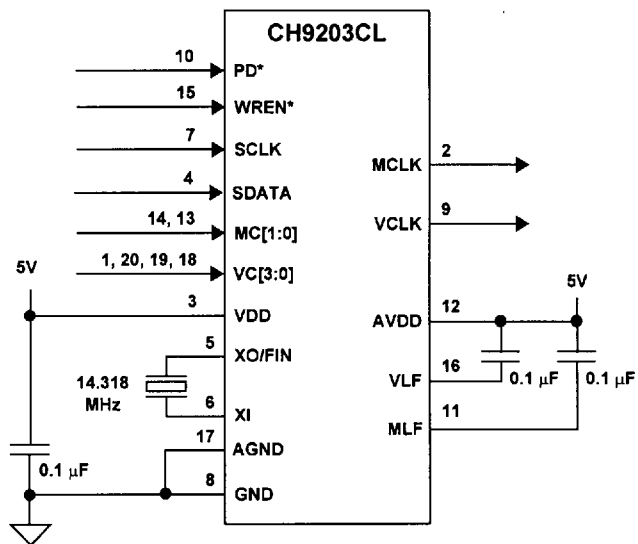
Figure 4: Application Schematic

ORDERING INFORMATION

Part number	Package type	Number of pins	Voltage supply
CH9203CL-NC	300 mil PDIP	20	5V
CH9203CL-SC	300 mil SOIC	20	5V

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