CIRRUS LOGIC

CL-GD610/620-C

Data Sheet

T-52-33-45

Flat Panel/CRT Enhanced VGA Controller

FEATURES

- Supports dual-scan and single-scan LCD panels
- Supports gas plasma and EL panels
- High-quality display on LCD panels at low frequencies
- Hardware-compatible with VGA, EGA, CGA, MDA, and HGC standards
- Automatic hardware mapping of 256 colors into 64 grayshades (AutoMap™)
- Intelligent power management for low power consumption
- 8 x 19-resolution programmable text characters on flat panels
- Blinking hardware cursor
- 8- or 16-bit PC bus interface
- Horizontal compression and vertical expansion in hardware
- Supports two 64K x 16 DRAMs for video memory
- Advanced, low-power CMOS technology

OVERVIEW

The CL-GD610/620-C flat panel VGA controller, an enhanced version of the widely used CL-GD610/620-B flat panel VGA controller, provides the following features for notebook, laptop, and CRT PC displays:

— Superb display quality
— Low power consumption
— Small form factor
— Full compatibility
— High performance

An ideal choice for minimum-board-space or low-chip-count designs, the high-integration/low-power CL-GD610/620-C drives LCD, gas plasma, electroluminescent (EL) and CRT displays. The CL-GD610/620-C is fully hardware compatible with the

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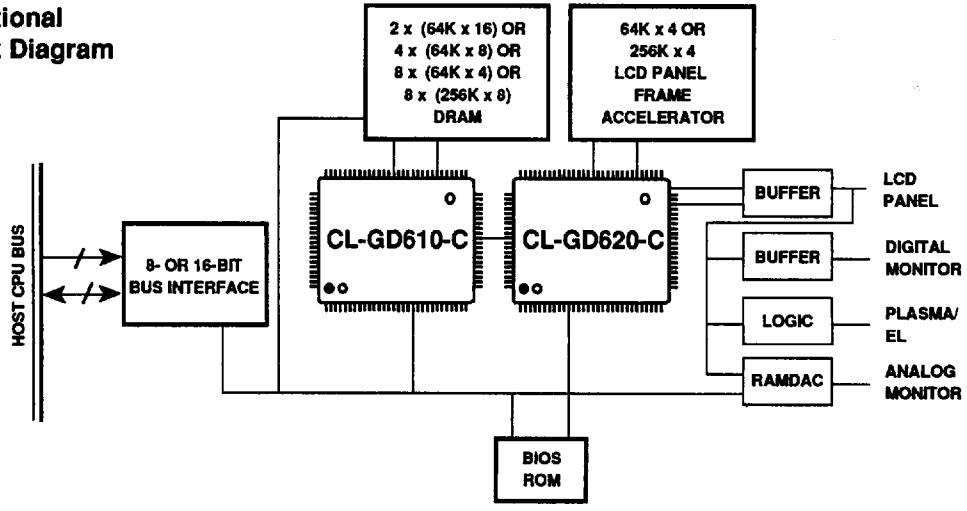
Functional Block Diagram



OVERVIEW (cont.)

IBM VGA, EGA, CGA, MDA, and HGC video standards, and a high-performance 8- or 16-bit bus interface is included. The VGA controller can also be used in overhead projection displays, desktop LCD systems, Point of Sale (POS) displays, industrial controls, and many other applications.

The CL-GD610/620-C eliminates flickering and stability problems normally associated with monochrome LCDs by using duty cycle modulation techniques that yield 16 solid grayscales. In addition, the Cirrus Logic AutoMap™ technique automatically (through hardware algorithms) maps 256 colors into 64 high-quality grayscales for CRT-quality grayscale emulation. The mapping of 256 colors into 64 grayscales is equivalent to the IBM VGA sum-to-gray feature when a monochrome analog VGA monitor is connected to the IBM VGA. The 64 grayshades are produced through a dithered pattern technique using the 16 solid grayscales. The automatic color-mapping is completely transparent and requires no user modifications. These techniques permit some LCD displays that can only display 4 or 8 grayscales to display 16 or 64 grayshades. Foreground/background color attributes are automatically remapped for maximum contrast in text modes. Hardware Expanded Text and Graphics modes provide larger character fonts and the ability to fill a panel (via scanline replication) even in low-resolution video modes, and are transparent to the application software. If expanded modes are not used, automatic screen centering is performed. 720-pixel-wide modes can be displayed on a 640-pixel-wide panel through either of two width compression options or a panning option.

Operating at dot clock rates up to 32 MHz, the CL-GD610/620-C controller supports high-resolution color or monochrome graphics and text modes on standard analog VGA monitors or many popular variable-frequency monitors. Refresh rates for flat panels range from 60 Hz to 160 Hz, and can be selected to match particular panel requirements. Cirrus Logic proprietary technology provides maximum contrast, reduced flicker, and lower power consumption with LCD panels while using a 24 MHz (or lower) dot clock (28 MHz for gas plasma and EL panels).

Video outputs to CRT displays are provided at 4 bits per pixel in all resolutions, and 8 bits per pixel in all IBM VGA 256-color modes. Using an analog video output and a standard external palette (INMOS 171-compatible RAMDAC), selections can be made from a palette of 18 bits per pixel (262,144 colors).

Video outputs to LCD panels are provided in dual-panel format with 4 bits going to the top half of the display, and 4 bits going to the bottom half of the display in parallel, a technique made possible by a proprietary half-frame buffer technique (LCD panels may also be driven directly). High-resolution 1024 x 768 and 1100 x 780 dual-panel LCDs are also supported by use of additional video memory (typically eight 256K x 4 DRAMs).

Gas plasma and EL panels are driven by CRT video signals. Panels that support 16 grayshades can use the AutoMap feature of 256K colors mapped into 64 grayshades. In addition, gas plasma and EL panels can use the same expansion/compression/panning features that the CL-GD610/620-C provides for LCD panels.

The CL-GD610/620-C has intelligent power management features in hardware that allow low power consumption even in normal operating modes, and very low or no power consumption in several power-reduction modes.

The CL-GD610/620-C is designed for systems requiring a small form factor such as notebook and laptop PCs. A minimum design (8-bit, E000 Planar BIOS, two 64K x 16 DRAMs) would include as few as 13 ICs without the use of any PALs, and can require as little as 5 to 6 square inches of board space. To permit flexibility, two 64K x 16 DRAMs, four 64K x 8 DRAMs, eight 64K x 4 DRAMs, or several other types of memories can be used to best suit your system needs.

The CL-GD610/620-C implements in hardware all control and data registers in the VGA, EGA, CGA, MDA, and HGC video standards, including those of the 6845 CRT Controller. Flexible register write protect control, and the ability to save/restore all registers, are both key elements enabling the controller to be used in a variety of operating systems

ADVANTAGES

Unique Features	Benefits
■ *Provides a superior-quality display*	❒ Higher definition, easier to read.
■ *8 x 19 programmable fonts*	❒ Large, easy-to-read text.
■ *64 shades of gray*	❒ Superb shading, monochrome-VGA-CRT-quality on LCDs.
■ *Screen width compression*	❒ Displays entire Hercules® screens.
■ *Uses low frequencies during normal operation*	❒ Extends battery operation, less heat.
■ *Intelligent power management*	❒ Extends battery operation.
■ *Support for 64K x 16 DRAM*	❒ Uses less space, ideal for notebook PCs.
■ *100% VGA-compatible*	❒ Runs all new software.
■ *100% HGC-, MDA-, CGA-, and EGA-compatible*	❒ Runs all existing software on CRTs and LCDs.
■ *1:1 CPU-to-Video Memory Interleave*	❒ Better performance on benchmark tests.
■ *Blinking hardware cursor*	❒ Easy to locate cursor on LCDs when running Microsoft® Windows™.
■ *BIOS available from both Cirrus Logic and Phoenix® Technology*	❒ Ensures availability and product differentiation.

OVERVIEW (cont.)

and application environments. When used with 640 x 480 8- or 16-grayscale LCD panels and VGA-compatible CRTs, all video standards (VGA, EGA, CGA, MDA, and HGC) are supported. When 640 x 480 16-grayshade gas plasma or EL panels are supported, full VGA compatibility is supported. Panels that are less than 640 x 480, or cannot display 16 grayshade, may not be suitable for displaying the supported video standards, but can still be used by limiting the controller to certain video modes or by use of non-standard video modes.

The sequencer design provides more video memory cycles for the CPU during the normal video refresh/display cycle. During display-blanked intervals, ALL memory cycles can be allocated to process CPU memory request. This gives a 1:1 CPU-to-Video Memory Interleave for high-performance VGA requirements. To provide additional performance, the intelligent 8-/16-bit Video Memory Interface detects memory map configurations that place adjacent bytes in adjacent memory locations and automatically configures the controller as a 16-bit peripheral. However, 16-bit operation may also be configured by program control.

The hardware supports a blinking mouse/graphics cursor and a blinking-insertion-point text cursor. When using application environments such as Microsoft Windows, a blinking cursor is an important aid in rapidly locating the cursor after it has been repositioned. Additional controls include blink disable and replace/invert mode control.

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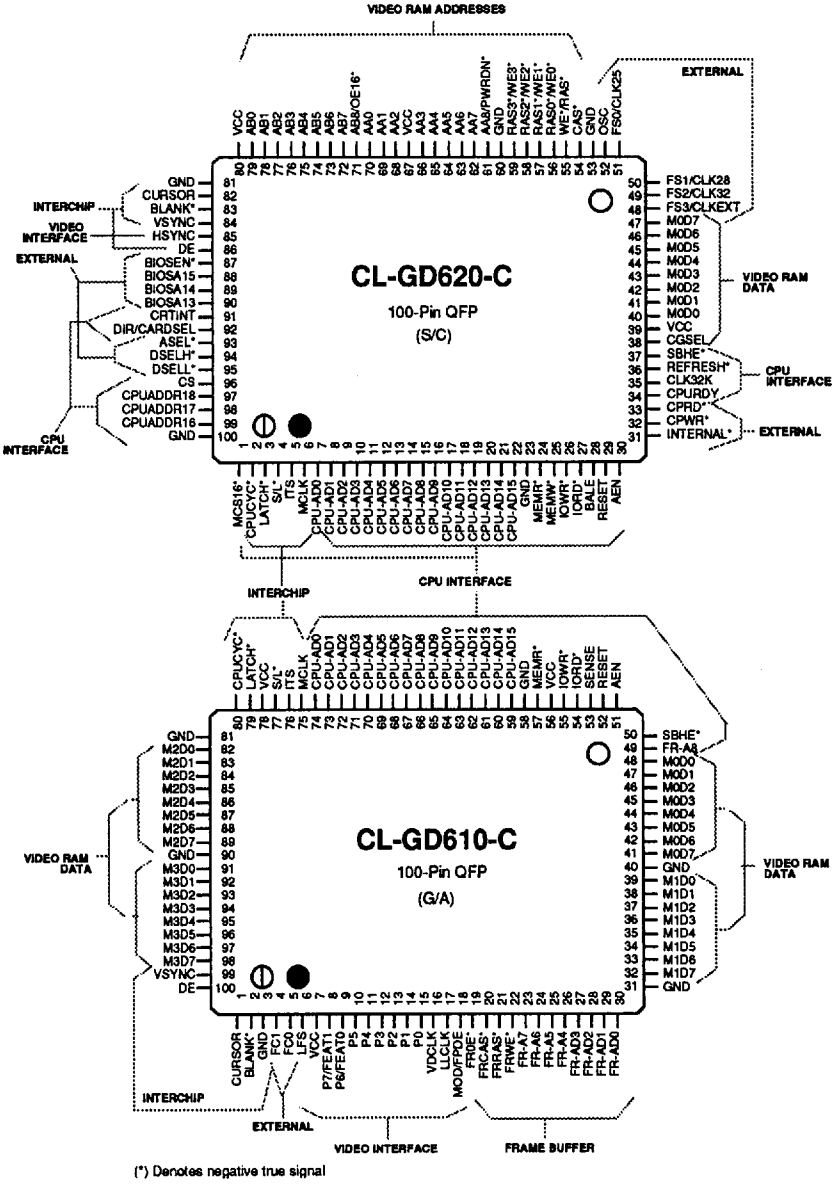
1. PIN INFORMATION

1.1 Pin Diagram



(*) Denotes negative true signal

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Figure 1–1. CL-GD610-C and CL-GD620-C Pin Diagram

1.2 Pin Assignment Table

Name	CL-GD610-C Pin No.	CL-GD620-C Pin No.	Type	Function
Processor Interface				
SBHE*	50	37	I-T	Bus High Enable from host CPU
AEN	51	30	I-T	DMA vs. non-DMA bus cycles)
RESET	52	29	I-T	System Reset
SENSE	53		I-T	Input from external logic to sense type of analog monitor
IORD*,IOWR*	54,55	27,26	I-T	I/O R/W Strobes
MEMR*,MEMW*	57	24,25	I-T	CPU Read/Write of Video Memory
CPU-AD [15:0]	59-74	7-22	I/O-T	Multiplexed CPU Address/Data/Switch Bus
CPUADDR [18:16]		97-99	I-T	Upper 3 address bits from host CPU
CS		96	I-T	Memory decode of LA[23:19]
DIR/CARDSEL*		92	O-T	Bidirectional CPU Data Bus Transceiver Control
CRTINT		91	OD	Display Retrace Interrupt
REFRESH*		36	I-T	System Refresh of Bus Attached RAM
CPURDY		34	OD	Data available signal for wait state logic
MCS16*		1	OD	16-bit peripheral access acknowledge
Video Memory Data Interface				
M0D[7:0]	41-48	47-40	I/O-T	Byte-wide bidirectional data bus to plane 0
M1D[7:0]	32-39		I/O-T	Byte-wide bidirectional data bus to plane 1
M2D[7:0]	82-89		I/O-T	Byte-wide bidirectional data bus to plane 2
M3D[7:0]	91-98		I/O-T	Byte-wide bidirectional data bus to plane 3
CGSEL (Attr Bit 3, M1D3)	38		I-T	Selects Alpha Map
Video Memory Address Interface				
CAS*		54	O-T	Column address strobe to all planes
WE*		55	O-T	Video Memory Write Enable
RAS[3:0]*/WE[3-0]*		56-59	O-T	Outputs either row Address Strobe or Write Enable Signal to DRAMs
AA[7:0], AA8/PO1*		61-66, 68-70	O-T	Address bus to byte planes 0 and 1. AA8 is either Address Bus Pin or Power-down Pin for clock generation and palette
AB[7:0],AB8/OE16*		71-79	O-T	Address bytes to planes 2 and 3. AB8 is either Address Bus Pin or Output Enable Pin for word-wide DRAMs
External Interface				
INTERNAL*		31	O-T	Selects internal vs. external video drivers; also can be used for Bt475-type palettes
CPWR*, CPRD*		32,33	O-T	Color Palette Write/Read
FS3/CLKEXT		48	I/O-T	Input from ext clock (feat. conn.) or clock select
FS2/CLK32,		49-51	I/O-T	Programmable pins, either clock select or clock FS1/ CLK28, inputs
FS0/CLK25				
OSC		52	I-T	Oscillator Input, MUST be connected to a clock
BIOSEN*		87	O-T	BIOS ROM Output Enable Select
BIOSA [15:13]		88-90	O-T	BIOS Page Select (for 27C512 devices)
ASEL*, DSELH*, DSELL*	93-95		O-T	Address and data select (low and high byte) enables

1.2 Pin Assignment Table *(cont.)*

Name	CL-GD610-C Pin No.	CL-GD620-C Pin No.	Type	Function
External Interface				
FC [1:0]	4,5		O-T	Programmable, normally used for power sequencing
CLK32K	35		I-T	Connects to 32 kHz clock; used in Suspend Mode as clock to refresh DRAMs
CL-GD610/620-C Interconnect				
CURSOR*	1	82	CL-GD620-C to CL-GD610-C	Cursor Valid Signal
BLANK*	2	83	CL-GD620-C to CL-GD610-C	Video Blanking Signal
ITS	76	5		CL-GD620-C to CL-GD610-C Interchip Timing Strobe
S/L*	77	4	CL-GD620-C to CL-GD610-C	Syncs loading shift registers with CRTC Character Clock
LATCH*	79	3	CL-GD620-C to CL-GD610-C	Latches video RAM data on CPU or CRT reads
CPUCYC*	80	2	CL-GD620-C to CL-GD610-C	Indicates CPU Read/Write Cycle to display memory
DE	100	86	CL-GD620-C to CL-GD610-C	Display Enable

Name	Pin No.	Type	Function	Analog	ECD	CD	MD	LCD
Video Interface								
LFS	6	O-C	LCD Frame Start					
P7/FEAT1	8	I/O-C	Pixel Data MSB/Feature Bit 1	P7				UD3
P6/FEAT0	9	I/O-C	Pixel Data 6/Feature Bit 0	P6				UD2
P5/SR	10	O-C	Pixel Data 5/Secondary Red	P5	SR			UD1
P4/SG/I	11	O-C	Pixel Data 4/Second. Green/Intens.	P4	SG	I	I	UD0
P3/SB/V	12	O-C	Pixel Data 3/Second. Blue/Video	P3	SB	V		LD3
P2/R	13	O-C	Pixel Data 2/Primary Red	P2	R	R		LD2
P1/G	14	O-C	Pixel Data 1/Primary Green	P1	G	G		LD1
P0/B	15	O-C	Pixel Data LSB/Primary Blue	P0	B	B		LD0
VDCLK	16	O-C	LCD Video Data Clock					
LLCLK	17	O-C	LCD Line Clock					
MOD/FPDE	18	O-C	LCD Modulation Output or display enable for gas plasma/EL flat panels					
HSYNC	85	O-T	Horizontal Sync Output					

Name	Pin No.	Pin No.	Type	Function
MCLK	75	6	CL-GD620-C to CL-GD610-C	Master Clock
VSYNC	99	84	CL-GD620-C to CL-GD610-C	Vertical Sync Signal
Frame-Accelerator Memory Address Interface				
FROE*	19		O-T	Frame-Accelerator Output Enable
FRCAS*	20		O-T	Frame-Accelerator CAS*
FRRAS*	21		O-T	Frame-Accelerator RAS*
FRWE*	22		O-T	Frame-Accelerator Write Enable
FR-A[8:4]	49,23-26		O-T	Upper 5 bits of Frame-Accelerator Address
FR-AD[3:0]	27-30		I/O-T	Multiplexed Frame-Accelerator Address/Data

NOTE: Under the TYPE column, T — TTL pad, C — CMOS pad, OD — Open Drain.

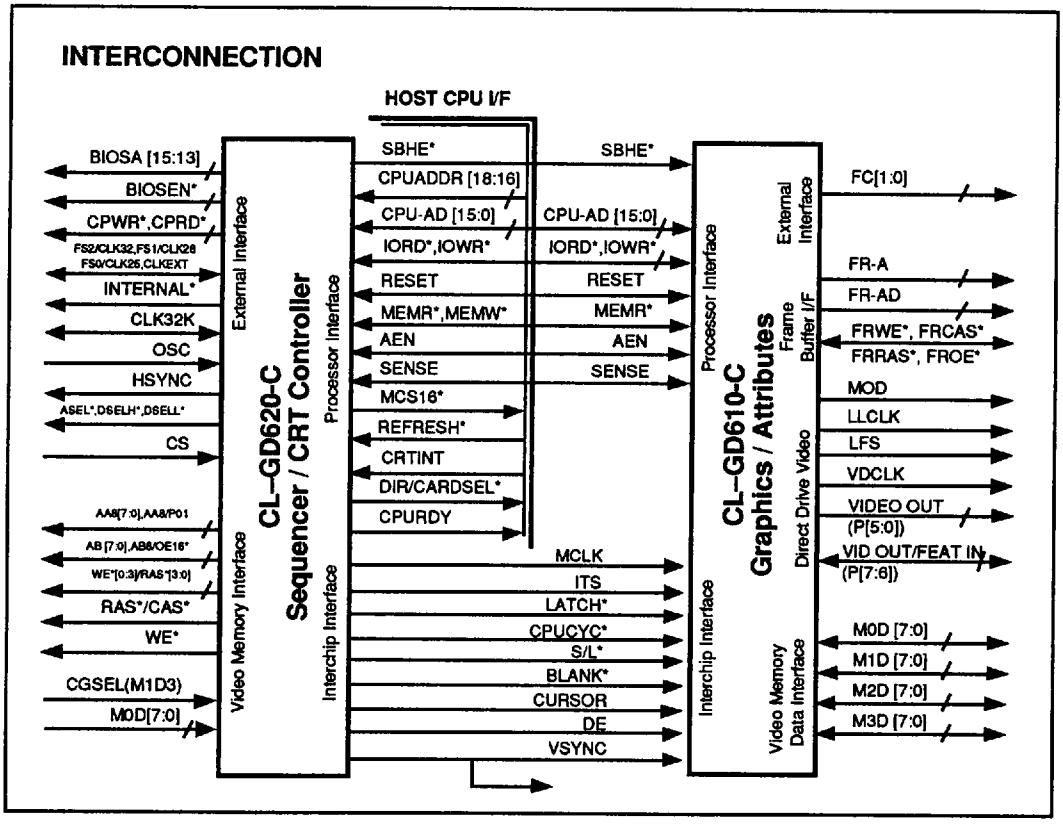

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Figure 1–2. CL-GD610/620-C Interconnection

2. DETAILED SIGNAL DESCRIPTION

2.1 Processor Interface

Name	CL-GD610-C	CL-GD620-C	Description
SBHE*	I	I	Host CPU System Byte High Enable. This signal is sampled only if 16-bit Mode is enabled (3C5 Index C7:0), otherwise 8-bit bus operations are assumed. 16-bit Mode is only for video memory access. I/O port accesses are always 8-bit.
CPUADDR [18:16]		I	The CL-GD620-C uses three upper address bits from the host CPU along with CPUAD [15:0] for address decoding.
CPU-AD[15:0]	I/O	I/O	Multiplexed Address and (bidirectional) data bus between the CPU and the chipset for Video RAM addresses, I/O register addresses and data.
CS		I	Input Pin. When high, indicates CPU access to lower 1 Mbyte memory. It is used internally by the CL-GD620-C to validate accesses.
CPURDY		O	Output signal used to synchronize CPU accesses to video memory. Normally, in the absence of any video memory access, this signal is at tristate. As soon as a video memory access is detected, it goes low. When the CL-GD620-C internal arbiter has given the CPU access to video memory and the read/write at the desired location is done, CPURDY goes high. After the system deasserts the MEMR* or MEMW* Signal, CPURDY returns to the tristate level. The timing for this signal is a function of CRT-CPU interleave and clock frequency.
CRTINT		O	Output signal to the CPU to indicate the start of a vertical retrace, normally connected to one of the interrupt inputs on the PC bus It is enabled by clearing Bit 5 of the Vertical Retrace End Register and cleared by resetting Bit 4 of the Vertical Retrace End Register. When enabled, the CRTINT Pin will go high at the start of the vertical retrace interval and remain high until cleared by a write of '0' to Bit 4 of the Vertical Retrace End Register (CR11). CRTINT is enabled by: • Clearing Bit 5 of CR11 • Setting Bit 4 of CR11

2.1 Processor Interface *(cont.)*

Name	CL-GD610-C	CL-GD620-C	Description
CRTINT *(cont.)*		O	If Bit 4 is not reset to a '1' after clearing the initial CRTINT, interrupts will cease. The CR11 of the CL-GD620-C is also readable at ER91. This feature greatly simplifies the task of ORing in the proper value for the remaining bits of the CR11 Register (this is not the case for an IBM-EGA or VGA controller). This Display Retrace Interrupt may be programmed for the AT Bus, or a direct interrupt controller interface. The interrupt polarity is controlled by ER80[5].
DIR		O	Controls the direction of the data buffer on the CPU-chipset data bus interface. DIR is driven low on I/O or memory read cycles performed by the CPU.
IORD*, IOWR*	I	I	When low, these signals indicate that an IORD* or IOWR* Cycle is taking place. The CL-GD610/620-C will respond only if CS is also active and the proper I/O port addresses have been decoded internally, and if not in the Sleep Mode.
RESET	I	I	This input is normally connected to the System Reset Bus Signal and is used as a hardware reset of the CL-GD610/620-C chips. The CL-GD620-C may be partially reset via software by clearing SR0-Bit 0 or 1. The falling edge of RESET* latches the data bus into switch registers to control S/W selectable functions. Two pins, CPU-AD15, 14 control H/W options.
REFRESH*		I	Indicates host system refresh of bus attached main memory and will cause the CL-GD620-C to ignore memory addresses on the bus.
AEN		I	Host CPU Bus Signal that distinguishes between DMA and non-DMA bus cycles. The signal is high for a DMA Cycle. Also will cause the CL-GD610/620-C to ignore IORD* and IOWR*.
BALE		I	Host CPU Bus Buffered Address Latch Enable Signal. High indicates a valid memory address.
MCS16*		O	This output is an acknowledge for 16-bit-wide accesses and is generated by the CL-GD620-C only if the 16-bit Peripheral Mode is enabled and a valid memory address range has been decoded. It may be generated by a full internal decode (LA16:23, SA15:14), a partial internal decode (without SA15) or with external decoding for fastest response time.

2.1 Processor Interface *(cont.)*

Name	CL-GD610-C	CL-GD620-C	Description
MEMR*	I	I	Video Memory Read Strobe. This input is driven low on all CPU memory read accesses. It decodes this operation if a valid CPU Cycle is in progress, (CPUCYC* = 0) and a read is not occurring (MEMR* = 1).
MEMW*		I	Video Memory Write Strobe. This input is driven low on all CPU memory read/write accesses. Video memory will be written if the CL-GD610/620-C chipset internal address decoders determine that the partial decode of the MSB addresses of the CPU address bus lies in the AxxxxH or BxxxxH range. The CL-GD610-C is not connected to MEMW* Signal.

2.2 Video Memory Interface

Name	CL-GD610-C	CL-GD620-C	Description
AA [7:0]		O	Multiplexed Video Memory Address Bus A. This bus contains the row/column address information required by the DRAMs in the video memory for memory planes 0 and 1. The CL-GD610/620-C chipset may be programmed to support 64K x 4 or 256K x 4 DRAMs (256K bytes or 1 Mbyte total video memory). This bus carries different addresses than AB in text modes.
AA8/PWRDN*		O	Software-selected Output Pin Function. Generates address Bit 8 for multiplexed address plane A or PWRDN* Signal. PWRDN* can be used to shut off clock chip and external palette PWRDN* is controlled by ERC7[3] inverted on reset PWRDN* = high.
AB[7:0]		O	Multiplexed Video Memory Address Bus B. This bus contains the row/column address information required by the DRAMs in the video memory for memory planes 2 and 3. The CL-GD610/620-C chipset may be programmed to support 64K x 4 or 256K x 4 DRAMs (256K bytes or 1 Mbyte total video memory). This bus carries different addresses than AA in text modes.
AB8/OE16*		O	Software-selected Output Pin Function. This pin is either the AB8 address line to video DRAMs, or the Output Enable Signal for word-wide DRAMs. Behavior is defined by the state of ERA7, Bit 2. This pin is AB8 if ERA7[2] is programmed high.

2.2 Video Memory Interface *(cont.)*

Name	CL-GD610-C	CL-GD620-C	Description
CAS*		O	Video Memory DRAM Column Address Strobe. A low-going edge on this signal latches the column address (contained on the AA and AB address buses) into video memory.
CGSEL		I	Enabled by the Sequencer Character Map Select Register. This bit (normally connected to M1D3 of the attribute memory plane in Text Mode) can be used to access 1 of 8 secondary character sets (instead of the normal intensity function), to give a total of 512 active display characters from a total of 4096.
M3D [7:0]	I/O		This bidirectional video memory data bus is controlled by the CL-GD610-C for read/write operations into Video Memory Plane 3, which stores graphic data for Color Plane 3, and eight extra alternate fonts in text modes.
M2D [7:0]	I/O		This bidirectional video memory data bus is controlled by the CL-GD610-C for read/write operations into Video Memory Plane 2, which stores graphic data for Color Plane 2 or character generator font tables in text modes.
M1D [7:0]	I/O		Bidirectional video memory data bus controlled by CL-GD610-C for read/write operations into Video Memory Plane 1, which stores graphic data for Color Plane 1 or attribute codes in text modes.
M0D [7:0]	I/O	I	This bidirectional video memory data bus is controlled by the CL-GD610-C for read/write operations into Video Memory Plane 0, which stores graphic data for Color Plane 0 or character codes in text modes. The CL-GD620-C uses these character codes in Text Mode to produce the proper address on the memory AB Bus to access the character generator fonts.
RAS [3:0]*/WE[0:3]*		O	Functions as either DRAM Row Address Strobe or DRAM Write Enable Signal. Option is selected by Extension Register ERA7, Bit 2. When it is set to 0, pins output row address strobe, and when set to 1, Output Write Enable Signal.
WE*/RAS*		O	Dual-function Output Pin, function selected by ERA7[2]. When ERA7[2] = 0, WE* is generated. When low, this signal enables a Video Memory Write to the bank selected by the appropriate RAS* Signal(s). The actual write occurs on the falling edge of CAS*. 64K x 16 DRAMs operate with WE[0:3]*, having four write enables, one per plane, and one RAS*.

2.3 Video Interface

The Pixel Data bits drive the external palette or digital inputs of color or monochrome displays. When driving dual-line LCD panels, P4-P7 drive the upper panel data inputs, and P0-P3 drive the lower panel data inputs. The P0-P7 pins are described more fully in the following table:

Name	Description	Analog RAM DAC Interface	ECD 64-Color Digital	CD 16-Color Digital	MD Mono-chrome	LCD	CL-GD610
P7/FEAT1	Tertiary Red Feature Bit 1†	P7	0	0	0	UD3	OUTPUT INPUT
P6/FEAT0	Tertiary Green Feature Bit 0†	P6	0	0	0	UD2	OUTPUT INPUT
P5/SR	Secondary Red	P5	SR	I	Note	UD1	OUTPUT
P4/SG/I	Secondary Green/ Intensity	P4	SG	I	Note	UD0	OUTPUT
P3/SB/V	Secondary Blue/ Video	P3	SB	I	Note	LD3	OUTPUT
P2/R	Primary Red	P2	R	R	Note	LD2	OUTPUT
P1/G	Primary Green	P1	G	G	Note	LD1	OUTPUT
P0/B	Primary Blue	P0	B	B	Note	LD0	OUTPUT

† FEAT1 and FEAT0 (Feature Bits 1 and 0) are programmable as inputs to the FC Register (Feature Control), and can be read at Port Address 3CA.

NOTES:

1) In monochrome modes, video outputs are driven from CL-GD610-C Palette Registers 0, 7, 8, 15 as follows:

Intensity	Video	Palette Register Selected	Mode
0	0	0	Mono Text or HGC Graphics
0	1	7	Mono Text or HGC Graphics
1	0	8	Mono Text Only
1	1	15	Mono Text Only

Intensity = Text Mode attribute byte Bit 3
Video = normal output to the monochrome display

2) TTL CRT displays (ECD, CD, and MD) require video BIOS support. Most video BIOSes do not currently support these displays. Please check with your BIOS supplier to determine if these displays are supported.

2.3 Video Interface *(cont.)*

Name	CL-GD610-C	CL-GD620-C	Description
MOD/FPDE	O		Dual-function pin, dependent on ERD6[4]. If bit is zero, then pin outputs MOD Signal. Used to prevent DC polarization of LCD. MOD changes polarity at least once per frame period. Some panels generate randomized alternating signals derived from LLCLK to perform this function, and may not need this signal. Its pulse width is programmable. The period is twice the number of line clocks written to Register 3C5:D9. If ERD6[4] Bit 4 is one, this pin outputs Display Enable Signal for use by external logic.
LLCLK	O		The LCD Line Clock is used to latch column segment data into the Horizontal Shift registers.
VDCLK	O		VDCLK is the video shift clock in LCD Mode. In CRT Mode, 4 bits of data for the upper panel, and 4 bits of data for the lower panel are simultaneously latched by this signal; it is not used for two corresponding scanlines.
LFS	O		LCD Frame Start pulse that indicates the start of a new frame, resetting horizontal and vertical logic to the first nibble of the first (of top and bottom panel) scanline.
HSYNC		O	Horizontal Sync. The active polarity of this signal can be selected by Bit 6 of the Miscellaneous Output Register (I/O address 3C2Hex) or Bit 6 of the Timing Control Register (extension address 85H).
VSYNC	I	O	Vertical Sync. The active polarity of this signal can be selected by Bit 7 of the Miscellaneous Output Register (I/O address 3C2H) or Bit 7 of the Timing Control Register (extension address 85H).

2.4 External Interface

Name	CL-GD610-C	CL-GD620-C	Description
BIOSA[15:13]		O	These 3 pins select one of the five 8K byte pages mapped into the upper 8K byte of the 32K byte BIOS address space, allowing a 64K byte ROM to be used in this 32K byte space.
OSC		I	Oscillator input, which MUST be connected to a clock, typically the 14.318 MHz clock from the system bus on the output of a frequency generator chip.
FS0/CLK25, FS1/CLK28, FS2/CLK32, FS3/CLKEXT		I/O	These pins are configured as inputs or outputs based on the state of CPU-AD14 latched from the bus on the falling edge of RESET*. They may be driven from crystal oscillators to provide 32.514, 28.332, and 25.172 MHz inputs to the CL-GD620-C internal mux (a 16.257 MHz clock, when required, is internally generated). When configured as outputs, they provide select signals to an external PLL-based multifrequency synthesizer circuit. When AD14 is pulled up, these pins are outputs; when it is pulled down, these pins are inputs.
CPWR*, CPRD*		O	Color Palette Write/Read strobes. These pins are active when valid I/O reads or writes to port addresses xC6-xC9H are decoded.
FC[1:0]		O	General-purpose Programmable Output pins, normally used to drive the feature connector, can be used for power sequencing in laptop PC applications. These bits may be write-protected with WRC Bit 6.

	0	**1**
Power-down	0	0
LCD	1	0
CRT	0	1
reserved	1	1

INTERNAL*		O	Programmable Output Pin, normally driving tristate control pins of video drivers for internal or external (feature connector) video operation in CRT Mode. This disables the external driver in LCD Mode. MISC Reg Bit 4 controls this pin.
BIOSEN*		O	This signal is typically connected to a ROM BIOS OE* Input. It enables the BIOS ROM outputs if a memory address in the C0000H-CFFFFH range has been decoded and ROM Control Register Bit 7 is cleared. This pin will not activate if the BIOS resides on the 'CPU' side of the address/data muxes as indicated by a high state of CPU-AD15 latched from the bus during the falling edge of RESET.

2.4 External Interface *(cont.)*

Name	CL-GD610-C	CL-GD620-C	Description
ASEL*		O	When low, enables external address buffers on multiplexed CPU-AD<15:> lines.
DSELL*		O	When low, enables CPU data bus lower-byte buffers onto multiplexed data/address lines CPU AD<7:0> of chipset. Active some time after ASEL* goes high, and deasserted shortly after command is inactive. Exact behavior is a function of the state of CPUAD0 (address phase) and SBHE* Signal.
DSELH*		O	When low, enables CPU data bus upper-byte buffers onto multiplexed data/address lines CPU AD<15:8> of chipset. Active some time after ASEL* goes high, and deasserted shortly after command is inactive. Exact behavior is a function of state of CPUAD0 (address phase) and SBHE* Signal.
SENSE	I		The SENSE Input Pin is used for detecting the type of monitor.
CLK32		I	Low-frequency Clock Input used in Suspend Mode to refresh DRAMs and reduce power consumption.

2.5 CL-GD610/620-C Interconnect Signals

Name	CL-GD610-C	CL-GD620-C	Description
BLANK*		O	Used to convey valid display area information to the CL-GD610-C and the external palette, if analog monitors are used. When high, display on screen is enabled. When low, screen is blanked. See description of DE Signal for more information.
DE		O	When high, indicates valid data display area. Low during overscan or retrace. This signal is connected to CL-GD620-C and is activated a few clocks before actual retrace.
CPUCYC*	I	O	Active low during CPU access to Video Memory Read or Write cycles, this signal brackets the LATCH* Signal during a read operation. The CL-GD610-C also uses this signal to differentiate between CPU and CRT read cycles.
CURSOR*	I	O	Active during valid cursor position.
ITS	I	O	Interchip Timing Strobe. This signal is in a critical timing path. Loading on this pin and the S/L* Pin must be the same.

2.5 CL-GD610/620-C Interconnect Signals *(cont.)*

Name	CL-GD610-C	CL-GD620-C	Description
MCLK	I	O	Derived from the currently selected clock, this is the master clock used to produce all of the signals in the CL-GD610/620-C.
LATCH*	I	O	Latches data from the video RAM in the CL-GD610-C.
S/L*	I	O	Shift/Load. Synchronizes the loading of the shift registers in the CL-GD610-C. This signal is in a critical timing path. Loading on this pin and the ITS Pin must be the same.
VSYNC	I	O	See description under video interface.

2.6 LCD Display Frame-Accelerator Interface Signals

Name	CL-GD610-C	CL-GD620-C	Description
FR-A[8:4]	O		Upper five bits of Frame Buffer Address
FR-AD[3:0]	I/O		Multiplexed Frame Buffer Address/Data
FRWE*	O		Frame-Accelerator Write Enable
FROE*	O		Frame-Accelerator Output Enable
FRCAS*	O		Frame-Accelerator CAS*
FRRAS*	O		Frame-Accelerator RAS*

(*) Denotes negative true signal.

3. FUNCTIONAL DESCRIPTION

3.1 Functional Operation

The tightly coupled CL-GD610-C Graphics/Attribute chip and CL-GD620-C Sequencer/CRTC chip interface with the host processor, video memory, display device, and other external I/O.

The host interface may be either 8- or 16-bits-wide under program control; Register LCD-CNTL3 is provided to switch sizes. Video memory may be 256K bytes or 1 Mbyte of DRAM.

Flat-panel display devices supported will typically be 640 x 480-resolution LCD, gas plasma, or EL panels. However, different resolution displays can be used if the VGA BIOS is modified to support nonstandard panel resolutions. CRT displays supported are PS/2 VGA-compatible analog monitors (IBM models 8503, 8512, 8513, and 8514), variable frequency analog monitors (NEC MultiSync type), and standard TTL monitors (ECD, CD, MD). It is important to note that most VGA BIOS for the CL-GD610/620-C do not support TTL monitors; prior to starting a design requiring TTL support, check with your BIOS supplier.

The four major operations supported by the CL-GD610/620-C are:

— Host Access to CL-GD610/620-C Registers
— Host Access to Video Memory
— Memory Refresh
— Display Access to Video Memory

Host Access to Registers

The host processor is typically an 8088/80286/80386/80486 processor in a PC/XT/AT bus-compatible environment and can access the CL-GD610/620-C registers by setting up a 24-bit address and generating IOR*/IOW*/MEMR*/MEMW* signals to read or write 8- or 16-bit data.

DRAM and screen refresh activities occur concurrently and independently unless the display parameters are being changed by the host CPU actions on the CL-GD610/620-C registers.

The registers that may be accessed by the host are listed in sections 5 and 6. They include the registers of the IBM VGA, EGA, CGA, MDA, and Hercules HGC as well as the 6845 CRT Controller. Non-VGA registers have also been made host-readable and writable in order to allow BIOS and driver software to determine the state of the video controller. The state must thus be readily switched and restored in multi-tasking and windowing environments. These extension registers provide the numerous enhancements to the basic VGA functions listed in the *Features/Benefits* section.

Host access to video memory is channeled via the CL-GD610/620-C controller. The host must set up the proper address/data/timing parameters in the CL-GD610/620-C registers, then handshake with the CL-GD610/620-C in order to connect the host data bus to one of four video memory byte plane buses. For example, consider VGA/EGA operation:

> Byte planes 0 and 1 share address bus A; planes 2 and 3 share address bus B. The CL-GD620-C Sequencer/CRTC chip takes 17-bit addresses from the host, and transforms them according to the selected Addressing Mode and Address Space Mapping, finally issuing multiplexed addresses to the different planes via the A and B address buses. The CAS* Signal, four RAS* signals, and WE* are also generated.

Note that the CL-GD620-C Sequencer/CRTC chip also contains an intelligent address sequencer that allocates video memory cycles not only to the host, as described above, but also to the DRAM refresh controller and the display CRT Controller.

Memory Refresh

Memory bandwidth is allocated to each process according to the actual real-time needs of the process, ensuring efficient use of the available bandwidth. In the case of a CRT display device, the display is blanked during horizontal and vertical retrace intervals, opening memory bandwidth for host access and/or memory refresh.

The CL-GD610/620, unlike early VGA implementations that gave the host only 14% of mem-

ory cycles, can give the host from 25-50% access to video memory (1 out of 2 memory cycles), largely due to the sequencing strategy.

Display Access to Video Memory

The CL-GD620-C Sequencer/CRT Controller chip works very closely with the CL-GD610-C Graphics/Attributes chip in all video modes, as the CL-GD610-C actually contains the video memory data interface as well as the video outputs to the display device. Thus the display data is latched in the CL-GD610-C after the CL-GD620-C determines where it is. Note that due to the 32-bit memory data interface, character data and attribute data can be pipelined. The CL-GD610-C contains the Video Shift registers to interface to the display device. The CL-GD620-C works with the CL-GD610-C in order to fetch scanline data from the font bitmaps, separately controlling the A and B address buses.

Foreground and background attributes are specified for each character in Alphanumeric Mode. Cursors and borders are also controlled by the CL-GD610-C in alpha modes.

In bit-mapped graphics (All Points Addressable) modes, pixel data is latched into the CL-GD610-C, transferred to shift registers, and shifted out upon translation through the color palette registers, which are also contained in the CL-GD610-C.

The CL-GD620-C supplies a clock (ITS) to the CL-GD610-C, as well as display Memory Read Strobe (LATCH*), CPU Read/ Write Cycle (CPUCYC*), and Shift Register Load (S/L*).

The CL-GD620-C keeps track of the active and unused areas of the screen and cursor positions and consequently supplies screen control signals (VSYNC, BLANK, Display Enable DE, and CURSOR) to the CL-GD610-C Graphics/ Attributes Chip.

When the CL-GD610/620-C interfaces with an LCD display, an additional 64K x 4 DRAM is needed. A Cirrus Logic proprietary Frame-Accelerator is used for split-panel data formatting. The reconstituted data from the Frame-Accelerator and the video memory is then supplied in parallel to the 4-bit upper and lower panel data buses of the LCD. This technique not only maintains normal display contrast, but also reduces the power consumption of the video circuitry, as the panel frame rate is double relative to the rate at which the data is fetched from video memory.

3.2 CRT Display Compatibility Modes

The CL-GD610/620-C includes all registers and data paths required for VGA/EGA, CGA, MDA, and HGC controllers. VGA enhancements to baseline EGA functionality include, a 320 x 200 8-bit/pixel Mode and support for an external color palette, 16 (double the IBM VGA capability) simultaneously loadable text fonts, Write Mode 3, and readable registers. These devices support new extended-resolution display modes with CRT displays.

Extended graphics resolutions beyond the 640 x 480 IBM VGA standard are available using either multiple-frequency monitors such as the NEC® MultiSync™ or Sony® MultiScan™. An 800 x 600 Mode with a 4:3 aspect ratio (the same as 640 x 480) requires a multifrequency display. High-resolution text modes offer from 100 columns by 30 rows up to 132 columns by 60 rows. 100 columns by 30 rows can be displayed on 640 x 480 flat panels.

Additional 256 color modes (besides IBM Mode 13) are available in the chipset and the Cirrus Logic BIOS supports these as well (RIX™ 360 x 480 Mode, etc.).

The CL-GD610/620-C also supports an Extended Mode 13 where 4 (256K bytes DRAM) or 16 (1 Mbyte DRAM) pages of 64K blocks of memory can be switched and displayed; IBM VGA handles only a single page. This allows for animation using 256 displayable colors without a large amount of data having to be manipulated (64K maximum size per image).

Apart from supporting byte-wide and nibble-wide DRAMs, the CL-GD610/620-C has a software-selectable feature that allows the interfacing of

word-wide DRAMs. Dual-function video memory interface pins automatically switch function to connect to 64K x 16 dynamic DRAM devices (requires VGA BIOS awareness). This brings two benefits to system designers: lower chip count and increased reliability.

3.3 Flat Panel Display Compatibility Modes

The CL-GD610/620-C will directly drive all of the popular dual panel/dual scan flat panels. Proprietary techniques minimize flicker, noise, and pattern motion while enhancing contrast within the grayshades being used.

Grayscaling is accomplished by modulating the ON-to-OFF time of individual pixels in the panel and allowing the eye to integrate the superposed pixels to 16 perceptible grayshades. Flicker is eliminated by proprietary techniques involving distribution of time between ON and OFF pixels during frame modulation.

The CL-GD610/620-C provides various mechanisms in order to allow the full spectrum of PC applications, written for various TTL and analog monitors, and various video modes, to run on standard 640 x 400 and 640 x 480 flat panels. These mechanisms include color emulation, attribute remapping, and resolution mapping.

In addition, summing circuitry allows rapid generation of IBM-compatible grayshade equivalents of color images. Up to 64 grayscale levels are available using algorithms similar to those used with IBM PS/2-monochrome CRT monitors, enhanced with proprietary two-dimensional stippling logic. This technique permits all applications that generate monochrome, 4,- 16-, or 256-color images to be run on a monochrome flat panel display.

Cirrus Logic's AutoMap logic is capable of mapping 256 colors into a monochrome image, which will appear in 64 shades. The hardware-based algorithm maintains independence of the particular palette map being used by calculating and storing (in real time) 6-bit grayshade values in an internal palette RAM that reflects all writes to the external RAMDAC. RAMDAC data may be stored as desired by the application in orderly sequences or in random sequences without affecting the consistently realistic renditions of color images.

In color text modes, foreground and background attributes can be automatically remapped to black and white for maximum contrast. Positive or negative raster may be selected under program control to match the visual qualities of the display and/or needs of the application. Bold characters are generated by using built-in intensified text fonts when the attribute calls for intensification.

The video resolutions that an application has selected are remapped to a flat panel according to whether Compatibility Mode, Compression Mode, or Expanded Mode was selected.

In Compatible Text Mode, the image is centered on the display with no change in the number of scanlines (200 line modes are double scanned to 400, however). 9-dot character fonts are replaced by 8-dot character fonts (HGC and VGA text) in order to fit within 640 columns. If alternate fonts from plane 3 are used, 9-dot fonts are no longer available. However, 9-dot fonts can be used with 720-pixel-wide panels

In Compatible Graphics Mode, the image is centered on the screen, with no change to the number of pixels displayed (except for double-scanning, 200 line CGA graphics modes). HGC images are 720 x 348, so panning with a 640-pixel-wide window may be performed to view the entire image.

Compression Mode allows the 720 horizontal pixels of an HGC-generated image to be displayed on a 640-pixel-wide display. Under program control, the 8th and 9th bit of each 9-bit word may be AND'ed or suppressed to generate the compressed bit. This compression provides very little degradation to text, and panning is always available if compressed graphics do not look satisfactory. All 720 pixels can be displayed on 720-pixel-wide panels.

Expansion Mode lets the display be filled in a symmetric and ratiometrically-determined fashion, and is available for both text and graphics video modes. In text modes, 9-dot characters are replaced by 8-dot characters, and character cell heights are expanded (from 8, 14, or 16 scanlines) to 19 scanlines. Thus 25 text-lines become 475 scanlines filling most of a 480-scanline panel. The filling algorithm was designed for a symmetric, pleasing expansion of the text, and automatically extends pixels used in character-based graphics applications to the cell boundaries.

3.4 Intelligent Power Management

Notebook and laptop PCs have stringent power limitations due to battery operation and heat dissipation. To meet these needs, the CL-GD610/620-C is manufactured using low-power CMOS technology. In addition, the CL-GD610/620-C has two programmable output pins as well as other intelligent power management features that will permit the controller to go into the following modes to conserve power:

Normal Mode

— Power to LCD panel and full screen refresh
— CPU access to video memory
— Refresh to video memory
— CPU access to RAMDAC
— CPU access to I/O registers

By use of a Frame-Accelerator the screen refresh can be at a maximum while the clock to the CL-GD610/620-C can be kept at a minimum of 24 MHz or less. This is important since power consumption is directly proportional to the frequency at which the controller is run. The Frame-Accelerator is used primarily with dual-scan LCD panels.

Standby Mode

— No power to LCD panel and no screen refresh
— CPU access to video memory
— Refresh to video memory
— CPU access to RAMDAC
— CPU access to I/O registers

The primary power savings in this mode are due to no power to the LCD panel. Since there is no screen refresh, normal clock rates are not required and may be replaced by slower clock rates to further reduce power consumption.

Suspend Mode

— No power to LCD Panel and no screen refresh
— No CPU access to video memory
— Refresh to video memory continues but using a very slow clock (32 kHz clock)
— No CPU access to RAMDAC
— No CPU access to I/O registers

The power savings in this mode (in addition to Standby Mode) are due to no CPU access to video memory and the use of a slow clock. This slow clock is used to refresh video memory, keeping CAS low and pulsing on RAS throughout the Suspend Mode. With slow-refresh DRAM, a clock running as slow as 32 kHz can be used. Standard DRAM requires a 64 kHz or faster clock. Other than this refresh logic, the rest of the CL-GD610/620-C does not have any clock, therefore reducing power consumption even further.

Death Mode

No power to video subsystem. Prior to entering this mode, the system saves the state of the video subsystem so it can be restored later. The CL-GD610/620-C allows the system to save or restore the status of all controller registers through the use of a Save/Restore Register.

4. VGA, EGA, CGA, AND HGC REGISTER PORT MEMORY MAP

Address	VGA/EGA Port	CGA Port	HGC Port
2B0/3B0	CRTC Index (R/W) (EGA Only)		6845 Index (R/W)
2B1/3B1	CRTC Data (R/W) (EGA Only)		6845 Data (R/W)
2B2/3B2	CRTC Index (R/W) (EGA Only)		6845 Index (R/W)
2B3/3B3	CRTC Data (R/W) (EGA Only)		6845 Data (R/W)
2B4/3B4	CRTC Index (R/W) (EGA Only)		6845 Index (R/W)
2B5/3B5	CRTC Data (R/W)		6845 Data (R/W)
2B6/3B6	CRTC Index (R/W) (EGA Only)		6845 Index (R/W)
2B7/3B7	CRTC Data (R/W) (EGA Only)		6845 Data (R/W)
2B8/3B8			Mode Control (R/W)
2B9/3B9			Set Light Pen Flip Flop (W)
2BA/3BA	Feature Control(W), Display Status(R)		Display Status (R)
2BB/3BB	Clear Light Pen Flip Flop (W)		Clear Light Pen Flip Flop (W)
2BC/3BC	Set Light Pen Flip Flop (W)		
2BD/3BD			
2BE/3BE			
2BF/3BF			Configuration (R/W)
2C0/3C0	Attribute Controller Index/Data (R/W)		
2C1/3C1	Attribute Controller Index/Data (R/W)		
2C2/3C2	Misc. Output (W), Feature (R)		
2C3/3C3	Misc. Output (W), Feature (R)		
2C4/3C4	Sequencer/Extensions Index (R/W)		
2C5/3C5	Sequencer/Extensions Data (R/W)		
2C6/3C6	Palette Pixel Mask (R/W)		
2C7/3C7	Palette Address Register R Mode (R/W)		
2C8/3C8	Palette Address Register W Mode (R/W)		
2C9/3C9	Palette Data (R/W)		
2CA/3CA	G. Pos. 2 (W) (EGA Only)		
2CB/3CB	(Reserved)		
2CC/3CC	G. Pos. 1(W)(EGA Only) Misc. Output (R)		

4.0 VGA, EGA, CGA, and HGC Register Port Memory Map *(cont.)*

Address	VGA/EGA Port	CGA Port	HGC Port
2CD/3CD	(Reserved)		
2CE/3CE	Graphics Controller Index (R/W)		
2CF/3CF	Graphics Controller Data (R/W)		
2D0/3D0	CRTC Index (R/W) (EGA Only)	6845 Index (R/W)	
2D1/3D1	CRTC Data (R/W) (EGA Only)	6845 Data (R/W)	
2D2/3D2	CRTC Index (R/W) (EGA Only)	6845 Index (R/W)	
2D3/3D3	CRTC Data (R/W) (EGA Only)	6845 Data (R/W)	
2D4/3D4	CRTC Index (R/W) (EGA Only)	6845 Index (R/W)	
2D5/3D5	CRTC Data (R/W)	6845 Data (R/W)	
2D6/3D6	CRTC Index (R/W) (EGA Only)	6845 Index (R/W)	
2D7/3D7	CRTC Data (R/W) (EGA Only)	6845 Data (R/W)	
2D8/3D8		Mode Control (R/W)	
2D9/3D9		Color Select (R/W)	
2DA/3DA	Feature Control(W), Display Status(R)	Display Status (R)	
2DB/3DB	Clear Light Pen Flip Flop (W)	Clear Light Pen Flip Flop (W)	
2DC/3DC	Set Light Pen Flip Flop (W)	Set Light Pen Flip Flop (W)	
2DD/3DD			
2DE/3DE			
2DF/3DF			

5. CGA, MDA, AND HGC REGISTERS

5.1 Color Graphics-Adapter- (CGA) Compatible Registers

Abbrev.	CGA Register Name	Bits	Reg. Type	R/W	Index	Port Address
MODE	Mode Control	7	CL-GD610/GD620-C‡	R/W	–	3D8
COLOR	Color Select	6	CL-GD610-C	R/W	–	3D9
STAT	Display Status	7	CL-GD610/GD620-C‡	R	–	3DA
CLPEN	Clear Light Pen Flip Flop	0	CL-GD620-C	W	–	3DB
SLPEN	Set Light Pen Flip Flop	0	CL-GD620-C	W	–	3DC
CRX	6845 Index	5	CL-GD620-C	R/W	–	3D4 (3D0,3D2,3D6)†
R0	Horizontal Total	8	CL-GD620-C	R/W	00	3D5 (3D1,3D3,3D7)†
R1	Horizontal Displayed	8	CL-GD620-C	R/W	01	3D5 (3D1,3D3,3D7)†
R2	Horizontal Sync Position	8	CL-GD620-C	R/W	02	3D5 (3D1,3D3,3D7)†
R3	Sync Width	4+4††	CL-GD620-C	R/W	03	3D5 (3D1,3D3,3D7)†
R4	Vertical Total	7	CL-GD620-C	R/W	04	3D5 (3D1,3D3,3D7)†
R5	Vertical Total Adjust	5	CL-GD620-C	R/W	05	3D5 (3D1,3D3,3D7)†
R6	Vertical Displayed	7	CL-GD620-C	R/W	06	3D5 (3D1,3D3,3D7)†
R7	Vertical Sync Position	7	CL-GD620-C	R/W	07	3D5 (3D1,3D3,3D7)†
R8	Interlace Mode	2	CL-GD620-C	R/W	08	3D5 (3D1,3D3,3D7)†
R9	Character Cell Height	5	CL-GD620-C	R/W	09	3D5 (3D1,3D3,3D7)†
RA	Cursor Start	5+2††	CL-GD620-C	R/W	0A	3D5 (3D1,3D3,3D7)†
RB	Cursor End	5	CL-GD620-C	R/W	0B	3D5 (3D1,3D3,3D7)†
CRC	Start Address High	8	CL-GD620-C	R/W	0C	3D5 (3D1,3D3,3D7)†
CRD	Start Address Low	8	CL-GD620-C	R/W	0D	3D5 (3D1,3D3,3D7)†
CRE	Cursor Address High	8	CL-GD620-C	R/W	0E	3D5 (3D1,3D3,3D7)†
CRF	Cursor Address Low	8	CL-GD620-C	R/W	0F	3D5 (3D1,3D3,3D7)†
LPENH	Light Pen High	8	CL-GD620-C	R	10	3D5 (3D1,3D3,3D7)†
LPENL	Light Pen Low	8	CL-GD620-C	R	11	3D5 (3D1,3D3,3D7)†

‡ Physical readback chip is underlined for split/duplicated registers

† Valid alternate register addresses are presented in parentheses

†† Split-field registers are denoted by 'X+Y'

5.2 Monochrome Display-adapter- (MDA) and Hercules Graphics-adapter-(HGC) Compatible Registers

Abbrev.	MDA/HGC Register Name	Bits	Reg. Type	R/W	Index	Port Address
MODE	Mode Control	7	CL-GD610/GD620-C‡	R/W	--	3B8
STAT	Display Status	7	CL-GD610/GD620-C‡	R	--	3BA
CONFIG	Configuration	2	CL-GD610/GD620-C‡	R/W	--	3BF
CLPEN	Clear Light Pen Flip Flop	0	CL-GD620-C	W	--	3BB
SLPEN	Set Light Pen Flip Flop	0	CL-GD620-C	W	--	3B9
CRX	6845 Index	5	CL-GD620-C	R/W	--	3B4 (3B0,3B2,3B6)†
R0	Horizontal Total	8	CL-GD620-C	R/W	00	3B5 (3B1,3B3,3B7)†
R1	Horizontal Displayed	8	CL-GD620-C	R/W	01	3B5 (3B1,3B3,3B7)†
R2	Horizontal Sync Position	8	CL-GD620-C	R/W	02	3B5 (3B1,3B3,3B7)†
R3	Sync Width	4+4††	CL-GD620-C	R/W	03	3B5 (3B1,3B3,3B7)†
R4	Vertical Total	7	CL-GD620-C	R/W	04	3B5 (3B1,3B3,3B7)†
R5	Vertical Total Adjust	5	CL-GD620-C	R/W	05	3B5 (3B1,3B3,3B7)†
R6	Vertical Displayed	7	CL-GD620-C	R/W	06	3B5 (3B1,3B3,3B7)†
R7	Vertical Sync Position	7	CL-GD620-C	R/W	07	3B5 (3B1,3B3,3B7)†
R8	Interlace Mode	2	CL-GD620-C	R/W	08	3B5 (3B1,3B3,3B7)†
R9	Character Cell Height	5	CL-GD620-C	R/W	09	3B5 (3B1,3B3,3B7)†
RA	Cursor Start	5+2††	CL-GD620-C	R/W	0A	3B5 (3B1,3B3,3B7)†
RB	Cursor End	5	CL-GD620-C	R/W	0B	3B5 (3B1,3B3,3B7)†
CRC	Start Address High	8	CL-GD620-C	R/W	0C	3B5 (3B1,3B3,3B7)†
CRD	Start Address Low	8	CL-GD620-C	R/W	0D	3B5 (3B1,3B3,3B7)†
CRE	Cursor Address High	8	CL-GD620-C	R/W	0E	3B5 (3B1,3B3,3B7)†
CRF	Cursor Address Low	8	CL-GD620-C	R/W	0F	3B5 (3B1,3B3,3B7)†
LPENH	Light Pen High	8	CL-GD620-C	R	10	3B5 (3B1,3B3,3B7)†
LPENL	Light Pen Low	8	CL-GD620-C	R	11	3B5 (3B1,3B3,3B7)

‡ Physical readback chip is underlined for split/duplicated registers

† Valid alternate register addresses are presented in parentheses

†† Split-field registers are denoted by 'X+Y'

6. VGA/EGA REGISTERS

6.1 Video Graphics Array/Enhanced Graphics-Adapter-Compatible Register Table

Abbrev.	EGA Register Name	Bits	Reg. Type	R/W	Reg. Index	Mono Port	Color Port
MISC	Miscellaneous Output	8	CL-GD610/GD620-C‡	W	–	3C2	3C2
FEAT	Input Status 0 (Feature Read)	4	CL-GD610/GD620-C‡	R	–	3C2	3C2
STAT	Input Status 1 (Display Status)	7	CL-GD610/GD620-C‡	R	–	3BA	3DA
FC	Feature Control	3	CL-GD610	W	–	3BA	3DA
GPOS1/MISC	Graphics 1 Pos. (W), Misc. (R)	2,8	CL-GD610/GD620-C‡	R/W	–	3CC	3CC
GPOS2/FC	Graphics 2 Pos. (W), FeatCtrl. (R)	2,3	CL-GD610/GD610-C	R/W	–	3CA	3CA
GRX	Graphics Controller Index	4	CL-GD610-C	R/W	–	3CE	3CE
GR0	Set/Reset	4	CL-GD610-C	R/W	00	3CF	3CF
GR1	Enable Set/Reset	4	CL-GD610-C	R/W	01	3CF	3CF
GR2	Color Compare	4	CL-GD610-C	R/W	02	3CF	3CF
GR3	Data Rotate	5	CL-GD610-C	R/W	03	3CF	3CF
GR4	Read Map Select	3	CL-GD610-C	R/W	04	3CF	3CF
GR5	Mode	7	CL-GD610-C	R/W	05	3CF	3CF
GR6	Miscellaneous	4	CL-GD620-C	R/W	06	3CF	3CF
GR7	Color Don't Care	4	CL-GD610-C	R/W	07	3CF	3CF
GR8	Bit Mask	8	CL-GD610-C	R/W	08	3CF	3CF
ARX	Attribute Controller Index	6	CL-GD610/GD620-C‡	R/W	–	3C0	3C0
AR0-F	Color Palette Regs 0-15	8	CL-GD610-C	R/W	00-0F	3C0	3C0
AR10	Mode Control	7	CL-GD610-C	R/W	10	3C0	3C0
AR11	Overscan Color	8	CL-GD610-C	R/W	11	3C0	3C0
AR12	Color Plane Enable	6	CL-GD610-C	R/W	12	3C0	3C0
AR13	Horizontal Pixel Panning	4	CL-GD610-C	R/W	13	3C0	3C0
AR14	Color Select	4	CL-GD610-C	R/W	14	3C0	3C0
CLPEN	Clear Light Pen Flip Flop	0	CL-GD620-C	W	–	3BB	3DB
SLPEN	Set Light Pen Flip Flop	0	CL-GD620-C	W	–	3BC/3B9	3DC
SERX	Sequencer/Extension Reg. Index	7	CL-GD620-C	R/W	–	3C4	3C4
SR0	Reset	2	CL-GD620-C	R/W	00	3C5	3C5
SR1	Clocking Mode	6	CL-GD620-C	R/W	01	3C5	3C5
SR2	Plane Mask	4	CL-GD620-C	R/W	02	3C5	3C5
SR3	Character Map Select	6	CL-GD620-C	R/W	03	3C5	3C5
SR4	Memory Mode	3	CL-GD610/20	R/W	04	3C5	3C5
SR6	Extensions Control (see Ext. Table)	1	CL-GD610/GD620-C‡	R/W	06	3C5	3C5
SR7	Reset H. Character Counter	1	CL-GD620-C	W	07	3C5	3C5
CRX	CRTC Index	6/5	CL-GD620-C	R/W	–	3B4	3D4
CR0	Horizontal Total	8	CL-GD620-C	R/W	00	3B5	3D5
CR1	Horizontal Display End	8	CL-GD620-C	R/W	01	3B5	3D5
CR2	Horizontal Blanking Start	8	CL-GD620-C	R/W	02	3B5	3D5
CR3	Horizontal Blanking End	5+2+1††	CL-GD620-C	R/W	03	3B5	3D5
CR4	Horizontal Retrace Start	8	CL-GD620-C	R/W	04	3B5	3D5
CR5	Horizontal Retrace End	5+2+1††	CL-GD620-C	R/W	05	3B5	3D5
CR6	Vertical Total	8	CL-GD620-C	R/W	06	3B5	3D5
CR7	Overflow	8	CL-GD620-C	R/W	07	3B5	3D5
CR8	Screen A Preset Row Scan	7	CL-GD620-C	R/W	08	3B5	3D5
CR9	Character Cell Height	5+1+1+1	CL-GD620-C	R/W	09	3B5	3D5
CRA	Cursor Start	6	CL-GD620-C	R/W	0A	3B5	3D5
CRB	Cursor End	5+2††	CL-GD620-C	R/W	0B	3B5	3D5
CRC	Screen A Start Address High	8	CL-GD620-C	R/W	0C	3B5	3D5
CRD	Screen A Start Address Low	8	CL-GD620-C	R/W	0D	3B5	3D5

6.1 Video Graphics Array/Enhanced Graphics-Adapter-Compatible Register Table *(cont.)*

Abbrev.	EGA Register Name	Bits	Reg. Type	R/W	Reg. Index	Mono Port	Color Port
CRE	Cursor Location High	8	CL-GD620-C	R/W	0E	3B5	3D5
CRF	Cursor Location Low	8	CL-GD620-C	R/W	0F	3B5	3D5
LPENH	Light Pen High	8	CL-GD620-C	R	10	3B5	3D5
LPENL	Light Pen Low	8	CL-GD620-C	R	11	3B5	3D5
CR10	Vertical Retrace Start	8	CL-GD620-C	W	10	3B5	3D5
CR11	Vertical Retrace End	4+2+1+1††	CL-GD620-C	W	11	3B5	3D5
CR12	Vertical Display End	8	CL-GD620-C	R/W	12	3B5	3D5
CR13	Offset	8	CL-GD620-C	R/W	13	3B5	3D5
CR14	Underline Location	5+2††	CL-GD620-C	R/W	14	3B5	3D5
CR15	Vertical Blanking Start	8	CL-GD620-C	R/W	15	3B5	3D5
CR16	Vertical Blanking End	8	CL-GD620-C	R/W	16	3B5	3D5
CR17	CRT Mode Control	7	CL-GD620-C	R/W	17	3B5	3D5
CR18	Line Compare	8	CL-GD620-C	R/W	18	3B5	3D5
CR22	Readback CRT Latches	8	CL-GD610-C	R	22	3B5	3D5
CR24	Attribute Index Toggle	7	CL-GD610-C	R	24	3B5	3D5
CR26MSB	CRTC scrA str addr MSB	2	CL-GD620-C	R/W	26	3B5	3D5
CR27MSB	CRTC cursor addr MSB	2	CL-GD620-C	R/W	27	3B5	3D5
CR30-CR3F	Frame Blank	1	CL-GD620-C	W	3X	3B5	3D5

‡ Physical readback chip is underlined for split/duplicated registers

†† Split-field registers are denoted by 'X+Y' or 'X+Y+Z' or 'X+Y+Z+M'

6.2 Extension Register Table (CL-GD510A/520A-Compatible)

Abbrev.	Extension Register	Bits	Reg. Type	Read/ Write	Reg/ Index	Port Addr.
SERX	Sequencer Extensions Register Index	7	CL-GD610/GD620-C‡	R/W	–	3C4
SR6	Extension Control	1	CL-GD610/GD620-C‡	R/W	06	3C5
CR7F	Identification	8	CL-GD620-C	R	7F	3B5/3D5
MC1	Misc. Control 1	8	CL-GD620-C	R/W	80	3C5
GPOS1	Graphics 1 Position	2	CL-GD610-C	R/W	81	3C5
GPOS2	Graphics 2 Position	2	CL-GD610-C	R/W	82	3C5
ARX	Attribute Controller Index	7	CL-GD610-C	R/W	83	3C5
WRC	Write Control	8	CL-GD610/GD620-C‡	R/W	84	3C5
TC	Timing Control	7	CL-GD620-C	R/W	85	3C5
BWC	Bandwidth Control	6	CL-GD620-C	R/W	86	3C5
MC2	Misc. Control 2	8	CL-GD620-C	R/W	87	3C5
FONTC	CGA, HGC Font Control	4	CL-GD620-C	R/W	89	3C5
	-reserved-	0	–	–	8A	3C5
SBPR	Screen B Preset Row Scan	5	CL-GD620-C	R/W	8B	3C5
SBSH	Screen B Start Address High	8	CL-GD620-C	R/W	8C	3C5
SBSL	Screen B Start Address Low	8	CL-GD620-C	R/W	8D	3C5
GAVER	CL-GD610-C Version Code	8	CL-GD610-C	R	8E	3C5
SCVER	CL-GD620-C Version Code	8	CL-GD620-C	R	8F	3C5
CR10	Vertical Retrace Start	8	CL-GD620-C	R/W	90	3C5
CR11	Vertical Retrace End	8	CL-GD620-C	R/W	91	3C5
LPENH	Light Pen High	8	CL-GD620-C	R/W	92	3C5
LPENL	Light Pen Low	8	CL-GD620-C	R/W	93	3C5
PPAH	Pointer Pattern Address High	8	CL-GD620-C	R/W	94	3C5
CADJ	Cursor Height Adjust	6	CL-GD620-C	R/W	95	3C5
CW	Caret Width	8	CL-GD610-C	R/W	96	3C5
CH	Caret Height	8	CL-GD610-C	R/W	97	3C5
CXH	Caret Horizontal Position High	3	CL-GD610-C	R/W	98	3C5
CXL	Caret Horizontal Position Low	8	CL-GD610-C	R/W	99	3C5
CYH	Caret Vertical Position High	2	CL-GD610-C	R/W	9A	3C5
CYL	Caret Vertical Position Low	8	CL-GD610-C	R/W	9B	3C5
PXH	Pointer Horizontal Position High	3	CL-GD610-C	R/W	9C	3C5
PXL	Pointer Horizontal Position Low	8	CL-GD610-C	R/W	9D	3C5
PYH	Pointer Vertical Position High	2	CL-GD620-C	R/W	9E	3C5
PYL	Pointer Vertical Position Low	8	CL-GD620-C	R/W	9F	3C5
GRL0	Graphics Ctrlr Memory Latch 0	8	CL-GD610-C	R/W	A0	3C5
GRL1	Graphics Ctrlr Memory Latch 1	8	CL-GD610-C	R/W	A1	3C5
GRL2	Graphics Ctrlr Memory Latch 2	8	CL-GD610-C	R/W	A2	3C5
GRL3	Graphics Ctrlr Memory Latch 3	8	CL-GD610-C	R/W	A3	3C5
CLK	Clock Select	6	CL-GD610-C	R/W	A4	3C5
CURS	Cursor Attributes	8	CL-GD610/GD620-C‡	R/W	A5	3C5
ISS	Internal Switch Source	8	CL-GD610-C	R/W	A6	3C5
MISCNTL	State Switch Control	8	CL-GD610/GD620-C‡	R/W	A7	3C5
256 CPC	256 Color Page Control	4	CL-GD620-C	R/W	AD	3C5
STATE	Active Adapter State	7	CL-GD610/GD620-C‡	R/W	AF	3C5
SCR0-F	Scratch Register 0-F	8	CL-GD610-C	R/W	B0-BF	3C5

‡ Physical readback chip is underlined for split/duplicated registers

6.3 Added Extension Register Table (New to CL-GD610/620-C)

Abbrev.	Extension Register	Bits	Reg. Type	Read/ Write	Reg/ Index	Port Addr
–	Graphics Cursor Address	2	CL-GD620-C	–	–	–
CR26MSB	CRTC scrA strt addr highest	2	CL-GD620-C	R/W	26	3?5
CR27MSB	CRTC Cursor addr highest	2	CL-GD620-C	R/W	27	3?5
LCDCNTL1	LCD Control Register 1	8	CL-GD610/620-C	R/W	8A	3C5
CPURAR	CPU Read Access Register	8	CL-GD620-C	R/W	C0	3C5
CPUWAR	CPU Write Access Register	8	CL-GD620-C	R/W	C1	3C5
LCDCNTL2	LCD Control Register 2	8	CL-GD620-C	R/W	C2	3C5
SWITCHH	Switch Setting Register High	8	CL-GD620-C	R	C4	3C5
SWITCHL	Switch Setting Register Low	8	CL-GD620-C	R	C5	3C5
SBSHH	Screen B strt addr highest	2	CL-GD620-C	R/W	C6	3C5
LCDCNTL3	LCD Control Register 3	7	CL-GD610/620-C	R/W	C7	3C5
COLOFF	Column Offset	8+1	CL-GD610-C	R/W	D0-D4	3C5
PNLHDIS	Panel Horizontal Displayed	8+1	CL-GD610-C	R/W	D1-D4	3C5
ROWOFF	Row Offset	8+1	CL-GD610-C	R/W	D2-D4	3C5
PRSEGTOT	Panel Row Segment Total	8+1	CL-GD610-C	R/W	D3-D4	3C5
PNLCNTL1	Panel Control 1	8	CL-GD610-C	R/W	D4	3C5
PNLCNTL2	Panel Control 2	8	CL-GD610-C	R/W	D5	3C5
FONTC	Plane 3 Alt font enable	7	CL-GD610/620-C	R/W	89	3C5
GROFFSET	Grayshade Offset	8	CL-GD610-C	R/W	D6	3C5
LCDCNTL4	LCD Control Register 4	5	CL-GD610-C	R/W	D7	3C5
MOD	Modulation/AC inversion	8	CL-GD610-C	R/W	D9	3C5
FRMCOLOR	Frame Color	4	CL-GD610-C	R/W	DA	3C5
PNLCNTL3	Panel Control 3 (reserved)	3	CL-GD610-C	R/W	DB	3C5

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Ambient temperature under bias..... 0°C to 70°C

Storage temperature..... -65°C to 150°C

Voltage on any pin with respect to ground..... GND -0.5 to V_{CC} + 0.5 Volts

Operating power dissipation (per chip)..... 0.300 Watt

Standby power dissipation (per chip) ..... 0.020 Watt

Power supply voltage..... 7 Volts

Injection current (latch-up)..... 25 mA

Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

7.2 CL–GD610/620-C DC Characteristics

(V_{CC} = 5V ± 5%, TA = 0° to 70°C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions
CL-GD610-C					
V_{CC}	Power Supply Voltage	4.75	5.25	V	Normal Operation
V_{IL}	Input Low Voltage	0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{IHC}	Input High Voltage CMOS	3.0		V0	
V_{ILC}	Input Low Voltage CMOS		1.5	V	
V_{OHC}	Output High Voltage CMOS	4.0		V	I
V_{OLC}	Output Low Voltage CMOS		0.4	V	I
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA†
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 400 µA
I_{CC}	Operating Supply Current	40.0		mA	@ 32 MHz, 5V nominal
I_{CCpd}	Powerdown Mode Current		4	mA	@ 32 MHz, 5V nominal
I_L	Input Leakage	-10.0	10.0	µA	$0 < V_{IN} < V_{CC}$
C_{IN}	Input Capacitance		10.0	pF	
C_{OUT}	Output Capacitance		10.0	pF	

7.2 CL–GD610/620-C DC Characteristics *(cont.)*

Symbol	Parameter	MIN	MAX	Units	Conditions
CL-GD620-C					
V_{CC}	Power Supply Voltage	4.75	5.25	V	Normal Operation
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{IHC}	Input High Voltage CMOS	3.0		V	
V_{ILC}	Input Low Voltage CMOS		1.5	V	
V_{OHC}	Output High Voltage CMOS	4.0		V	I
V_{OLC}	Output Low Voltage CMOS		0.4	V	I
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA††
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 400 µA
I_{CC}	Operating Supply Current	40.0		mA	@ 32 MHz, 5V nominal
I_{CCpd}	Powerdown Mode Current		4	mA	@ 32 MHz, 5V nominal
I_L	Input Leakage	-10.0	10.0	µA	$0 < V_{IN} < V_{CC}$
C_{IN}	Input Capacitance		10.0	pF	
C_{OUT}	Output Capacitance		10.0	pF	

†† I_{OL} MAX for CL-GD620-C = 12 mA for CPURDY, CRTINT, = 8 mA for DIR/CRDSEL*, WE*, CAS*.

7.3 AC Characteristics/Timing Information

The following timing information assumes that all outputs will drive one Schottky TTL load in parallel with 50 pF and all inputs are at TTL level. The MIN and MAX timings are those conforming to the operating ranges of a power supply voltage of 5V ± 5% and an ambient temperature of 0°C to 70°C.

7.3.1 DRAM Memory Performance Table

Dram Access Time (ns)	Dot Clock Freq. (MHz)	Memory Bandwidth CPU:CRT Cycle Interleave
80	25	
100	20	1:1, 1:2
120	16	
150	13	
80	33	
100	30	3:2‡
120	25	
150	20	
80	FcMax†	
100	33	1:4 8-dot character clock
120	25	
150	20	
80	FcMax†	
100	FcMax†	1:7 8-dot character clock
120	30	1:4 9-dot character clock
150	26	

† FcMax = Maximum CLKIN frequency = 1/Tc = 32 MHz

‡ Used when Dot Clock = Clock in/2

NOTE:

1 character clock is 8-dot clocks in graphics modes and either 8- or 9-dot clocks in text modes, depending upon the character width used.

7.3.2 Index of Characteristics/Timing Waveform Section

7.3.3 AC Timing Characteristics

This section provides the AC specification of the CL-GD610/620-C chipset.

General Notes:

Numbers in the **Notes** column on the following pages are correlated to remarks on this page.

1. The CL-GD610/620-C has an 8-bit I/O interface and a 16-bit memory interface.
2. For I/O read-write operations, the state of BHE is ignored and only CPUAD[7-0] lines are valid for address and data.

   The table below gives 8/16 bus cycle control details:

SBHE	A0	DSELL*	DSELH*	Operation
0	0	0	0	16-bit word
0	1	1	0	Odd byte
1	0	0	1	Even byte
1	1	X	0	8-bit mode, odd address

3. The chipset has a multiplexed address bus. The address is latched on the falling edge of command. However, where relevant from the host system perspective, limits are indicated.
4. Some parameters are functions of external system components and limits are given as a design guideline. These are for operations on CL-GD610/620-C.
5. Parameters marked EXT are dependent on external system components and are for operations in which the CL-GD610/620-C is involved.
6. Since ALE can be pulled up to + 5 volts, it is not indicated in the diagrams.
7. AEN has to be inactive, (low) for all chipset accesses.
8. In all timing diagrams, logic '1' is measured at 2.4V for TTL and 3.0V for CMOS. Logic '0' is measured at 0.8V for TTL and 0.4V for CMOS. Parameter values are with reference to these levels as applicable.
9. For the CL-GD610-C, Tc refers to tCLKIP(15), either MCLK or ITS. For the CL-GD620-C, Tc refers to tSCLKP (5).

Table 7–1. RESET Sequence Timing

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
t_{RPW} (1)	Reset Pulse Width	500			ns	
t_{RSLI} (2)	ASEL*, DSELL*, DSELH* high delay from RESET high		100		ns	
t_{RSLH} (3)	DSELL*, DSELH*, ASEL* inactive hold after RESET low	40			ns	
t_{HVLX} (4)	HSYNC, VSYNC, LLCLK, LFS do not care from RESET high			500	ns	a

a. Value given for guideline purposes only.

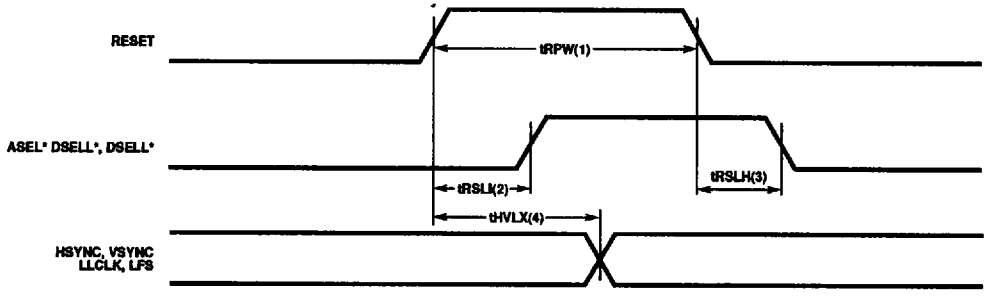

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Figure 7–1. RESET Sequence Timing

Table 7–2. MCLK, OSC, CLK28, CLK25, and CLK32 Specifications Table

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
I. CL-GD620-C Inputs from external clocks						
t_{SCLKP} (5)	System clock period	30(42)		(62.5)	ns	a, b
t_{SCLKL} (6)	System clock low width	Tc/2 - 5%		Tc/2 + 5%	ns	9
t_{SCLKH} (7)	System clock high width	Tc/2 - 5%		Tc/2 + 5%	ns	9
t_{SCLKF} (8)	System clock fall time			8	ns	
t_{SCLKR} (9)	System clock rise time			8	ns	
t_{CLKDLY} (19a)	Input clock to MCLK, ITS delay			20	ns	
II. CL-GD620-C outputs to CL-GD610-C						
t_{CLKOP} (10)	ITS/MCLK period	30(42)		(62.5)	ns	
t_{CLKOH} (11)	ITS/MCLK high width	Tc/2 - 5%		Tc/2 + 5%	ns	9
t_{CLKOL} (12)	ITS/MCLK low width	Tc/2 - 5%		Tc/2 + 5%	ns	9
t_{CLKOF} (13)	ITS/MCLK fall time			8	ns	
t_{CLKOR} (14)	ITS/MCLK rise time			8	ns	
III. CL-GD610-C Input clocks (from CL-GD620-C)						
t_{CLKIP} (15)	ITS/MCLK period	30(42)		(62.5)	ns	
t_{CLKIL} (16)	ITS/MCLK low width	Tc/2 - 5%		Tc/2 + 5%	ns	9
t_{CLKIH} (17)	ITS/MCLK high width	Tc/2 - 5%		Tc/2 + 5%	ns	9
t_{CLKIR} (18)	ITS/MCLK rise time			10	ns	
t_{CLKIF} (19)	ITS/MCLK fall time			10	ns	

a) SCLK, CLKO, and CLKI are terms used to indicate clock inputs to CL-GD620-C, clock output from CL-GD620-C and clock input to CL-GD610-C, respectively.

b) Values in brackets specify limits when LCD interface is active.

– Numbers in the **Notes** column are correlated to remarks in section 7.3.3 under **General Notes**.

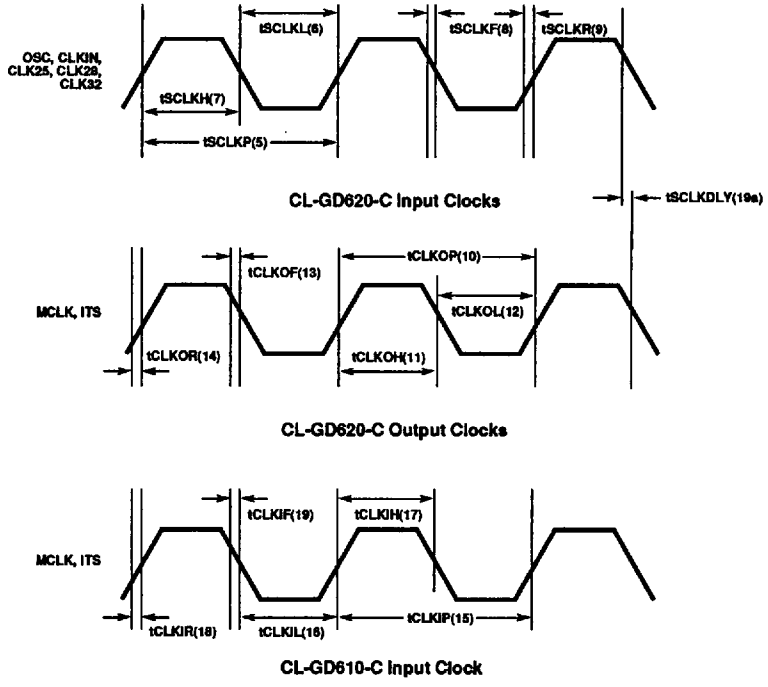

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Figure 7–2. CL-GD610/620-C Clocks

Table 7–3. I/O Write Cycle

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
$t_{IOWP\ (20)}$	I/O Write Pulse Width	150			ns	1,2
$t_{ASW\ (21)}$	Address setup to IOWR* low	20			ns	
$t_{AHW\ (22)}$	Address hold after IOWR* high	0			ns	3
$t_{AHWI\ (22a)}$	Address hold after IOWR* low	20			ns	
$t_{DSW\ (23)}$	Data setup to IOWR* high	60			ns	
$t_{DHW\ (24)}$	Data hold from IOWR* high	10			ns	
$t_{IOWRR\ (25)}$	IOWR* Recovery Time	80			ns	
$t_{ASHC\ (26)}$	ASEL* high after command low	20		30	ns	
$t_{ASLC\ (27)}$	ASEL* low after command high	30		55	ns	
$t_{DSLD\ (28)}$	DSELL*, DSELH* active delay from ASEL* high	8		15	ns	
$t_{DSHD\ (29)}$	DSELL*, DSELH* high 30 after IORD*, IOWR* inactive		55	ns		
$t_{ADLY\ (30)}$	CPUAD[7:0] delay from system address bus			20	ns	4
$t_{DDR(31)}$	Data drive delay from DSELL*/H* low			20	ns	3

NOTE:

– Numbers in the **Notes** column are correlated to remarks in section 7.3.3 under **General Notes**.

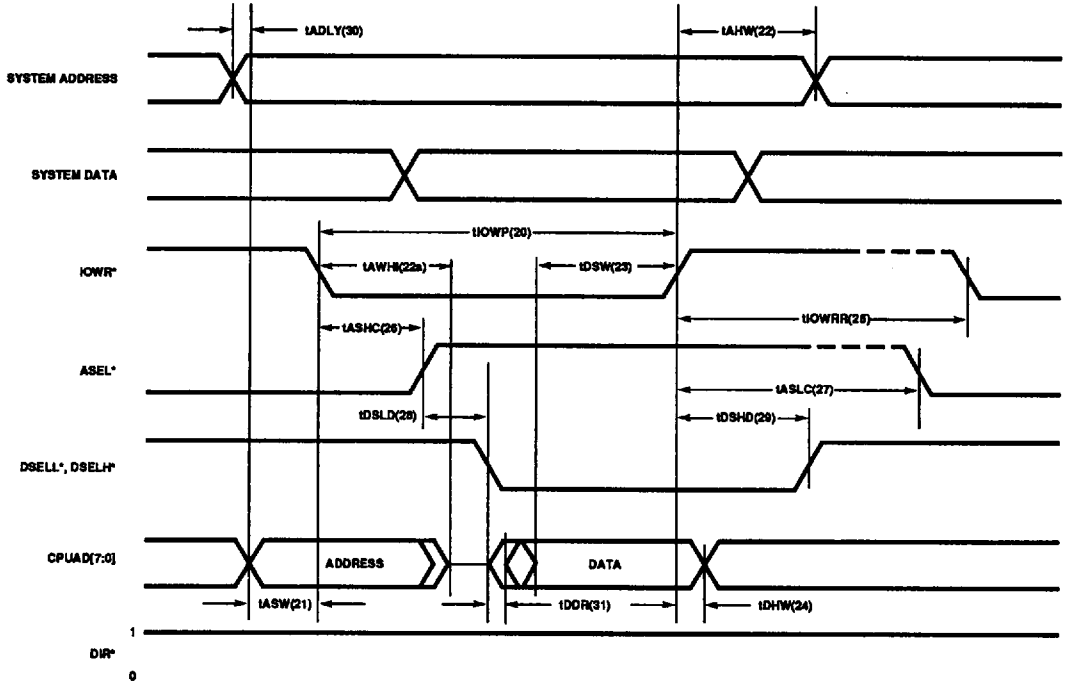

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Figure 7–3. I/O Write Cycle

Table 7–4. I/O Read Cycle

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
t_{IORP} (32)	I/O Read Pulse Width	150			ns	1,2
t_{ASRD} (33)	Address setup to IORD* low	20			ns	
t_{AHRD} (34)	Address hold from IORD* high	0			ns	3
t_{AHRI} (34a)	Address hold from IORD* low	20			ns	
t_{DVR} (35)	Data valid from IORD* low			100	ns	
t_{DHR} (36)	Data tristate after IORD* high			80	ns	
t_{IORR} (37)	IORD* Recovery Time	80			ns	
t_{ASHC} (26)	ASEL* high after IORD* low	20		30	ns	
t_{ASLC} (27)	ASEL* low after IORD* high	30		55	ns	
t_{DSLD} (28)	DSELL*, DSELH* active delay from ASEL* high	8		15	ns	
t_{DSHD} (29)	DSELL*, DSELH* high after IORD*, IOWR* inactive	30		55	ns	
t_{DLRWL} (38)	DIR/CARDSEL* low from IO/MEM read low			30	ns	
t_{DHRWH} (39)	DIRCARDSEL* high from IO/MEM read high			30	ns	
t_{ADLY} (30)	CPUAD[7:0] delay from system address bus			20	ns	4
t_{DDR} (31)	Data drive delay from DSELL*/H* low			20	ns	3

NOTE:

– Numbers in the **Notes** column are correlated to remarks in section 7.3.3 under **General Notes**.

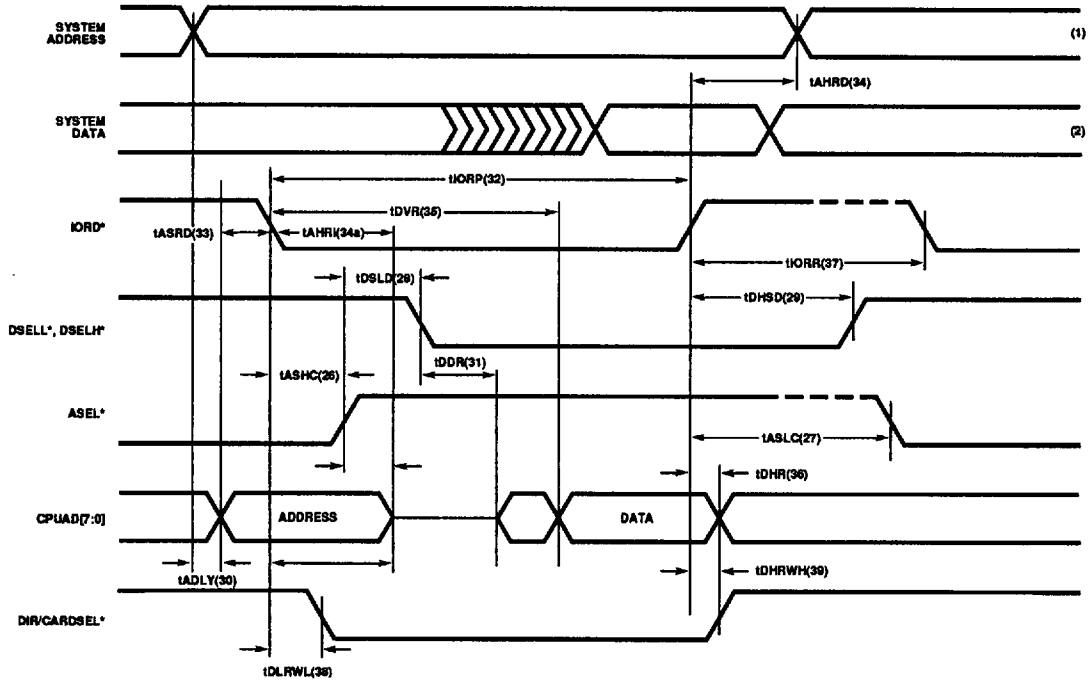

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Figure 7–4. I/O Read Cycle

Table 7–5. Color Palette Write Cycle

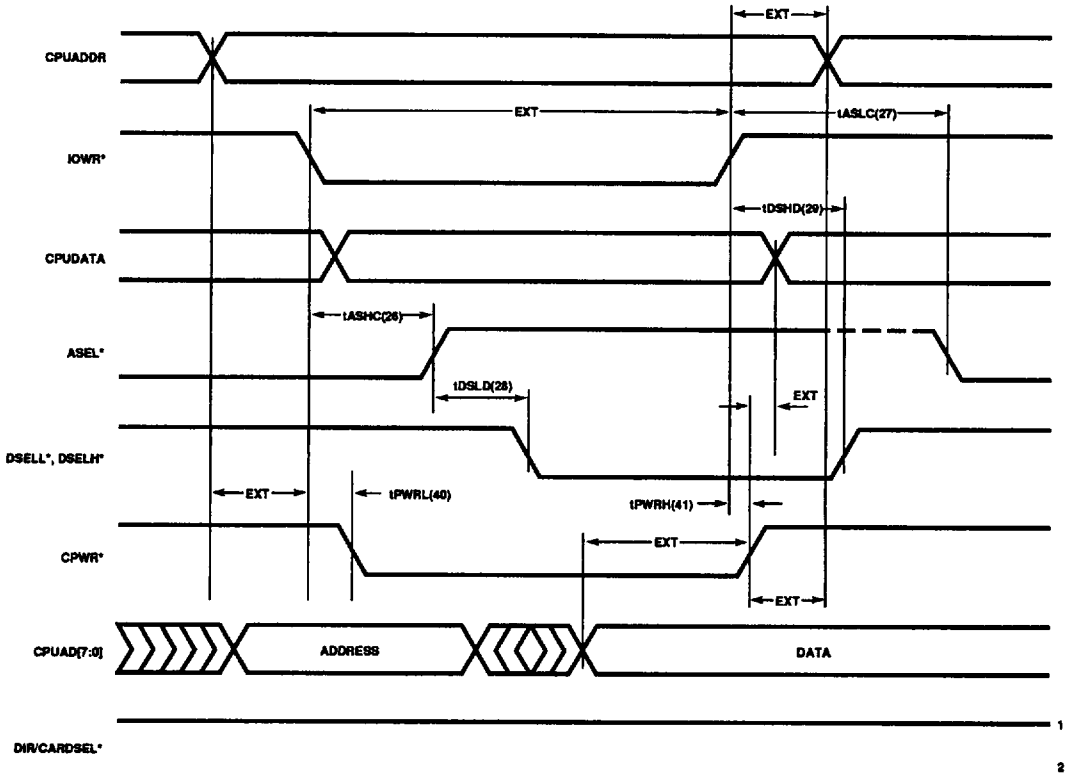
Symbol	Parameter	MIN	TYP	MAX	Units	Notes
EXT	I/O Write Pulse Width	150			ns	a,5
EXT	Address setup to CPWR* low	10			ns	b
EXT	Address hold from CPWR* high	10				
EXT	Data setup to CPWR* high	10				5
EXT	Data hold from CPWR* high	10				
$t_{PWRL\ (40)}$	CPWR* low delay from IOWR* low			30	ns	
$t_{PWRH\ (41)}$	CPWR* high delay IOWR* high			20	ns	
$t_{ASHC\ (26)}$	ASEL* high from IOWR* active	20		30	ns	
$t_{DSLD\ (28)}$	DSELL*, DSELH* low from ASEL* high	8		15	ns	
$t_{DSHD\ (29)}$	DSELH*, DSELL* high from IOWR* inactive	30		55	ns	
$t_{ASLC\ (27)}$	ASEL* low from IOWR * high	30		55	ns	

NOTES:

a) The figure and timing for the palette data and address is for illustrative purposes only. Values are given only for the signal generated by CL-GD610-C and CL-GD620-C.

b) Values given for parameters marked EXT are for reference. See data sheet of device used for design information.

– Numbers in the **Notes** column are correlated to remarks in section 7.3.3 under **General Notes**.



314610-7

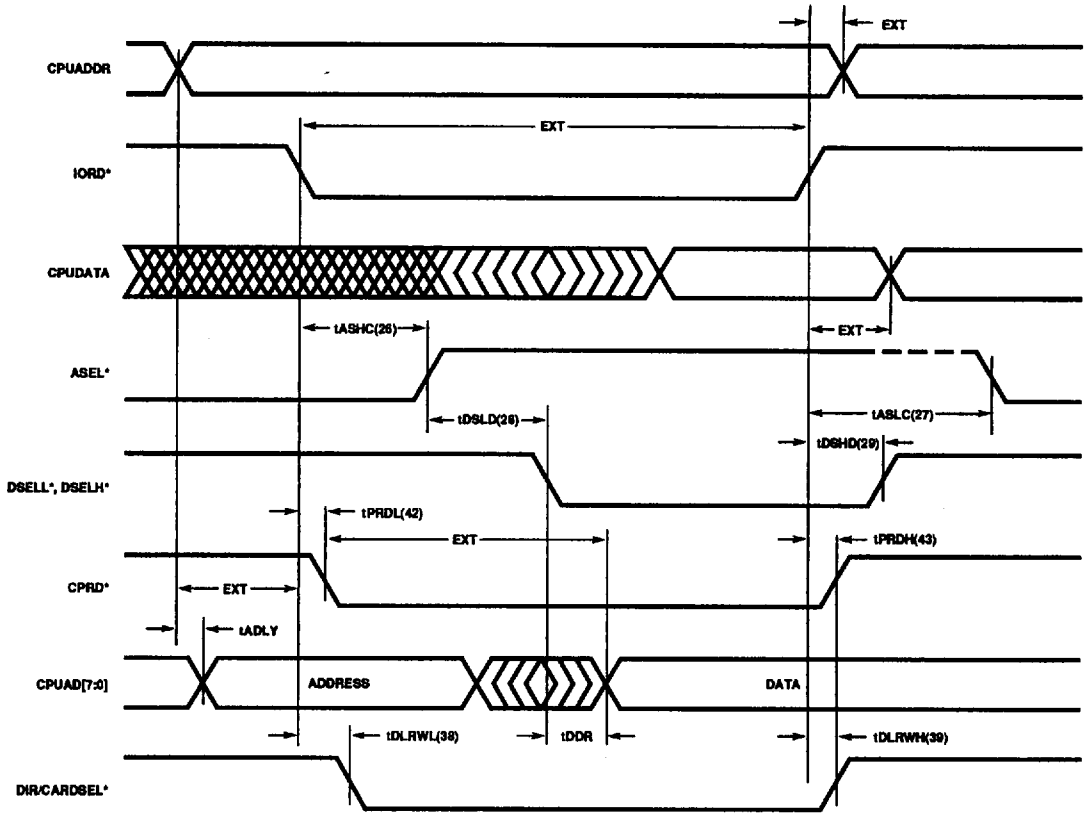
Figure 7–5. Color Palette Write Cycle

Table 7–6. Color Palette Read Cycle

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
EXT	I/O Read Pulse Width	150			ns	
EXT	Address setup to CPRD* low	10			ns	
EXT	Address hold from CPRD* high	10			ns	
EXT	Data valid from CPRD* low					
EXT	Data hold from CPRD* high					
t_{DLRWL} (38)	DIR/CARDSEL* low from IO/MEM read low			48	ns	
t_{DLRWH} (39)	DIR/CARDSEL* high delay from IORD* high			30	ns	
t_{PRDL} (42)	CPRD* low delay from IORD* low			33	ns	
t_{PRDH} (43)	CPRD* high delay from IORD* high			30	ns	
t_{ASHC} (26)	ASEL* high from command active	20		30	ns	
t_{DSLD} (28)	DSELL*, DSELH* low from ASEL* high	8		15	ns	
t_{DSHD} (29)	DSELH*, DSELL* high from command inactive	30		77	ns	
t_{ASLC} (27)	ASEL* low from command high	30		77	ns	

NOTE:

The figure and timing for the palette data and address is for illustrative purpose only. Values given only for the signal generated by the CL-GD610-C and CL-GD620-C. See data sheet of device used for design information.



314810-8

Figure 7–6. Color Palette Read Cycle

Table 7–7. Video Memory Read (System Interface)

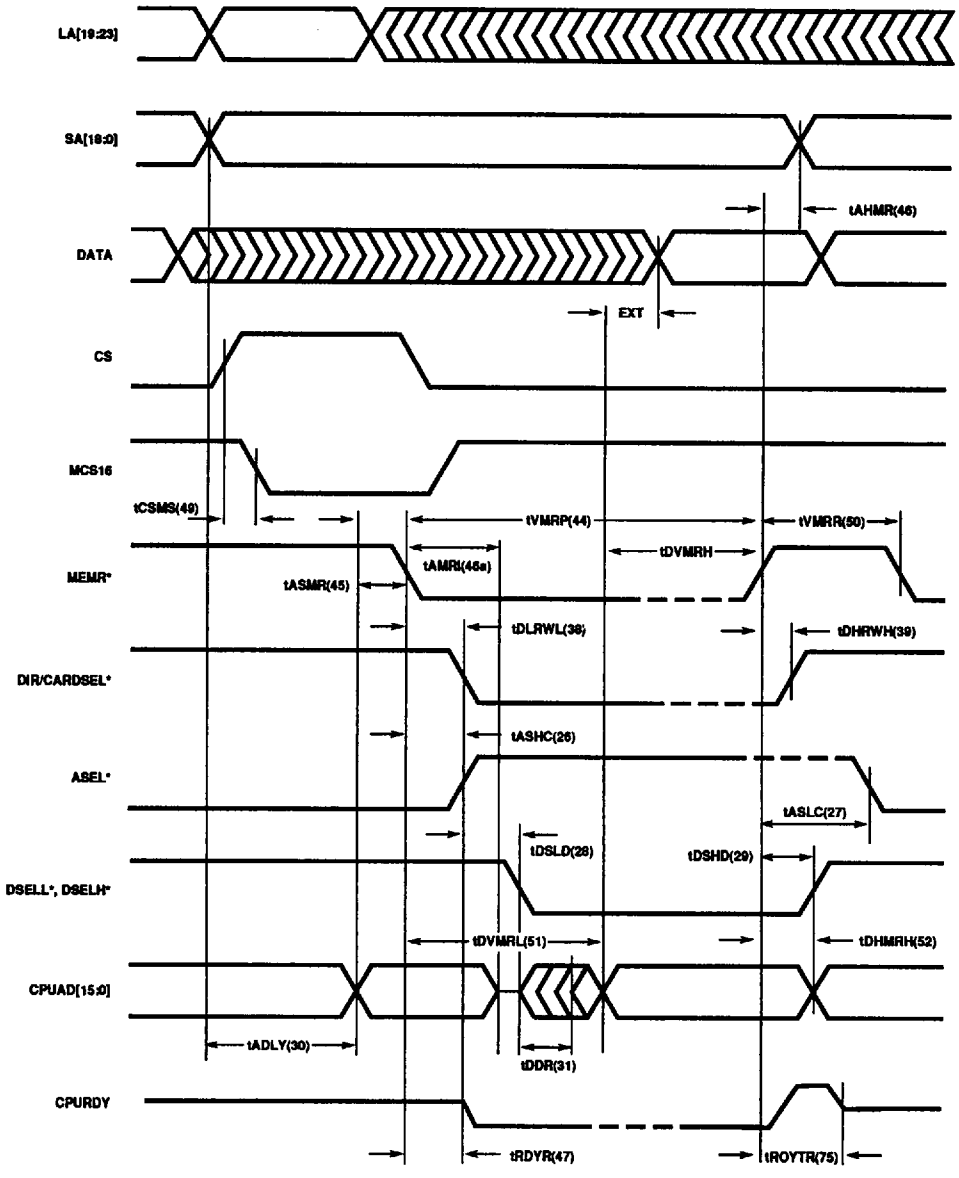
Symbol	Parameter	MIN	TYP	MAX	Units	Notes
t_{VMRP} (44)	Video Memory Pulse Width	200			ns	a
t_{ASMR} (45)	Address setup to MEMR* low	5				
t_{AHMR} (46)	Address hold from MEMR* high	0			ns	3
t_{AMRI} (46a)	Address hold from MEMR* low	30			ns	
t_{RDYR} (47)	CPURDY low from MEMR* low		15		ns	
t_{RDYTR} (48)	CPURDY tristate from MEMR* high					
t_{CSMS} (49)	MCS16* low from CS high address valid			15	ns	
t_{VMRR} (50)	MEMR* Recovery Time	100			ns	
t_{ASHC} (26)	ASEL* high from MEMW* active	20		30	ns	
t_{DSLD} (28)	DSELL*, DSELH* low from ASEL* high	8		15	ns	
t_{DSHD} (29)	DSELH*, DSELL* high from MEMW* inactive	30		55	ns	
t_{ASLC} (27)	ASEL* low from MEMW* high	30		55	ns	
t_{DLRWL} (38)	DIR/CARDSEL* low from IO/MEM read low			30	ns	
t_{DHRWH} (39)	DIR/CARDSEL* high from IORD*/MEMR* high			30	ns	
t_{DVMRL} (51)	Data valid from MEMR* low				ns	b
t_{DHMRH} (52)	Data hold from MEMR* high	10			ns	
t_{ADLY} (30)	CPUAD[7:0] delay from system address bus			20	ns	
t_{DDR}(31)	Data drive delay from DSELL*/H* low			20	ns	3

NOTES:

a) At least one wait state will be executed for memory read and memory write cycles.

b) Value for (51) is a function of DRAMs used and interleave selected; it will normally be minimum for 1:1 interleave.

– Numbers in the **Notes** column are correlated to remarks in section 7.3.3 under **General Notes**.



314610-9

Figure 7–7. Video Memory Read (System Interface)

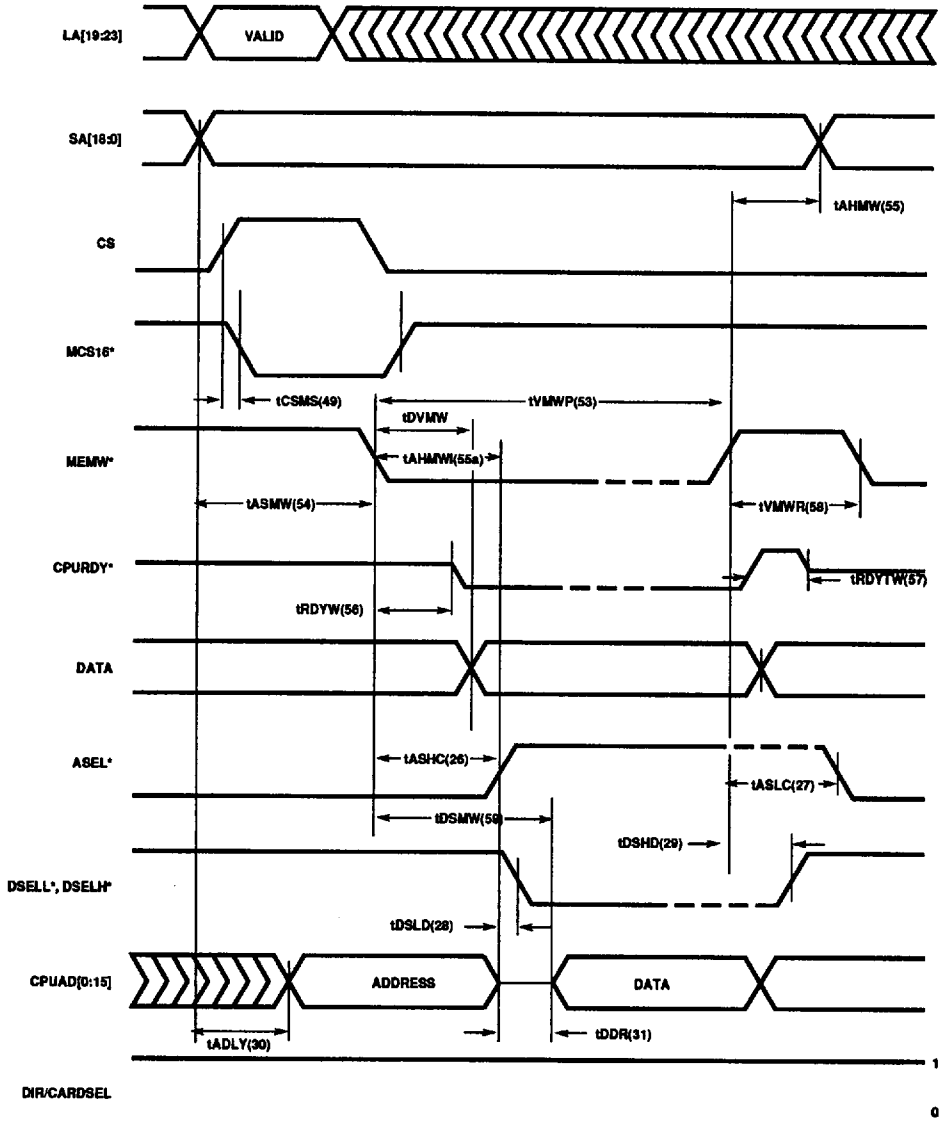
Table 7–8. Video Memory Write Cycle (System Interface)

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
$t_{VMWP\ (53)}$	MEMW* pulse width	200			ns	a
$t_{ASMW\ (54)}$	Address setup to MEMW* low	5			ns	
$t_{AHMW\ (55)}$	Address hold from MEMW* high	0			ns	
$t_{AHMWI(55a)}$	Address hold from MEMW* low	20			ns	
$t_{RDYW\ (56)}$	CPURDY low from MEMW* low		15		ns	
$t_{RDYTW\ (57)}$	CPURDY tristate from MEMW* high		15		ns	
$t_{CSMS\ (49)}$	MCS16* low from address valid			15	ns	
$t_{DSMW\ (59)}$	Data setup from MEMW* low			40	ns	
$t_{DHMW\ (60)}$	Data hold from MEMW* high	0			ns	
$t_{VMRW\ (58)}$	MEMW* recovery time	100			ns	
$t_{ASHC\ (26)}$	ASEL* high from MEMW* active	20		30	ns	
$t_{DSLD\ (28)}$	DSELL*, DSELH* low from ASEL* high	8		15	ns	
$t_{DSHD\ (29)}$	DSELH*, DSELL* high MEMW* inactive	40		55	ns	
$t_{ASLC\ (27)}$	ASEL* low from MEMW* high	30		55	ns	
$t_{DDR(31)}$	Data drive delay from DSELL*/H* low			20	ns	3
$t_{ADLY\ (30)}$	CPUAD[7:0] delay from system address bus			20	ns	3

NOTES:

a) At least one wait state will be executed for memory read and memory write cycles.

– Numbers in the **Notes** column are correlated to remarks in section 7.3.3 under **General Notes**.



314610-10

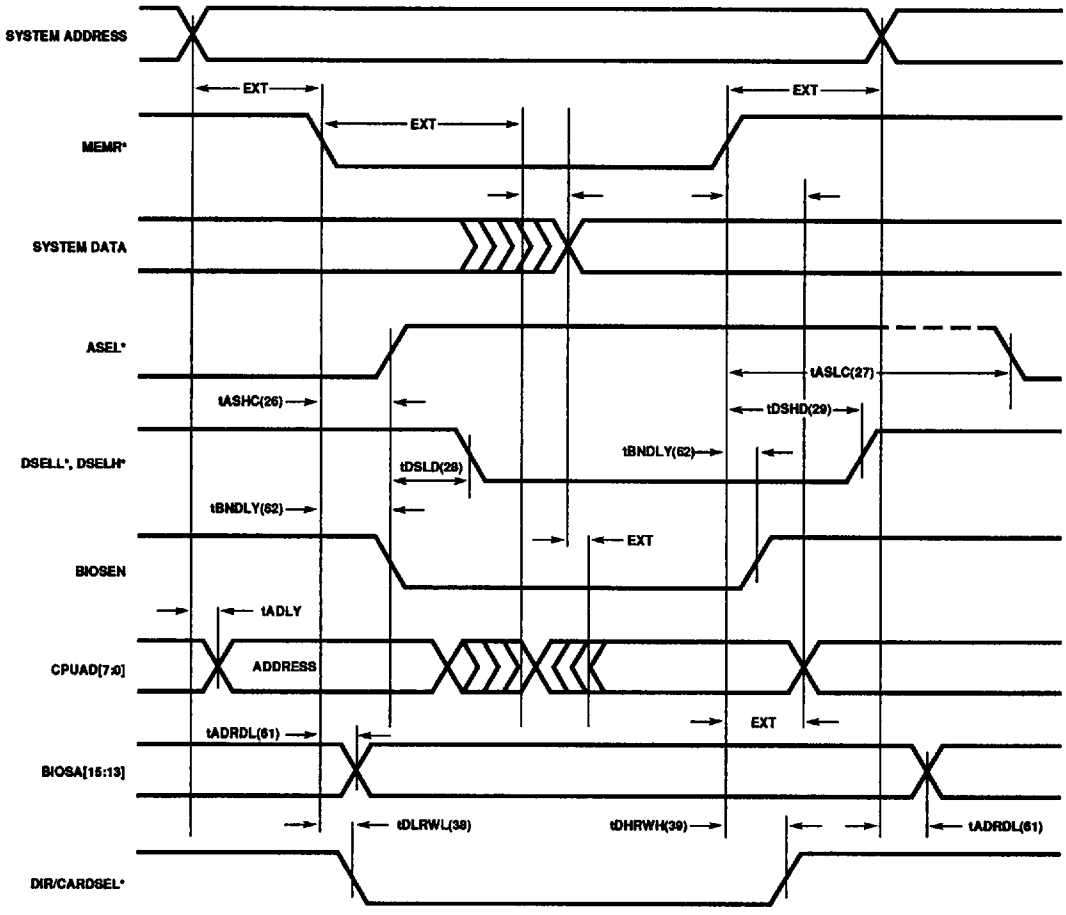
Figure 7–8. Video Memory Write (System Interface)

Table 7–9. BIOS Read Cycle

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
EXT	Address setup to MEMR* low				ns	5
EXT	Address hold from MEMR* high				ns	5
$t_{BNDLY\ (62)}$	BIOSEN* delay from valid MEMR* low	10		40	ns	
$t_{ASHC\ (26)}$	ASEL* high after MEMR* low			40	ns	
$t_{DSLD\ (28)}$	DSELL*, DSELH* low delay from ASELH* high	8		15	ns	
EXT	ROMDATA valid from MEMR* low					5
EXT	ROMDATA hold after MEMR* high					5
$t_{DSHD\ (29)}$	DSELL*, DSELH* high delay after command inactive	30		55	ns	
$t_{ADRDL\ (61)}$	Valid BIOSA <15:13> delay from MEMR* active	10		25		
$t_{DLRWL\ (38)}$	DIR/CARDSEL* low memory/IO read low			30	ns	
$t_{DHRWH\ (39)}$	DIR/CARDSEL* high from memory/IO read high			30	ns	
$t_{ASLC\ (27)}$	ASEL* low delay from MEMW* inactive	30		55	ns	

NOTE:

– Numbers in the **Notes** column are correlated to remarks in section 7.3.3 under **General Notes**.



314610-11

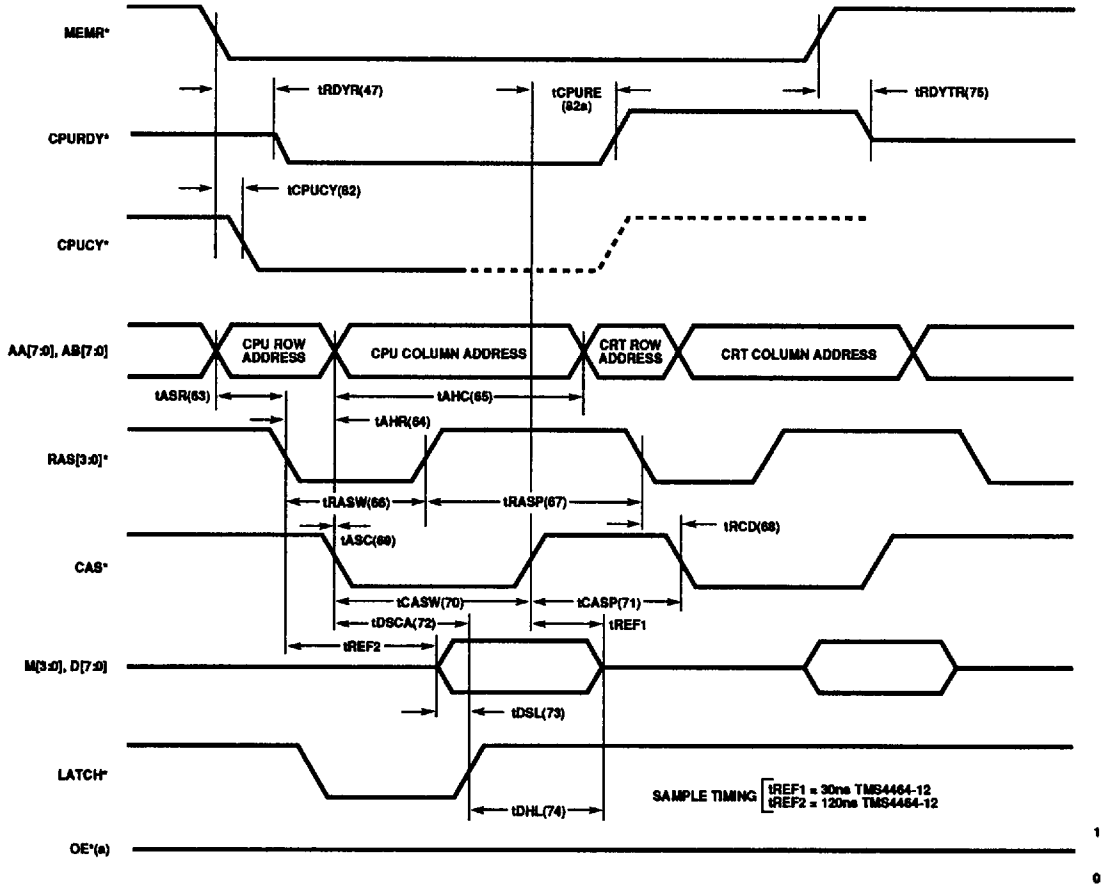
Figure 7–9. BIOS Read Cycle

Table 7-10. DRAM Sequencer Read Timing

SYMBOL	PARAMETER	X:Y - Z 1:4 - 9 3:2 - 9 †	1:4 - 8	1:7 - 8	3:2 - 8	1:2 - 6	1:1 - 8	1:1 - 9	
tC	CLKIN Cycle Time (100-ns DRAM)	25	30	25	30	50	50	50	Typ
tRDYR	CPURDY Low from MEMR* (4T)	15	15	15	15	15	15	15	Typ
tASR	Row Address Setup Time (63)	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
tAHR	Row Address Hold Time (64)	0.5 Tc	0.5 Tc	0.5 Tc	0.5 Tc	15	15	15	Typ
tAHC	Column Address Hold Time (65)	4 Tc	3 Tc	4 Tc	3 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
tRASW	RAS* Low Time (66)	4 Tc	3 Tc	4 Tc	3 Tc	2 Tc	2 Tc	2 Tc	Typ
tRASP	RAS* Precharge (67)	3 Tc	3 Tc	3 Tc	3 Tc	2 Tc	2 Tc	2 Tc	Typ
tRCD	RAS* to CAS* Delay (68)	1 Tc	1 Tc	1 Tc	1 Tc	0.5 Tc	0.5 Tc	0.5 Tc	Typ
tASC	Column Address Setup Time (69)	5	5	5	5	5	5	5	Typ
tCASW	CAS* Low Time (70)	5 Tc	4 Tc	5 Tc	4 Tc	2.5 Tc	2.5 Tc	2.5 Tc	Typ
tCASP	CAS* Precharge (71)	2 Tc	2 Tc	2 Tc	2 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
tDSCA	Data Sample From CAS* (72)	4.5 Tc	3.5 Tc	4.5 Tc	3.5 Tc	2.0 Tc	2.0Tc	2.0Tc	Typ
tDSL	Data Setup (to LATCH*) (73)	0	0	0	0	0	0	0	Typ
tDHL	Valid Data Hold Time (to LATCH*) (74)	.5 Tc	.5 Tc	.5 Tc	.5 Tc	.5 Tc	.5 Tc	.5 Tc	Typ
tRDYTR	VMEMR* Inactive to CPURDY* Tristate (75)	15	15	15	15	15	15	15	Typ
tRDYI	CPU Read Cycle End to CPURDY* Inactive (76)	1 Tc	1 Tc	1 Tc	1 Tc	1 Tc	1 Tc	1 Tc	Typ
tCPUCY	VMEMW*/R* low to CPUCY* low (82)	4 Tcc	4 Tcc	7 Tcc	3 Tcc	2 Tcc	1 Tcc	1 Tcc	Max a, b
tCPURE	Read Cycle End to CPURDY high (82a)	4 Tc	2 Tc	2 Tc	2 Tc	2 Tc	2 Tc	2 Tc	Typ

† X:Y - Z (X = CPU Cycles, Y = CRT Cycles, Z = Dots / Character)

NOTES: All times are in nanoseconds (ns) unless otherwise noted. (a) Tcc - 1 character clock. (b) Value of tCPUCY is 9 Tcc during synchronous reset.



(a) Signal timing for 64K x 16 DRAM interface only.

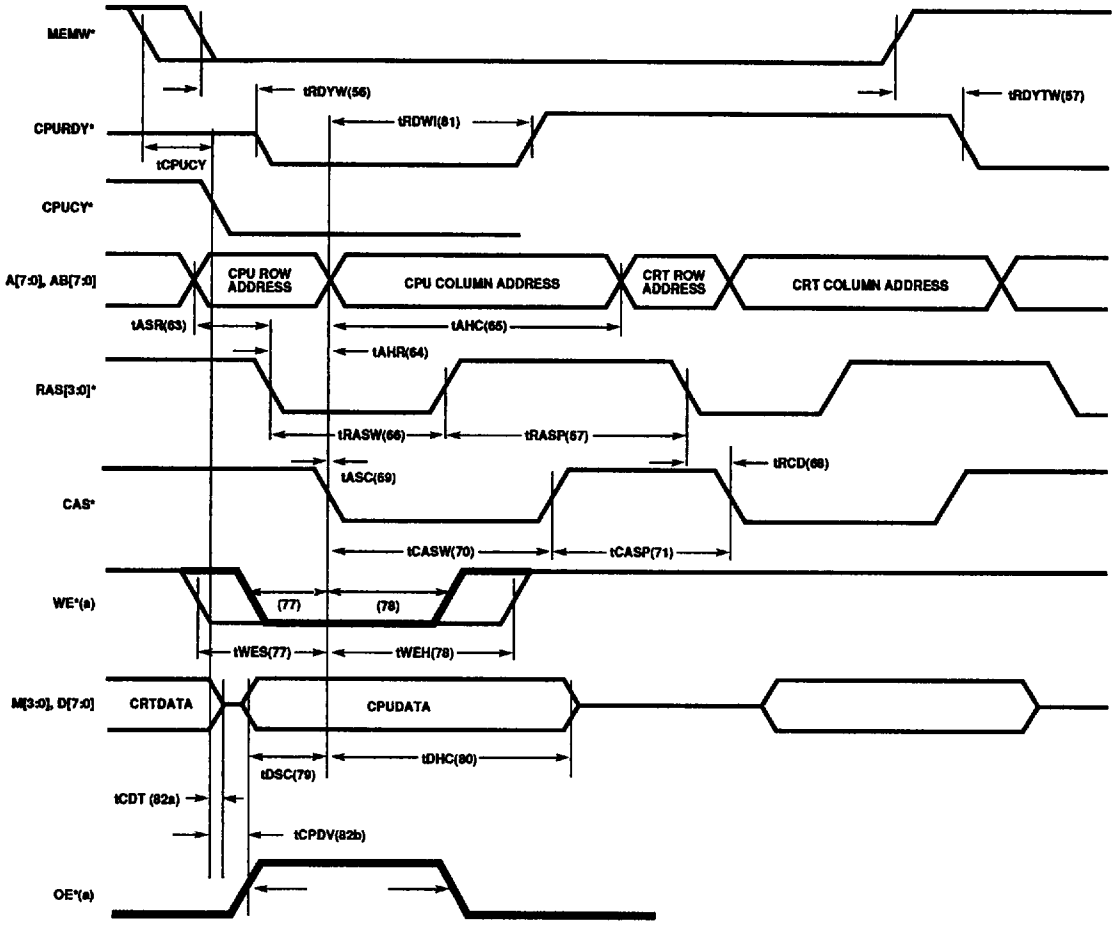
Figure 7–10. DRAM Sequencer Read Timing

Table 7-11. DRAM Sequencer Write Timing

SYMBOL	PARAMETER	X:Y - Z 1:4 - 9 † 3:2 - 9	1:4 - 8	1:7 - 8	3:2 - 8	1:2 - 6	1:1 - 8	1:1 - 9	
tC	CLKIN Cycle Time (100 ns DRAM)	25	30	25	30	50	50	50	Typ
tRDYW	CPURDY Low from VMEMR* (56)	15	15	15	15	15	15	15	Typ
tASR	Row Address Setup Time (63)	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
tAHR	Row Address Hold Time (64)	0.5 Tc	0.5 Tc	0.5 Tc	0.5 Tc	15	15	15	Typ
tAHC	Column Address Hold Time (65)	4 Tc	3 Tc	4 Tc	3 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
tRASW	RAS* Low Time (66)	4 Tc	3 Tc	4 Tc	3 Tc	2 Tc	2 Tc	2 Tc	Typ
tRASP	RAS* Precharge (67)	3 Tc	3 Tc	3 Tc	3 Tc	2 Tc	2 Tc	2 Tc	Typ
tRCD	RAS* to CAS* Delay (68)	1 Tc	1 Tc	1 Tc	1 Tc	0.5 Tc	0.5 Tc	0.5 Tc	Typ
tASC	Address Setup to CAS (69)	5	5	5	5	5	5	5	Typ
tCASW	CAS* Low Time (70)	5 Tc	4 Tc	5 Tc	4 Tc	2.5 Tc	2.5 Tc	2.5 Tc	Typ
tCASP	CAS* Precharge (71)	2 Tc	2 Tc	2 Tc	2 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
tWES	WE* Setup to CAS* (77)	(1)1.5 Tc	(1)1.5 Tc	(1)1.5 Tc	(1)1.5 Tc	(1)1 Tc	(.5)1 Tc	(.5)1 Tc	Typ,a
tWEH	WE* Hold from CAS* (78)	(3)5 Tc	(2)4 Tc	(3)5 Tc	(2)4 Tc	(1)2.5 Tc	(1.5)2.5 Tc	(1.5)2.5 Tc	Typ,a
tDSC	Data Setup to CAS* (79)	5	5	5	5	10	10	10	Typ
tDHC	Data Hold to CAS* (80)	5Tc	4Tc	5 Tc	4Tc	2.5 Tc	2.5 Tc	2.5 Tc	Typ
tRDWI	CPU Write Cycle End to CPURDY* Inactive (81)	2 Tc	2 Tc	2 Tc	2 Tc	2 Tc	2 Tc	2 Tc	Typ
tRDYTW	VMEMR* Inactive to CPURDY* Tristate (57)	15	15	15	15	15	15	15	Typ
tCPUCY	VMEMR*/W* low to CPUCY* low (82)	4 Tcc	4 Tcc	7 Tcc	3 Tcc	2 Tcc	1 Tcc	1 Tcc	Max,b,c
tCDT (82a)	CRT Data Invalid from CPUCY* low	.5 Tc	.5 Tc	.5 Tc	.5 Tc	.5 Tc	.5 Tc	.5 Tc	Typ
tCPDV (82b)	CPU Data Valid from CPUCY* low	Tc	Tc	Tc	Tc	Tc	Tc	Tc	Typ
tEOH(82C)	OE* high period	4 Tc	3 Tc	4 Tc	3 Tc	2 Tc	2 Tc	2 Tc	Typ

† X:Y - Z (X = CPU Cycles, Y = CRT Cycles, Z = Dots / Character)

NOTES: (1) All times are in nanoseconds (ns) unless otherwise noted. (a) Numbers in brackets are for 64K x 16 DRAM interface. (b) Tcc - 1 character clock. (c) Value of tCPUCY is 9 Tcc during synchronous reset.



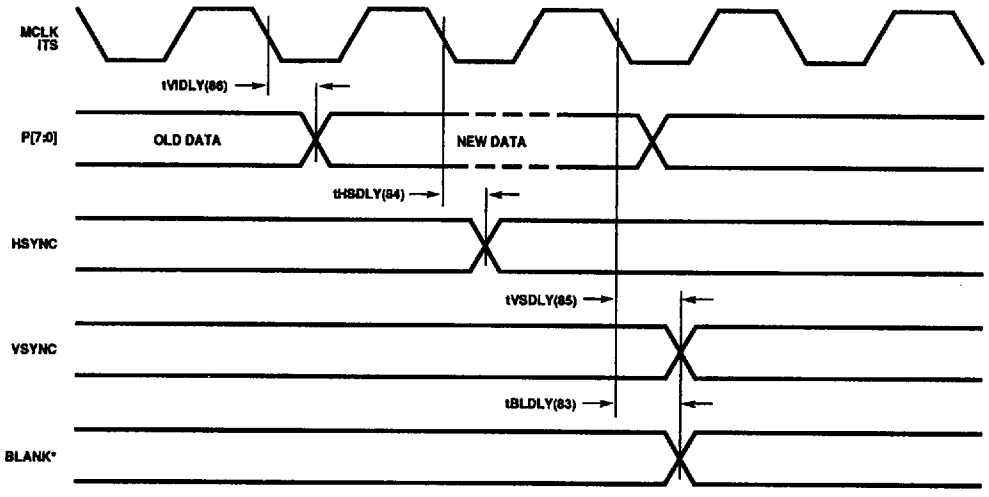
314810-13

(a) Thick-line waveforms indicate 64K x 16 DRAM interface.

Figure 7–11. DRAM Sequencer Write Timing

Table 7–12. CRT Interface Timing

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
$t_{BLDLY\ (83)}$	BLANK* delay from ITS/MCLK*	12		20	ns	
$t_{HSDLY\ (84)}$	HSYNC delay from ITS/MCLK*	10		40	ns	
$t_{VSDLY\ (85)}$	VSYNC delay from ITS/MCLK*	20		60	ns	
$t_{VIDLY\ (86)}$	P[7:0], video data delay from ITS/MCLK*	10		24	ns	



314610-14

Figure 7–12. CRT Interface Timing

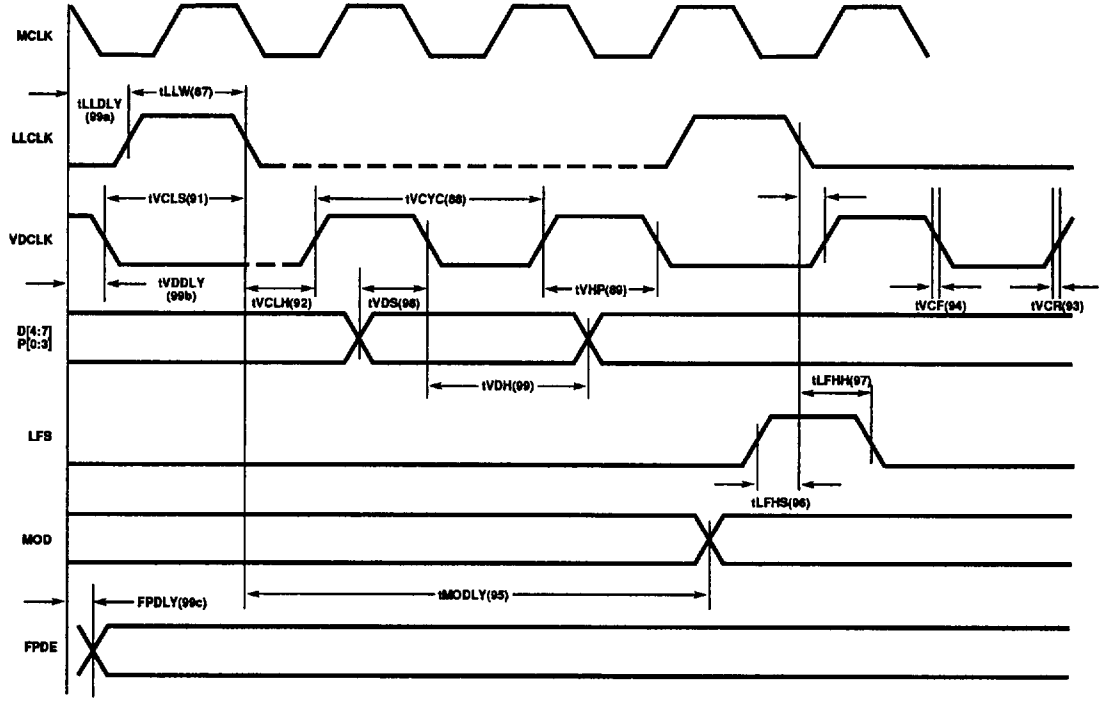
Table 7–13. LCD Interface Timing

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
$t_{LLW\ (87)}$	LLCLK pulse width	4Tc			ns	a
$t_{VCYC\ (88)}$	VDCLK cycle time	4Tc (1)			ns	b
$t_{VHP\ (89)}$	VDCLK high width	2Tc (.5Tc)			ns	
$t_{VLP\ (90)}$	VDCLK low width	2Tc (.5Tc)			ns	
$t_{VCLS\ (91)}$	VDCLK low setup to LLCLK	4Tc+20 (.5Tc)			ns	
$t_{VCLH\ (92)}$	VDCLK low hold time after LLCLK low	4Tc-20 (.5Tc)			ns	
$VCR_{\ (93)}$	VDCLK rise time			10	ns	
$t_{VCF\ (94)}$	VDCLK fall time			10	ns	
$t_{MODLY\ (95)}$	MOD delay from LLCLK low			30	ns	
$t_{LFHS\ (96)}$	LFS high setup time to LLCLK low	4Tc (.5Tc)			ns	
$t_{LFHH\ (97)}$	LFS high hold time after LLCLK low	4Tc (.5Tc)			ns	
$t_{VDS\ (98)}$	Video data setup time	2Tc (.5Tc)			ns	
$t_{VDH(99)}$	Video data hold time	2Tc (.5Tc)			ns	
$t_{LLDLY\ (99a)}$	LLCLK delay from MCLK/ITS			25	ns	
$t_{VDDLY\ (99b)}$	VDCLK delay from MCLK/ITS	4Tc (.5Tc)		25	ns	
$t_{FPDLY\ (99c)}$	FPDE delay from MCLK/ITS	4Tc (.5Tc)		60	ns	

NOTES:

a) Tc refers to MCLK cycle time. See figure and table on clock specifications for details.

b) VDCLK cycle time is 1 MCLK for other panels, indicated in brackets.



314610-15

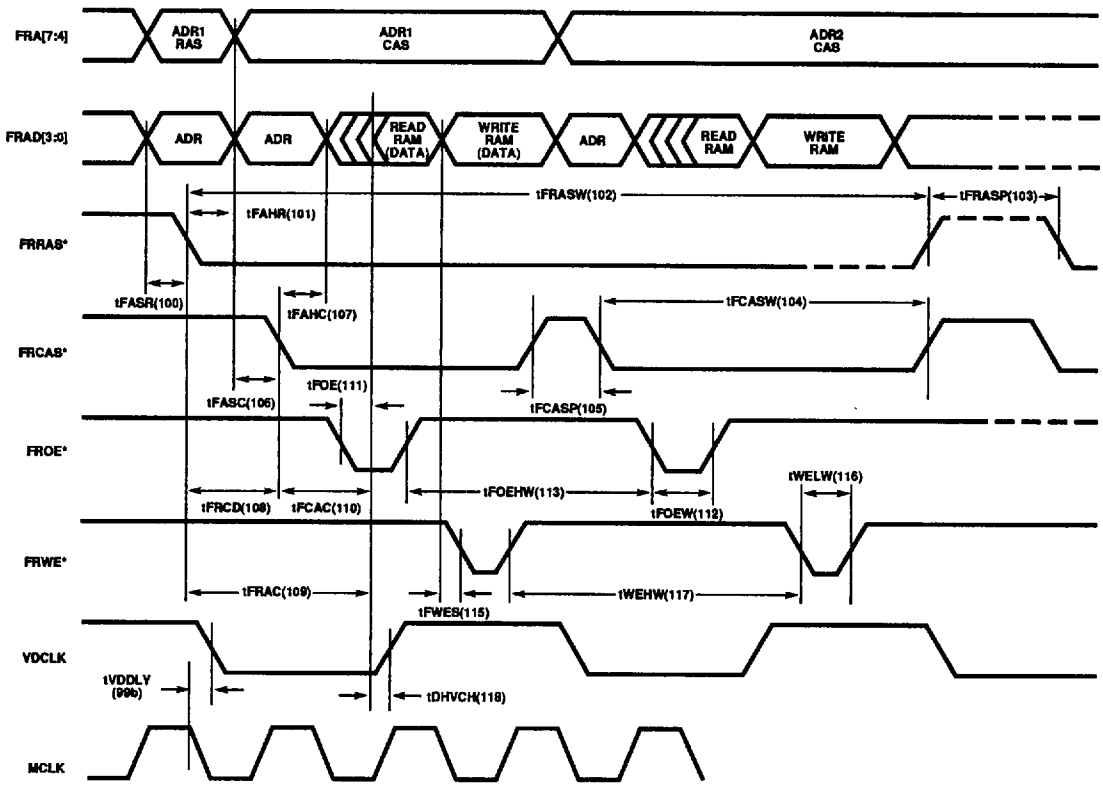
Figure 7–13. LCD Interface Timing

Table 7–14. LCD Frame Buffer Read-Modify-Write Timing

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
FTc	MCLK cycle in LCD mode	42		62.5	ns	a
$t_{VDDLY\ (99b)}$	VDCLK delay from MCLK			25	ns	
$t_{FASR\ (100)}$	Row address setup time	2Tc			ns	
$t_{FAHR\ (101)}$	Row address hold time	0.5Tc			ns	
$t_{FRASW\ (102)}$	FRAS* low width	641Tc			ns	
$t_{FRASP\ (103)}$	FRRAS* high width	12Tc			ns	
$t_{FCASW\ (104)}$	FRCAS* low width	3.5Tc			ns	
$t_{FCASP\ (105)}$	FRCAS* high width	0.5Tc			ns	
$t_{FASC\ (106)}$	Column address setup time to FRCAS* low	0.5Tc			ns	
$t_{FAHC\ (107)}$	Column address hold time after FRCAS* low	0.5Tc			ns	
$t_{FRCD\ (108)}$	FRCAS* low delay from FRRAS* low	Tc			ns	
$t_{FRAC\ (109)}$	FRRAS* access time	2.5Tc			ns	
$t_{FCAC\ (110)}$	FRCAS* access time	1.5Tc			ns	
$t_{FOE\ (111)}$	FROE* access time	Tc			ns	
$t_{FOEW\ (112)}$	FROE* low pulse width	Tc			ns	
$t_{FOEHW\ (113)}$	FROE* high pulse width	1.5Tc			ns	
$t_{FOEA\ (114)}$	Data out delay from FROE*	0.5Tc+10			ns	
$t_{FWES\ (115)}$	Write data setup to FRWE*	0.5Tc-10			ns	
$t_{WELW\ (116)}$	FRWE* low pulse width	Tc			ns	
$t_{WEHW\ (117)}$	FRWE* high pulse width	3Tc			ns	
$t_{DHVCH\ (118)}$	Data hold after VDCLK rising edge	0.5Tc-10			ns	

NOTE:

a) Tc refers to MCLK cycle time. See figure and table on clock specifications for details.



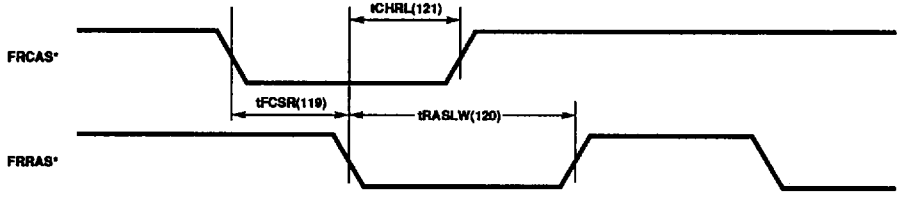
314610-16

Figure 7–14. LCD Frame Read-Modify-Write Cycle

Table 7–15. LCD Frame Buffer Refresh Cycle

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
$t_{FCSR\ (119)}$	FRCAS* setup to FRRAS*	4Tc			ns	
$t_{RASW\ (120)}$	FRRAS* Low Width	4Tc			ns	
$t_{CHRL\ (121)}$	FRCAS* hold after FRRAS* low	4Tc			ns	

NOTE:
Frame buffer read-modify-write cycle and refresh cycles are specified in Tc units where Tc is one MCLK/ITS period. For MCLK specifications, see figure and table on clock specifications.



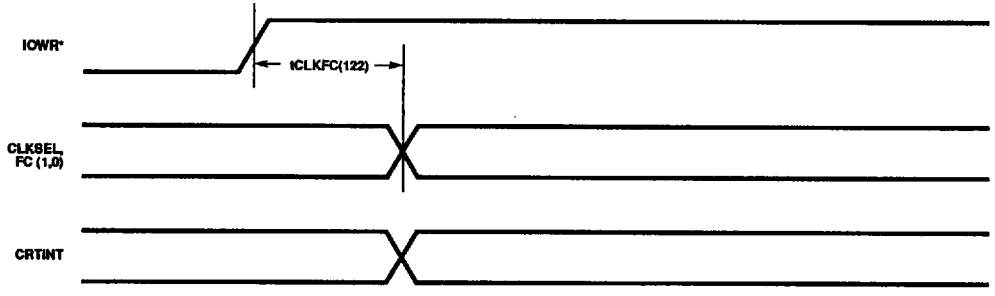
314610-17

NOTE: Frame buffer read-modify-write cycle and refresh cycles are specified in Tc units where Tc is one MCLK cycle period. For MCLK specifications, see figure.

Figure 7–15. LCD Frame Buffer Refresh Cycle

Table 7–16. Miscellaneous Timing

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
$t_{CLKFC\ (122)}$	CLKSEL FC[1:0] output delay from IOWR* high			100	ns	
$t_{INT\ (123)}$	CRTINT delay from IOWR* high			100	ns	



314610-18

Figure 7–16. Miscellaneous Timing

Table 7–17. CL-GD620-C Video Interface

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
$t_{SLLD\ (124)}$	S/L* low delay from MCLK/ITS			10	ns	a
$t_{SLHD\ (125)}$	S/L* high delay from MCLK/ITS			15	ns	
$t_{BLDLY\ (83)}$	BLANK* delay from MCLK/ITS	10		24	ns	
$t_{DEDLY\ (126)}$	DE delay from MCLK/ITS			20	ns	
$t_{CDLY\ (127)}$	CURSOR delay from MCLK/ITS			20	ns	
$t_{HSDLY\ (84)}$	HSYNC delay from MCLK/ITS	10		40	ns	
$t_{VSDLY\ (85)}$	VSYNC delay from MCLK/ITS	20		60	ns	

NOTE:

a) At least one wait state will be executed for memory read and memory write cycles.

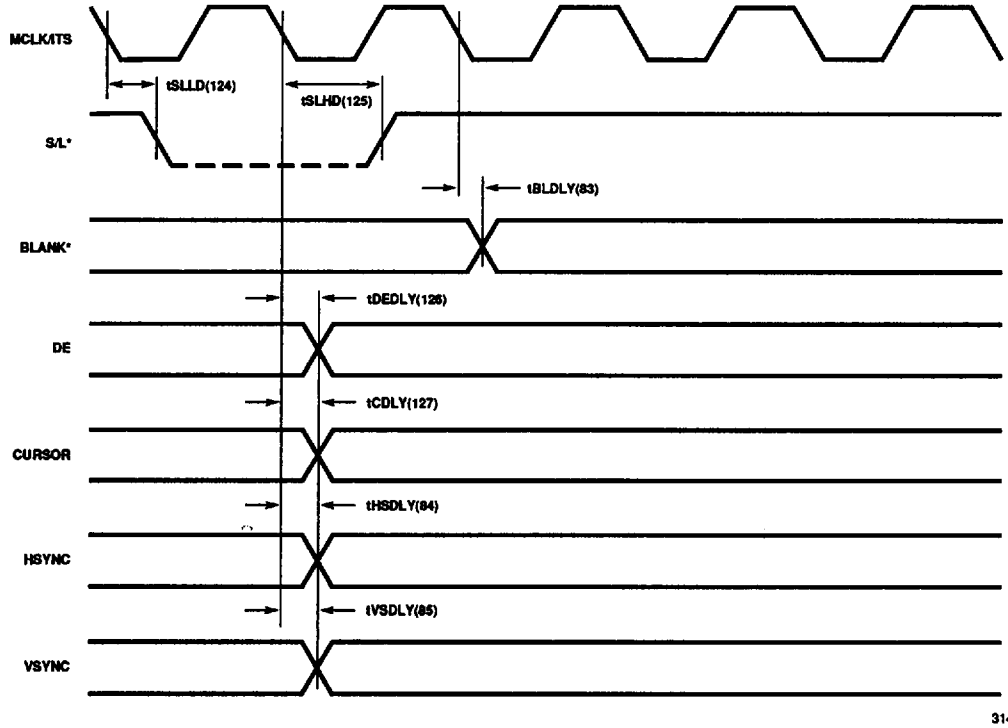


Figure 7–17. CL-GD620-C Video Interface

Table 7–18. CL-GD610-C Video Interface

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
$t_{BLSC\ (128)}$	BLANK setup to MCLK/ITS	20			ns	
$t_{DESC\ (129)}$	DE setup to MCLK/ITS	20			ns	
$t_{CSC\ (130)}$	CURSOR setup to MCLK/ITS	20			ns	
$t_{VSSC\ (131)}$	VSYNC setup to MCLK/ITS	25			ns	
$t_{BHCL\ (132)}$	BLANK hold to MCLK/ITS	20			ns	
$t_{DEHC\ (133)}$	DE hold to MCLK/ITS	20			ns	
$t_{CHC\ (134)}$	CURSOR hold to MCLK/ITS	20			ns	
$t_{VSHC\ (135)}$	VSYNC hold to MCLK/ITS	25			ns	
t_{SLCL}				10	ns	
t_{SLHC}				10	ns	

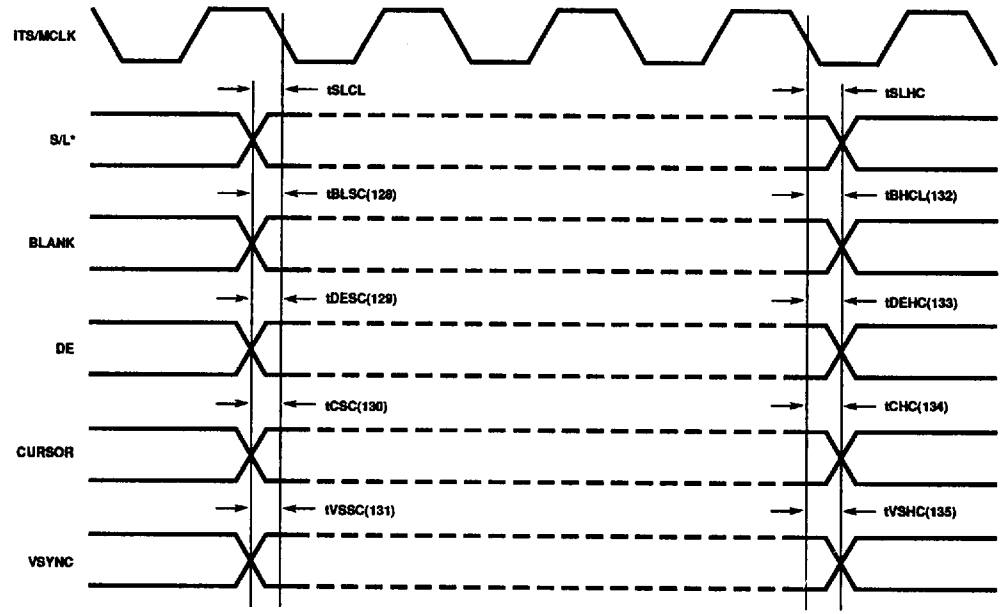
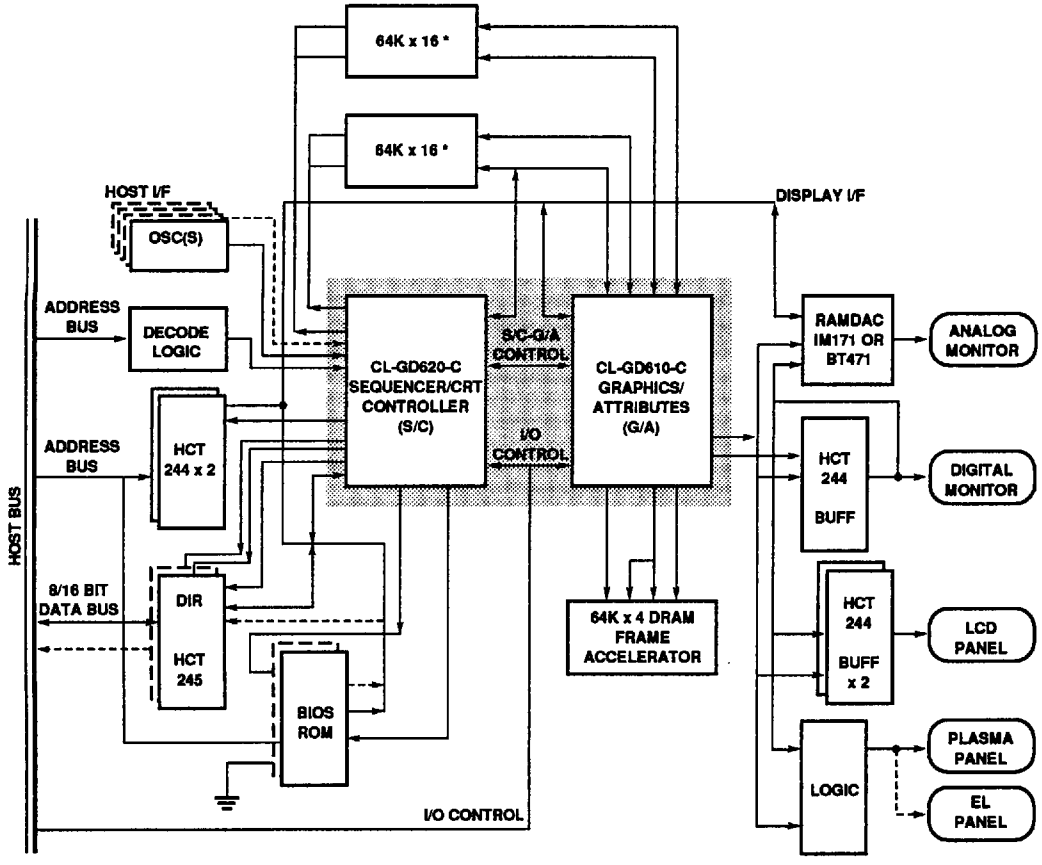


Figure 7–18. CL-GD610-C Video Interface

8. TYPICAL APPLICATION

8.1 System Block Diagram



* Alternately, 64K x 4 (8), 256K x 4 (8) or 64K x 8 (4) can be used.

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Figure 8–1. CL-GD610/620-C System Block Diagram

8.2 Parts List

Core Logic	16-bit Interface	Display RAM
• 1 CL–GD610-C Graphics/Attributes chip		• 8 256 x 4 DRAMs or
• 1 CL–GD620-C Sequencer/CRT Controller chip		• 8 64K x 4 DRAMs or
• 1 BIOS (64 KB 27C512 ROM) or	• 2 C256 ROMs	• 4 128K x 8 pseudo
• 1 HCT245 Octal Data Bus transceiver or	• 2 HCT245	static RAMs or
• 2 HCT244 Octal Address Bus buffer		• 2 64K x 16 DRAMs or
• 1 HCT244 Octal Pixel Output Bus buffer		• 4 64K x 8 DRAMS

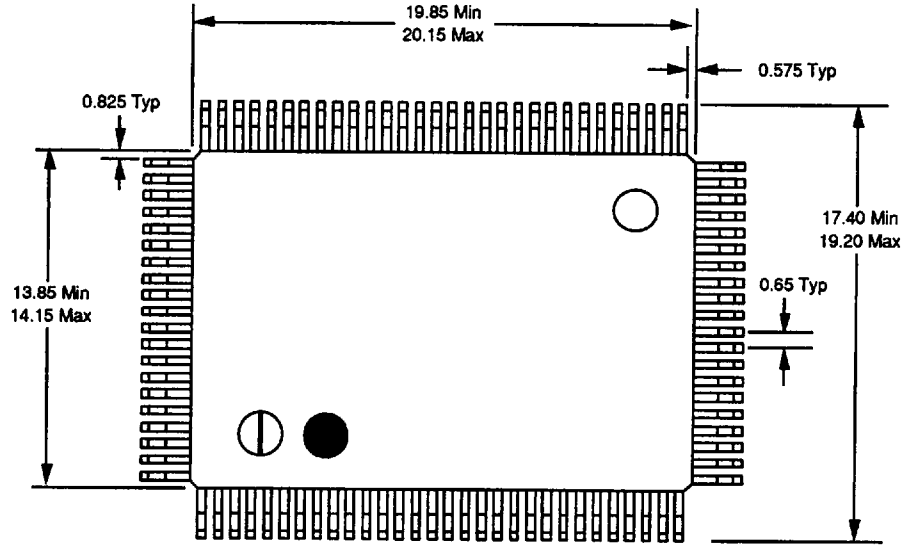
7 core ICs for 8-bit I/F; 9 core ICs for 16-bit I/F; 4 RAM chips for 512K bytes or 8 RAM chips for 256K bytes/1M byte.

Optional Logic

- 1/2 HCT244 Octal Pixel Output Bus buffer for LCD panel interface
- 1 Refresh accelerator (one 64K x 4 DRAM) for LCD panel interface
- 1 IMSG171 or BT471 RAMDAC or equivalent (required for VGA only)
- 1 MSI device for plasma or electroluminescent panel interface
- 1 PLL IC to replace up to 5 crystal oscillators
- 2 Latches to demux addresses for PSRAM or SRAM from RAS, CAS
- 2 MSI devices to control latches for PSRAM/SRAM applications

9. PACKAGE INFORMATION

9.1 100-Pin QFP Package Dimensions



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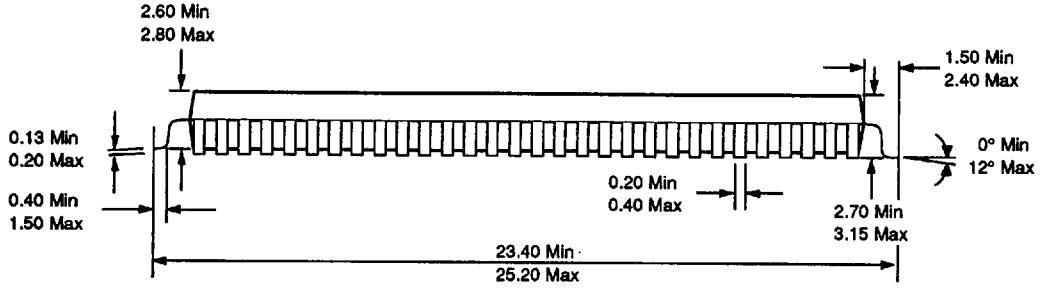

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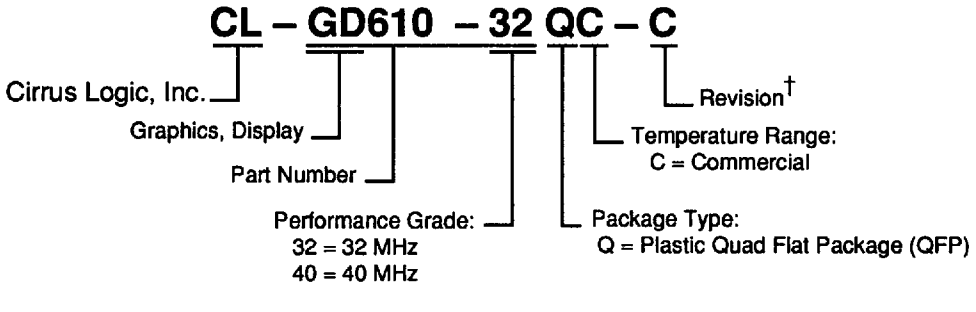
NOTE: All dimensions are in millimeters and are nominal unless otherwise stated.

Figure 9–1. 100-Pin QFP Package Dimensions

10. ORDERING INFORMATION

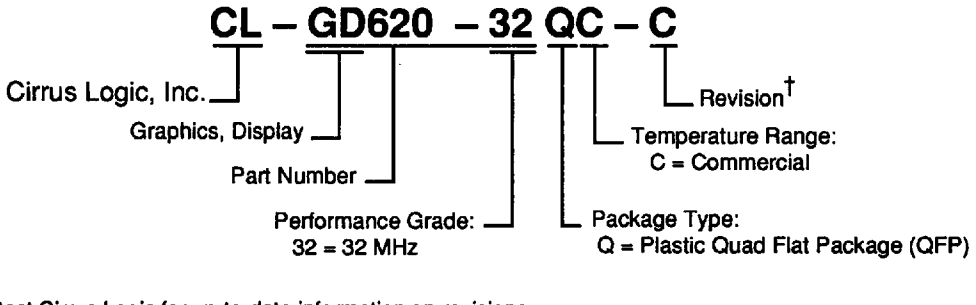
10.1 Numbering Guide – Graphics/Attributes Chip:



† Contact Cirrus Logic for up-to-date information on revisions.

Figure 10–1. Numbering Guide – Graphics/Attributes Chip

10.2 Numbering Guide – Sequencer/CRT Controller:



† Contact Cirrus Logic for up-to-date information on revisions.

Figure 10–2. Numbering Guide – Sequencer/CRT Controller