CIRRUS LOGIC®

CL-GD6410

Data Book

FEATURES

- **Single-chip VGA controller**
- **IBM® VGA hardware-compatible**
- **Simultaneous CRT and LCD (SimulSCAN™) operation**
- **Two 256K x 4 DRAM video memory for small form factor**
- **Integrates RAMDAC**
- **Integrates LCD panel interface**
  - — Control and data buffering
  - — Power-sequencing logic
- **Direct connection to ISA (PC AT) Bus**
- **Frame-Accelerator for low-active power**
- **Standby and Suspend Modes to save power**
- **Expanded operational range: 5V ± 10%**
  - — Low-voltage (4.5V) operation saves power
- **64-shade grayscale on monochrome STN LCD**
  - — NTSC sum-to-gray color mapping
  - — Multiple sum-to-gray weighting options
- **Direct connection to 512-color TFT LCD**
  - — Single-controller design for STN monochrome and TFT color LCDs
- **Graphics and text expansion and compression maps CRT modes to fixed-resolution LCD**
- **800 x 600 x 16 color on analog CRT**
- **8- or 16-bit CPU interface**
- **160-pin (EIAJ-standard) QFP package**
  - — Pinout optimized for efficient board layout

High-Integration LCD VGA Controller for Notebook Computers

OVERVIEW

The CL-GD6410 is a single-chip VGA controller optimized for use in notebook computers, where reduced form factor and low power consumption are critical design objectives. With the CL-GD6410, a complete motherboard VGA controller requires only four or five ICs and can fit within four square inches (excluding power sources and connectors). A true two-DRAM video memory (256K x 4), on-chip RAMDAC, direct-connect ISA (PC AT) Bus interface, and direct-connect LCD interface all help to minimize the form factor.

By using Cirrus Logic's Frame-Accelerator technique, the CL-GD6410 is able to provide a high vertical refresh rate for dual-scan LCD panels while operating at approximately one-half the clock speed of other LCD controller solutions; this provides a significant reduction in full-active power consumption and extends battery life. In addition, Standby and Suspend Modes are supported in the hardware of the CL-GD6410 to enable multiple levels of system power management.

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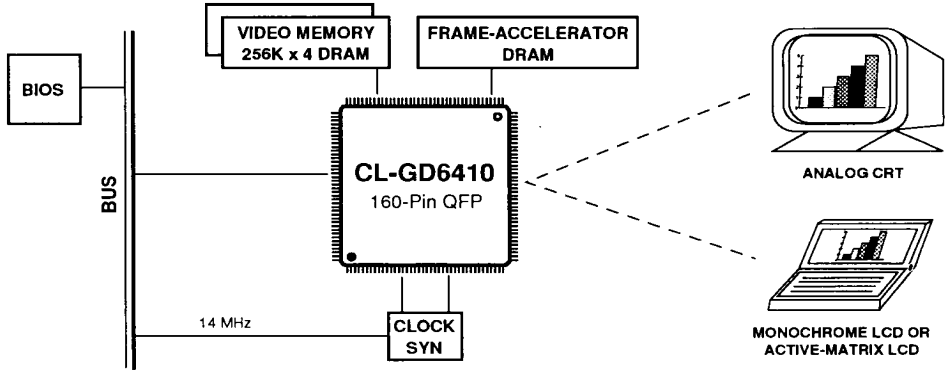
System Block Diagram



April 1993

OVERVIEW (cont.)

Cirrus Logic LCD VGA controllers have earned a reputation for providing the industry's best LCD image quality. The CL-GD6410 continues this lineage, providing 64 shades of gray on monochrome LCD panels. Duty-cycle modulation, combined with dynamic pattern-management algorithms, provide 640 x 480-resolution grayscales with no apparent flicker. Pixel-doubling and stippling techniques provide increased grayscale in the VGA high-color Mode 13. In all cases, the Cirrus Logic grayscale provides consistent linear-step functions, making smooth transitions from black, through the grayscale, to white.

With a direct connection to 512-color TFT (Thin Film Transistor) LCD panels, the CL-GD6410 provides a single-controller solution for 64-grayscale-monochrome and 256-simultaneous-color portable computers. The CL-GD6410 also provides a direct interface to the CL-GD6340, Cirrus Logic's color LCD interface controller. With this combination, color LCDs can produce stunning, CRT-quality images.

The CL-GD6410 panel interface includes programmable panel parameters that allow a controller design to be optimized for excellent display quality on a variety of panels.

SimulSCAN™ operation, a Cirrus Logic technique for achieving simultaneous CRT and LCD operation, is one of the features of the CL-GD6410. SimulSCAN allows the portable computer to become a key part of presentation environments for sales force automation, field service, and educational organizations.

SimulSCAN™ Operation

SimulSCAN operation is:

- ❑ Simultaneous display on internal LCD and external CRT
- ❑ Compatible with VGA modes — not limited to special modes
- ❑ Compatible with VGA applications software — not limited to special applications
- ❑ Transparent to the viewer of the external display

SimulSCAN provides:

- ❑ An external display for audience presentations — fixed frequency or multi-frequency analog CRT
- ❑ An internal display for computer operation — single-scan or dual-scan LCD (6.3-MHz panel speed required for dual-scan LCD)
- ❑ Reverse intensity (optional) on the internal display; simultaneous with normal operation of the external display

SimulSCAN operation allows the portable computer to be used in large audience presentation/demonstration environments. With SimulSCAN, the computer provides an analog RGB video signal for overhead projection systems, standard CRTs, or large-screen CRTs for the audience to view, while maintaining operation of the computer's internal LCD display for the computer operator to view.

To achieve SimulSCAN operation, the CL-GD6410 provides separate CRT and LCD display data output paths. Resolution mapping logic converts the various CRT resolutions to the fixed resolution of the LCD. Clock management logic converts the CRT timing to LCD timing. The CL-GD6410 is able to provide clock signals at different rates to two displays simultaneously.

Today's most popular monochrome STN (Super Twist Nematic) LCD panels are of dual-panel construction. It is a considerable design challenge to reconcile the single-scan format of the CRT with the dual-scan format required by the LCD. The Frame-Accelerator technology of the CL-GD6410 buffers one-half of a frame, alternating between the lower-panel half-frame and upper-panel half-frame of the LCD. In this manner, the controller's direct-output operates as though it is driving a single-scan display, with the frame accelerator driving the half-frame that lags (or leads) the direct-output frame.

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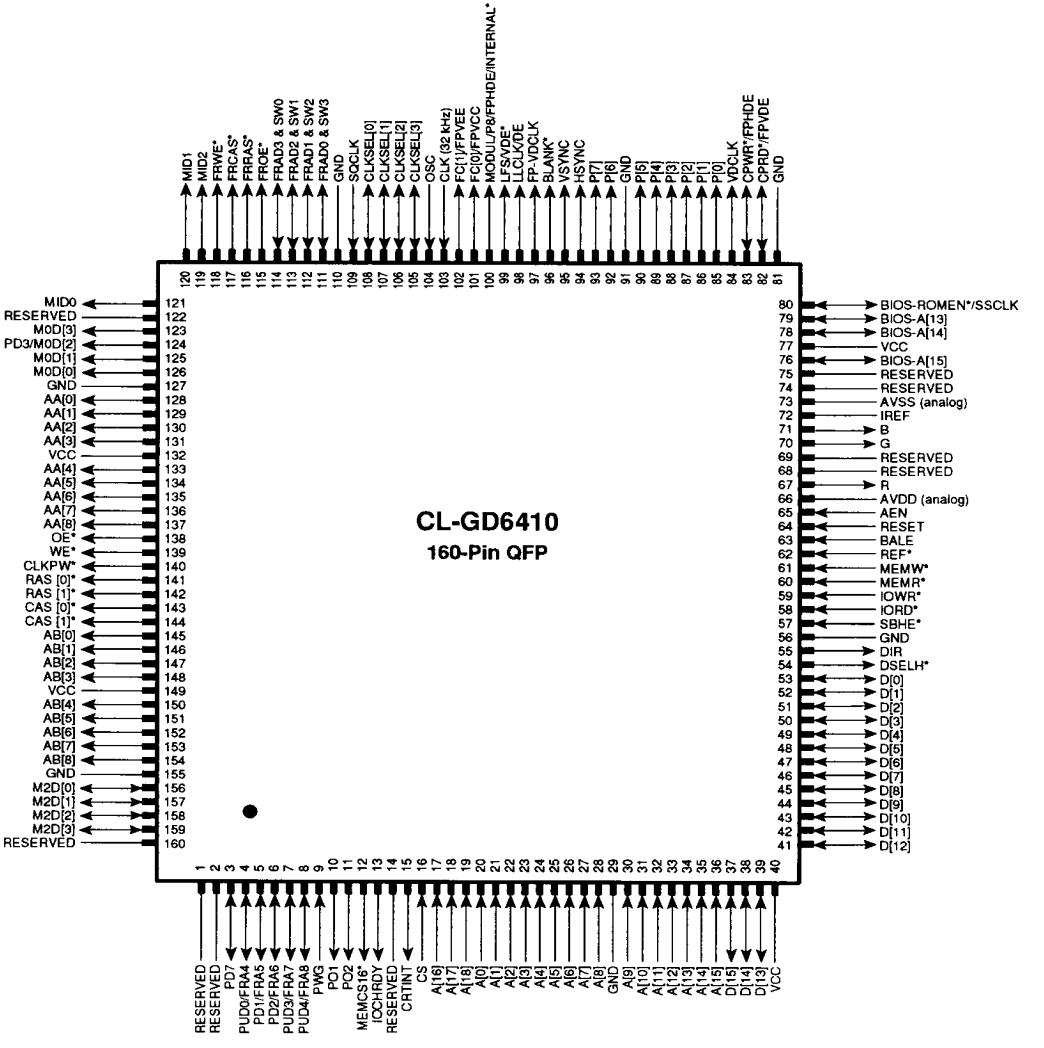
1. PIN INFORMATION

The CL-GD6410 is available in a 160-pin quad flat pack device configuration, shown below.

1.1 Pin Diagram



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2. PIN ASSIGNMENTS

The following conventions are used in the pin assignment table: (I) indicates input; (O) indicates output; (TO) indicates tristate output; (AO) indicates analog output; (AI) indicates analog input; (PW) indicates power; (*) denotes a negative-true (active-low) signal.

2.1 Pin Assignment Table

Name	Pin No.	Type	Description
CS	16	I	**CHIP SELECT**: When high, this indicates that the CL-GD6410 is selected for memory accesses.
A[18:16], A[15:9], A[8:0]	19:17 36:30, 28:20	I	**CPU ADDRESS INPUTS.**
D[15:0]	37:39 41:53	I/O	**CPU DATA I/O.**
DSELH*	54	O	**DATA SELECT HIGH BYTE**: This enables the CPU data bus upper-byte buffer when needed.
DIR	55	O	**CPU DATA BUS BUFFER DIRECTION**: When low, this indicates a CPU read. (DIR is used only when CPU data has to be buffered).
SBHE*	57	I	**BYTE HIGH ENABLE**: This signal is sampled only if 16-Bit Mode is enabled; otherwise, 8-bit bus operations are assumed.
IORD*	58	I	**I/O READ**: This indicates that an I/O read cycle is occurring.
IOWR*	59	I	**I/O WRITE**: This indicates that an I/O write cycle is occurring.
MEMR*	60	I	**MEMORY READ**: This indicates that a memory read cycle is occurring.
MEMW*	61	I	**MEMORY WRITE**: This indicates that a memory write cycle is taking place.
REF*	62	I	**REFRESH**: This indicates a memory-refresh cycle and will cause the CL-GD6410 to ignore memory accesses on the bus.
BALE	63	I	**ADDRESS LATCH ENABLE**: A high indicates a valid memory address.

2.1 Pin Assignment Table *(cont.)*

Name	Pin No.	Type	Description
RESET	64	I	**SYSTEM RESET**: This input is normally connected to the System Reset Bus Signal and is used as a hardware reset signal for the CL-GD6410.
AEN	65	I	**ADDRESS ENABLE**: This is a host CPU Bus Signal that distinguishes between DMA and non-DMA Bus Cycles. The signal is high for a DMA Cycle, and it will cause the CL-GD6410 to ignore IORD* and IOWR*.
MEMCS16*	12	TO	This output is an acknowledge for 16-bit-wide accesses and is generated by the CL-GD6410 only if the 16-Bit Peripheral Mode is enabled and a valid memory-address range has been decoded.
IOCHRDY	13	TO	This signal is driven low to lengthen memory cycles.
CRTINT	15	TO	Indicates the start of a vertical retrace, normally connected to one of the interrupt inputs on the PC Bus. It is enabled by clearing Bit 5 of the Vertical Retrace End Register and disabled by clearing Bit 4 of the Vertical Retrace End Register. When enabled, the CRTINT Pin will go high at the start of the vertical retrace interval, and remain high until cleared by a write of '0' to Bit 4 of the Vertical Retrace End Register (CR11). CRTINT is enabled by: *Clearing Bit 5 of CR11* *Setting Bit 4 of CR11* If Bit 4 is not reset to a '1' after clearing the initial CRTINT, interrupts will cease. This feature greatly simplifies the task of OR'ing in the proper value for the remaining bits of the CR11 Register (this is not the case for an IBM® EGA or VGA controller). CRTINT may be programmed for the AT Bus, or a direct-interrupt controller interface.
AA[8:4] AA[3:0]	137:133 131:128	O	**VIDEO MEMORY 'A' ADDRESS BUS**: This bus contains the row/column address information required by the DRAMs in Video Memory Planes 0 and 1. This bus carries different addresses than the 'AB' Bus in text modes.
AB[8:4] AB[3:0]	154:150 148:145	O	**VIDEO MEMORY 'B' ADDRESS BUS**: This bus contains the row/column address information required by the DRAMs in Video Memory Planes 2 and 3. This bus carries different addresses than the 'AA' Bus in text modes.

2.1 Pin Assignment Table *(cont.)*

Name	Pin No.	Type	Description
OE*	138	O	**VIDEO MEMORY OUTPUT ENABLE**, active low.
WE*	139	O	**VIDEO MEMORY WRITE ENABLE**.
CLKPW*	140	O	**CLOCK CHIP POWER CONTROL**, active low, can be used to control external transistor logic connected to clock synthesizer power pins. This signal is active in Suspend Mode.
RAS*[1:0]	142:141	O	**VIDEO MEMORY RAS**: RAS*[0] to AA Bus, RAS*[1] to AB Bus.
CAS*[1:0]	144:143	O	**VIDEO MEMORY CAS**: CAS*[0] to AA Bus, CAS[*1] to AB Bus.
M0D[3], M0D[1:0], M0D[2]/PD3	123:126	I/O	**VIDEO MEMORY DATA PINS**, Planes 0 and 1, Bits 3:0. MOD[2] is multiplexed with PD3.
MID[2:0]	119:121	I	**MONITOR ID**, Bits 2:0. This pin is sampled on reset or under software control.
M2D[3:0]	159:156	I/O	**VIDEO MEMORY DATA PINS**, Planes 1 and 2, Bits 3:0.
PD7	3	I	**CONFIGURATION PULL-DOWN 7**.
FRWE*	118	O	**FRAME-ACCELERATOR WRITE ENABLE**.
FRCAS *	117	O	**FRAME-ACCELERATOR CAS**.
FRRAS*	116	O	**FRAME-ACCELERATOR RAS**.
FROE*	115	O	**FRAME-ACCELERATOR OE**.
FRAD3 & SW0	114	I/O	**FRAME-ACCELERATOR MULTIPLEXED ADDRESS/ DATA[3]** multiplexed with Switch 0.
FRAD2 & SW1	113	I/O	**FRAME-ACCELERATOR MULTIPLEXED ADDRESS/ DATA[2]** multiplexed with Switch 1.
FRAD1 & SW2	112	I/O	**FRAME-ACCELERATOR MULTIPLEXED ADDRESS/ DATA[1]** multiplexed with Switch 2.
FRAD0 & SW3	111	I/O	**FRAME-ACCELERATOR MULTIPLEXED ADDRESS/ DATA[0]** multiplexed with Switch 3.

2.1 Pin Assignment Table *(cont.)*

NAME	PIN NO.	TYPE	DESCRIPTION
FRA4 & PUD0	4	I/O	**FRAME-ACCELERATOR ADDRESS [4]** multiplexed with Pull-Up or Pull-Down 0.
FRA5 & PD1	5	I/O	**FRAME-ACCELERATOR ADDRESS [5]** multiplexed with Pull-Down 1.
FRA6 & PD2	6	I/O	**FRAME-ACCELERATOR ADDRESS [6]** multiplexed with Pull-Down 2.
FRA7 & PUD3	7	I/O	**FRAME-ACCELERATOR ADDRESS [7]** multiplexed with Pull-Up or Pull-Down 3.
FRA8 & PUD4	8	I/O	**FRAME-ACCELERATOR ADDRESS [8]** multiplexed with Pull-Up or Pull-Down 4.
PWG	9	I	**POWER GOOD INPUT**: This signal initiates flat panel power sequencing when power is applied or is removed from the CL-GD6410.
PO1	10	O	**PROGRAMMABLE OUTPUT 1.**
PO2	11	O	**PROGRAMMABLE OUTPUT 2.**
CPRD*/FPVDE	82	I/O	**COLOR PALETTE (RAMDAC) READ** if external RAMDAC configuration, or **FLAT-PANEL VERTICAL DISPLAY ENABLE** for special panels.
CPWR*/FPHDE	83	I/O	**COLOR PALETTE (RAMDAC) WRITE** if external RAMDAC configuration, or **FLAT-PANEL HORIZONTAL DISPLAY ENABLE** for special panels.
VDCLK	84	O	**VIDEO CLOCK**: This is the output for the external RAMDAC or color panel.
P[0:7]	85:90 92:93	O	**VIDEO DATA OUT** if external RAMDAC configuration and pixel-data output for flat panels.
HSYNC	94	O	**HORIZONTAL SYNC** to CRT Monitor.
VSYNC	95	O	**VERTICAL SYNC** to CRT Monitor.
BLANK*	96	O	**BLANK OUTPUT** if external RAMDAC configuration; I/O if on-chip RAMDAC configuration.

2.1 Pin Assignment Table *(cont.)*

Name	Pin No.	Type	Description
FPVDCLK	97	O	**FLAT-PANEL VIDEO CLOCK.**
LLCLK/DE	98	O	**FLAT-PANEL LINE CLOCK**: This is used to increment Row Shift Registers within LCD panels or display enable if the CL-GD6410 is used with the CL-GD6340.
LFS	99	O	**LCD FRAME START PULSE**: This indicates the start of a new frame on flat panels.
MODUL/P8/FPHDE INTERNAL*	100	O	**LCD PANEL MODULATION SIGNAL**: This is required for LCD panels that do not drive the function themselves. INTERNAL* is a programmable output. P8 is needed for 512-color LCD panels. FPHDE is needed as an alternate for Pin 83.
FC[0]/FPVCC	101	O	**FEATURE CONNECTOR PROGRAMMABLE I/O BIT [0]** or LCD panel 5V control.
FC[1]/FPVEE	102	O	**FEATURE CONNECTOR PROGRAMMABLE I/O BIT [1]** or LCD panel back-light power control.
CLK32K	103	I	**32-kHz CLOCK**: The input is used both for slow timers and in Suspend Mode. This input is required.
OSC	104	I	**CLOCK-IN**: This is an input from a multifrequency clock source or 14.318-MHz crystal.
CLKSEL[3:0]	105:108	I/O	**CLOCK SELECT**: These are inputs from external oscillators or outputs to a multifrequency synthesizer.
SQCLK	109	I	**VIDEO MEMORY SEQUENCER CLOCK.**
R	67	AO	**ANALOG RED.**
G	70	AO	**ANALOG GREEN.**
B	71	AO	**ANALOG BLUE.**
BIOS-A[13:15]	79, 78, 76	O	**BIOS ADDRESS 13-15.**
BIOS-ROMEN*/SSCLK	80	I/O	**BIOS-ROM ENABLE**: This is used to enable C000 BIOS ROM if the CL-GD6410 is used in an adapter card application. **SCREEN-SAVE CLOCK**: This input is used to detect keyboard activity for Standby Mode in E000 motherboard applications.

2.1 Pin Assignment Table *(cont.)*

Name	Pin No.	Type	Description
IREF	72	AI	**RAMDAC CURRENT REFERENCE.**
AVSS	73	PW	**RAMDAC ANALOG V_{SS}.**
AVDD	66	PW	**RAMDAC ANALOG V_{DD}.**
V_{CC}	40, 77 132, 149	PW	**V_{CC} PINS.**
GND	127, 155, 56, 29, 81, 91, 110	PW	**GND PINS.**

3. FUNCTIONAL DESCRIPTION

3.1 Functional Operation

The CL-GD6410 interfaces with the host processor, video memory, display device, and other external I/O. The host memory interface may be either 8- or 16-bit. Video memory interface is optimized for 256K bytes. The CL-GD6410 is AT bus-compatible to 10 MHz. Because the CL-GD6410 has a demultiplexed address and data bus, most systems will be able to interface it directly — without the addition of bus-interface buffers.

Flat-panel display devices supported will typically be 640 x 480-resolution monochrome STN or color TFT LCD panels. These panels are supported by a direct interface, precluding the need for buffers. Different-resolution displays can be used if the VGA BIOS is modified to support non-standard panel resolutions. Direct-power sequencing is supported for panels that require it.

CRT displays supported are PS/2™ VGA-compatible analog monitors, including the IBM 85XX families, and multifrequency analog monitors, including the NEC® Multisync™ families. The CL-GD6410 also interfaces with the Cirrus Logic CL-GD6340 Color LCD Interface Controller for the best possible color support on a wide variety of color panels.

A PS/2-compatible RAMDAC, necessary to accomplish a VGA design, is built into the CL-GD6410. This allows savings in both power consumption and space requirements. The RAMDAC is fully compatible, and is fully supported by the CL-GD6410 enhanced power-management features.

The four major operations supported by the CL-GD6410 are:

- ***Host Access to CL-GD6410 Registers***
- ***Host Access to Video Memory***
- ***Memory Refresh***
- ***Display Refresh***

Host Access to Registers

The host processor is typically a minimum 8088- or 80X86-type microprocessor in a PC/XT/AT bus-compatible environment and can access the CL-GD6410 Registers by setting up a 24-bit address and generating IORD*, IOWR, MEMR* and MEMW* Signals. Memory reads and writes can be 8- or 16-bit; I/O reads and writes are 8-bit.

DRAM and screen-refresh activities occur concurrently and independently. The registers that may be accessed by the host are listed in Section 4. They include all of the standard VGA registers.

All registers have been made host-readable and writable to allow BIOS and driver software to determine the state of the video controller, allowing it to be readily switched and restored in multi-tasking and windowing environments.

Host Access to Video Memory

Host access to video memory is channeled via the CL-GD6410. The host must establish the proper address/data/timing parameters in the CL-GD6410 Registers to transfer to and from video memory.

The CL-GD6410 also contains an intelligent sequencer that allocates Video Memory Cycles not only to the host, but also to the DRAM Refresh and the Display CRT Controllers.

Memory Refresh

Memory bandwidth is allocated to each process according to the actual real-time needs of the process, ensuring efficient use of the available bandwidth. In the case of a CRT display device, the display is blanked during horizontal and vertical-retrace intervals, opening memory bandwidth for host access and/or memory refresh.

Unlike early VGA implementations that gave the host only 14% of memory cycles, the CL-GD6410 can give the host from 25-50% access to video memory, or one out of two memory cycles. This is largely due to the sequencing strategy.

Display Refresh

In bit-mapped graphics modes, and text modes, pixel data is latched into the CL-GD6410, transferred to Shift Registers, and shifted-out upon translation through the CL-GD6410 self-contained color-palette registers and RAMDAC.

The CL-GD6410 tracks the active and unused areas of the screen and cursor positions and consequently supplies screen control signals: VSYNC, HSYNC, and BLANK*.

When the CL-GD6410 is connected to a dual-scan LCD display, an additional 64K x 4 DRAM is needed. The Frame-Accelerator is used for split-panel data formatting. The reconstituted data from the Frame-Accelerator and video memory is then supplied in parallel to the LCD 4-bit upper and lower panel data buses. This technique not only maintains display contrast, but also reduces the power consumption of the video circuitry. The panel-frame rate is twice the rate that the data is fetched from video memory.

3.2 CRT Display Modes

The CL-GD6410 includes all registers and data paths required for VGA compatibility. VGA enhancements include 16 simultaneously loadable text fonts (twice the capability of IBM VGA), and readable registers.

Extended graphics resolutions beyond the 640 x 480 IBM VGA standard are available. Using multiple-frequency monitors, such as the NEC MultiSync or Sony® MultiScan™, 800 x 600 Mode with a 4:3 aspect ratio can be displayed.

High-resolution text modes offer from 100 columns by 30 rows up to 132 columns by 60 rows. 100 columns by 30 rows can be displayed on 640 x 480 flat panels.

3.3 Flat Panel Display Modes

The CL-GD6410 will directly drive all of the popular monochrome dual-panel/dual-scan LCD panels. Proprietary techniques minimize flicker, noise, and pattern motion while enhancing contrast within the grayscales being used.

Grayscaling is accomplished by modulating the ON-to-OFF time of individual pixels in the panel, and allowing the eye to integrate the superposed pixels to 16-perceptible grayscales. Flicker is eliminated by proprietary techniques involving distribution of time between ON and OFF pixels during frame modulation.

The CL-GD6410 allows the full spectrum of PC applications written for analog monitors and various video modes to run on standard 640 x 480 flat panels. This is accomplished through color emulation, attribute remapping, and resolution mapping.

In addition, summing circuitry allows rapid generation of IBM-compatible grayscale equivalents of color images. Up to 64 grayscale levels are available by using proprietary two-dimensional stippling logic. This technique permits all applications that generate monochrome, 4-, 16-, or 256-color images to be run on a monochrome flat-panel display.

Cirrus Logic AutoMap™ Logic can map 256 colors into a monochrome image; the colors then appear in 64 shades. The hardware-based algorithm tracks the particular palette map being used by the internal RAMDAC. RAMDAC data may be stored, as desired by the application, in orderly or random sequences. Realistic renditions of color images are not affected.

In color-text modes, foreground and background attributes can be automatically remapped to black and white for maximum contrast. Positive or negative raster may be selected under program control to match the visual qualities of the display and/or needs of the application.

The video resolutions that an application has selected are remapped to a flat panel according to whether Compatibility Mode, Compression Mode, or Expanded Mode was selected.

3.4 Intelligent Power Management and Sequencing

Notebook and laptop PCs have stringent power limitations due to battery operation and heat dissipation. To meet these needs, the CL-GD6410 is manufactured using low-power CMOS technology. In addition, the CL-GD6410 has programmable output pins as well as other intelligent power management features that permit the controller to enter four possible power-conserving modes, which are discussed below:

Normal Mode

- Power to LCD panel and full screen refresh
- CPU access to Video Memory
- Refresh to Video Memory
- CPU access to RAMDAC
- CPU access to I/O Registers

Since power consumption is directly proportional to the frequency at which the controller is run, the CL-GD6410 uses a proprietary Frame-Accelerator to maintain the maximum screen refresh rate, while the clock to the CL-GD6410 functions at 25 MHz or less. The Frame-Accelerator is used only with dual-scan LCD panels.

Standby Mode

- No power to LCD panel and no screen refresh
- Panel power sequencing is observed
- CPU access to Video Memory
- Refresh to Video Memory
- CPU access to RAMDAC
- CPU access to I/O Registers
- Frequency Synthesizer is not powered-down

The primary power savings in this mode comes from reducing power to the LCD panel only. Since there is no screen refresh, normal clock rates are not required and may be replaced by slower clock rates to further reduce power consumption. The input pin SSCLK (Screen-Save-Clock) detects any keyboard activity. Any RAMDAC I/O can be executed. The system will recover from Standby Mode after receiving stimuli in the form of video memory read or write accesses, or the presence of the SSCLK Signal. If power sequencing is in progress, then the CL-GD6410 will allow the sequencing to complete before exiting from Standby Mode.

The CL-GD6410 contains a power-save timer that allows it to be programmable, in increments of 1 minute, up to 63 minutes. If the feature is enabled, this is the time-out time from the last stimuli to automatically switch to Standby Mode. The timer can be activated by either the SSCLK Signal or by CPU memory access (read or write).

Suspend Mode

- No power to LCD panel and no screen refresh
- Panel power sequencing is observed
- No CPU access to Video Memory
- Refresh to Video Memory continues but using a 32-kHz clock
- No CPU access to RAMDAC
- No CPU access to I/O Registers
- Frequency Synthesizer is powered-down

The power savings in this mode occurs because host access to video memory is now denied and a slower clock is used. This slow clock refreshes video memory by performing CAS*-before-RAS* refresh. With slow-refresh DRAM, a clock running as slow as 32 kHz can be used. Other than this refresh logic, the rest of the CL-GD6410 does not have clocks, reducing power consumption even further.

Suspend Mode can be activated or deactivated, under program control, by a sequence of three consecutive I/O writes to the 'active' IBM VGA-compatible 'Sleep' Port (46E8H or 3C3H).

Shutdown

- No power to LCD panel

Prior to initiating a system-wide shutdown, the video-subsystem state can be saved by the system itself for later restoration. The CL-GD6410 allows the system to save or restore the status of all Controller Registers.

The CL-GD6410 can operate at 5V ± 10%. With this range, a substantial power savings can be realized by designing for 4.5V operation.

Several dedicated pins have been assigned to facilitate power management. The PWG Signal (Power Good) can be used to signify the beginning of a power-on or power-off sequence. The FPVCC and FPVEE Signals can be used to control panel logic power and panel backlight/contrast, when a panel requires that these functions be sequenced or controlled.

3.5 Internal RAMDAC

The CL-GD6410 includes an on-chip, high-speed, memory digital-to-analog converter known as a RAMDAC. The RAMDAC circuitry helps the CL-GD6410 process color-video signals and timing information to the display.

The RAMDAC includes a 256-entry by 18-bit word color lookup table, three 6-bit digital-to-analog converters (DACs), a Pixel Mask Register, and a Border Color Register.

An 8-bit address value applied on the Pixel Address Inputs defines the memory location for reading an 18-bit color data word from the color lookup table. This data is partitioned as three fields of six bits each — one for R, one for G, and one for B — and then applied to the individual DAC Inputs.

A pixel word mask is incorporated to allow the incoming pixel address to be altered, permitting changes to the color lookup table contents to be made immediately. This feature allows special display operations such as flashing objects and overlays to be created.

The color lookup table contents are accessed via its 8-bit-wide host interface. An internal synchronizing circuit allows the color value accesses to be completely asynchronous to the pixel video operation.

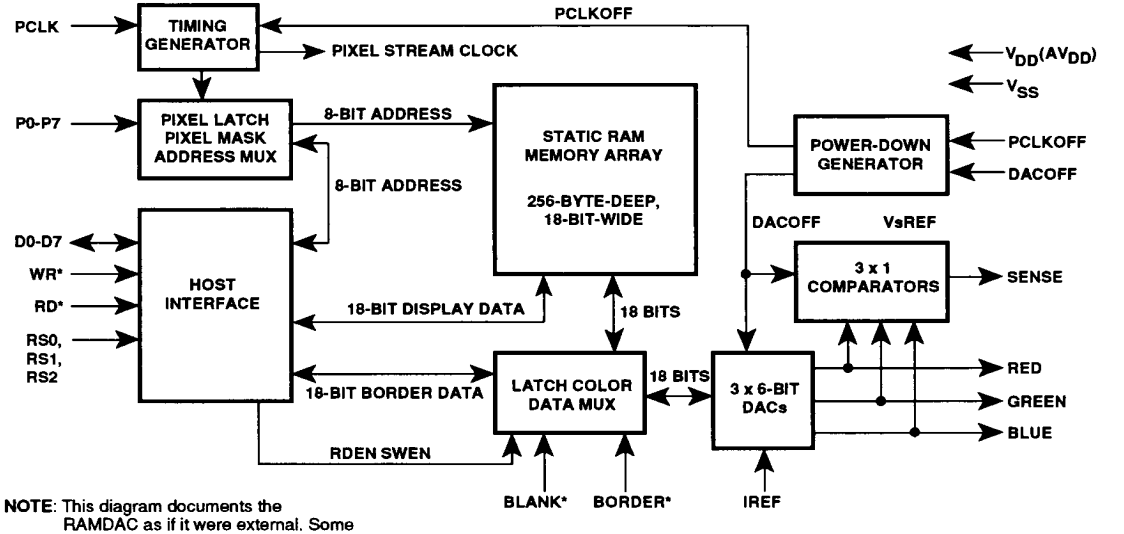


Figure 3–1. RAMDAC Block Diagram

RAMDAC Video Operation

In video operation, pixel addresses P0 through P7, BLANK* and BORDER* are sampled on the rising edge of the Pixel Clock (PCLK). Their effect appears at the DAC Outputs after three further rising edges of PCLK.

Both BLANK* and BORDER* are active-low signals. When the BLANK* Input is low, a binary 0 is applied to the DAC Inputs, producing a zero-volt DAC Output. When the BORDER* Input is low, the color data from the Border Color Register is applied to the DAC Inputs.

The DACOFF* Input is both a display disable control and a DAC power-down control. When DACOFF* is low, the DACs in the RAMDAC are totally inoperative, which results in the power dissipation being reduced to standby minimum. During this time, the three DAC Outputs are at a zero-volt level. When DACOFF* goes high, several PCLK Cycles are required before the DACs in the RAMDAC will function properly.

Analog Outputs

The DAC outputs are designed to produce 0.7-volt peak white amplitude with a reference current (I_{REF}) of 6.7 mA when driving a doubly-terminated 75-ohm load, which corresponds to an effective DAC Output load of 37.5 ohms ($R_{effective}$).

For all values of I_{REF} and output loading:

$V_{blacklevel}$ = 0 volts

Writing to the Color Lookup Table

To write a color definition to the lookup table, a value specifying an address location in the lookup table is first written to the Write Mode Address Register. The color values for the red, green, and blue intensities are then written in succession to the Color Value Register. After the blue data is latched, this new color data is then written into the lookup table at the defined address, and the Address Register is incremented automatically.

Since Address Register increments after each transfer of data to the lookup table, it is best to write a set of consecutive locations at once. The start address of the set of locations is first written to the Write Address Mode Register. The color data for each address location is then sequentially written to the Color Value Register. The RAMDAC automatically writes data to the lookup table, and increments the Address Register after each host transfer of three bytes of color data.

Reading from the Color Lookup Table

To read color data from the lookup table, a value specifying the address location of the data is written to the Read Mode Address Register. After the address is latched, the data from this location is automatically read out to the Color Value Register, and the Address Register automatically increments.

The color intensity values are then read from the Color Value Register by the sequence of three read (RD*) commands. After the blue value is transferred out, new data is read from the lookup table at the current address to the Color Value Register, and the Address Register to automatically increment again.

If the Address Register is loaded with a new starting address while an unfinished sequence is in progress, the system resets and starts a new sequence. This occurs for both read and write operations.

3.6 CL-GD6410 Configuration

The CL-GD6410 provides several configuration options. These options are set by installing 'pull-up' or 'pull-down' resistors on certain CL-GD6410 pins that are sampled at system reset.

NOTE: The CL-GD6410-A needs configuration resistors to establish either 'high' or 'low' conditions. The CL-GD6410-B has internal pull-down resistors; it requires pull-up resistors to establish other than default (low) values.

The configurations need to be made only once. All listed connections are required.

Pin Name (and No.)	Function	Notes
M0D[2]/PD3 (124)	Reserved	Low to maintain compatibility with future CL-GD64XX VGA controllers. (Only needs to be set on the CL-GD6410-A.)
FRA5/PD1 (5)	Reserved	Low to maintain compatibility with future CL-GD64XX VGA controllers. (Only needs to be set on the CL-GD6410-A.)
FRA4/PUD0 (4)	BIOS Support High = BIOS @ C000; Low = E000	Low for motherboard implementations when the desired BIOS is at E000. Pull high for adapter implementations or when the BIOS is at C000.
FRA6/PD2 (6)	VGA Address Space High = Yxx (I/O)/Yxxx (memory) Low = 3xx (I/O)/Axxx (memory)	Low in most cases. Pulling high allows for a non-DOS environment.
FRA7/PUD3 (7)	Sleep Mode I/O Address High = 46E8h; Low = 3C3h	Normally high for adapter controller implementations; low for motherboard implementations.
FRA8/PUD4 (8)	BIOS Width Select High = 16-bit BIOS; Low = 8-bit	Defines BIOS-to-controller interface.
PD7 (3)	DIR Configuration High = Reserved; Low = DIR	When buffers are required by the design, then this signal should be pulled low to allow Pin 55 to control buffer devices.
FRAD0/SW3 (111) and FRAD1/SW2 (112)	Reserved	No connection required.
FRAD2/SW1 (113) and FRAD3/SW0 (114)	Panel Class	**SW1** **SW0** **Panel Class** 0 0 0 0 1 1 1 0 2 1 1 3

4. VIDEO MODES

4.1 CRT Video Modes

Table 4–1. IBM® Standard VGA Video Modes

Mode No.	Number of Colors	Char. x Row	Char. Cell	Screen Format	Display Mode	Dot Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	Monitor Supported
0, 1	16/256K	40 x 25	9 x 16	360 x 400	Text	28	31.5	70	All
2, 3	16/256K	80 x 25	9 x 16	720 x 400	Text	28	31.5	70	All
4, 5	4/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70	All
6	2/256K	80 x 25	8 x 8	640 x 200	Graphics	25	31.5	70	All
7	Mono.	80 x 25	9 x 16	720 x 400	Text	28	31.5	70	All
d	16/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70	All
e	16/256K	80 x 25	8 x 14	640 x 200	Graphics	25	31.5	70	All
f	Mono.	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70	All
10	16/256K	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70	All
11	2/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60	All
12	16/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60	All
13	256/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70	All

Table 4–2. Cirrus Logic Extended CRT Video Modes

Mode No.	Number of Colors	Char. x Row	Char. Cell	Screen Format	Display Mode	Dot Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	Monitor Supported
41	16/256K	100 x 50	8 x 8	800 x 400	Text	32	31.5	60	All
42	16/256K	100 x 60	8 x 8	800 x 480	Text	32	31.5	70	All
43	16/256K	100 x 25	8 x 16	800 x 400	Text	32	31.5	60	All
51	16/256K	132 x 50	8 x 8	1056 x 400	Text	32	25	60	Multifrequency
52	16/256K	132 x 60	8 x 8	1056 x 480	Text	32	25	50	Multifrequency
53	16/256K	80 x 60	8 x 8	640 x 480	Text	25	31.5	60	All
54	16/256K	132 x 25	8 x 16	1056 x 400	Text	32	25	60	Multifrequency
64, 6a	16/256K	100 x 37	8 x 16	800 x 600	Graphics	32	31.5	53	Multifrequency

4.2 LCD Video Modes

Table 4–3. IBM Standard VGA Video Modes

Mode No.	Mono. STN Number of Shades	Color TFT Number of Colors	CRT Number of Colors	Char. x Row	Char. Cell	Screen Format	Expanded Char. Cell	Expanded Size	Display Mode
0, 1	16/16	16/185K	16/256K	40 x 25	9 x 16	360 x 400	16 x 19	640 x 475	Text
2, 3	16/16	16/185K	16/256K	80 x 25	9 x 16	720 x 400	8 x 16	640 x 475	Text
4, 5	4/64	4/185K	4/256K	40 x 25	8 x 8	320 x 200	NA	640 x 475	Graphics
6	2/16	2/185K	2/256K	80 x 25	8 x 8	640 x 200	NA	640 x 475	Graphics
7	2/16	2/185K	Mono.	80 x 25	9 x 16	720 x 400	8 x 19	640 x 475	Text
d	16/64	16/185K	16/256K	40 x 25	8 x 8	320 x 200	NA	640 x 475	Graphics
e	16/16	16/185K	16/256K	80 x 25	8 x 14	640 x 200	NA	640 x 475	Graphics
f	2/16	2/185K	Mono.	80 x 25	8 x 14	640 x 350	NA	640 x 475	Graphics
10	16/16	16/185K	16/256K	80 x 25	8 x 14	640 x 350	NA	640 x 475	Graphics
11	2/16	2/185K	2/256K	80 x 25	8 x 16	640 x 480	NA	640 x 480	Graphics
12	16/16	16/185K	16/256K	80 x 25	8 x 16	640 x 480	NA	640 x 480	Graphics
13	64/64	256/185K	256/256K	40 x 25	8 x 8	320 x 200	NA	640 x 475	Graphics

Table 4–4. Cirrus Logic Extended LCD Video Mode

Mode No.	Mono. STN Number of Shades	Color TFT Number of Colors	CRT Number of Colors	Char. x Row	Char. Cell	Screen Format	Expanded Char. Cell	Expanded Size	Display Mode
63	16/16	16/185K	16/256K	80 x 60	8 x 8	640 x 480	8 x 8	640 x 480	Text

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Ambient temperature under bias ..... 0° C to 70° C
Storage temperature ..... -65° C to 150° C
Voltage on any pin with respect to ground ..... -0.5 to V_{CC} + 0.5 Volts
Operating power dissipation ..... 1 Watt
Standby power dissipation ..... 0.1 Watt
Suspend power dissipation ..... 0.02 Watt
Power supply voltage ..... 7 Volts
Injection current (latch-up) ..... 25 mA

NOTE: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

5.2 CL-GD6410 DC Specifications (Digital)

(V_{CC} = 5V ± 10%; T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions
V_{CC}	Power Supply Voltage	4.50	5.50	V	Normal Operation
V_{IL}	Input Low Voltage	0	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{IHC}	Input High Voltage CMOS	3.0	V_{CC} - 0.7	V	
V_{ILC}	Input Low Voltage CMOS		0.6	V	
V_{OHC}	Output High Voltage CMOS	3.5		V	I_{OHC} = -200 µA
V_{OLC}	Output Low Voltage CMOS		0.4	V	I_{OLC} = 3.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OHC} = -200 µA
V_{OL}	Output Low Voltage		0.5	V	I_{OLC} = 3.2 mA
I_{CC}	Operating Supply Current		180	mA	5V nominal SimulSCAN
I_L	Input Leakage	-10	10	µA	$0 < V_{IN} < V_{CC}$
I_{OZ}	Input Leakage	-10	10	µA	$0 < V_{IN} < V_{CC}$
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	

NOTES:

1) I_{OL} MAX for IOCHRDY, MEMCS16* = 24 mA.
   I_{OL} MAX for CRTINT = 12 mA.
   I_{OL} MAX for CPU DATA, DIR, WE*, CAS* = 8 mA.
   I_{OL} MAX for LCD Control Signals = 4 mA (LCD Control Signals = FPVDCLK, LLCLK, MOD, and LFS).
2) I_{CCpd} — The actual current in Power Down Modes will vary depending on the implementation of the system environment. For information on system implementation of Power Down Modes, refer to application notes.

5.3 CL-GD6410 DC Specifications (RAMDAC)

(V_{CC} = 5V ± 10%; TA = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions
V_{CC}/AV_{DD}	Power Supply Voltage	4.50	5.50	V	Normal Operations
I_{REF}	DAC Reference Current	-6.7	-10	mA	Notes 1 and 2
I_{DD}	Operating Supply Current		100	mA	Note 3

NOTES:

1) Reference currents below the minimum specified may cause the analog output to become invalid.
2) The pixel clock frequency must be stable for a period of 20 µs after power-up before proper device operation.
3) I_{DD} is dependent upon the digital output loading and pixel clock rate. The value specified is with the outputs unloaded and the pixel clock frequency equal to 32 MHz.

5.4 DAC Characteristics

Symbol	Parameter	MIN	MAX	Units	Conditions
R	Resolution	6		Bits	
Vomax	Output Voltage		0.75	V	IO < 10 mA
Iomax	Output Current		-21	mA	Vo < 1V
tr	Rise Time		8	ns	Note 1
ts	Full-scale settling time		30	ns	Notes 1 and 2

NOTES:

1) Load = 37.5 ohms and 30 pF, and I_{REF} = -6.7 mA.
2) From a 2% change in output voltage until settling within 2% of the final value.

6. AC TIMING CHARACTERISTICS

This section includes system timing requirements for the CL-GD6410. Timings are provided in nanoseconds (ns), at TTL input levels, with the ambient temperature varying from 0° to 70° C, and V_{CC} varying from 4.50 to 5.50V DC. The AT-bus speed is10 MHz unless otherwise noted. Note that (*) denotes an active-low signal. Also note the following.

1. All timings assume a load of 50 pF.
2. TTL signals are measured at TTL threshold; CMOS signals are measured at CMOS threshold.
3. On power-up, all DRAM interface signals are inactive. Memory data bus is in Input Mode to sense values on configuration option pins set by pull-up or pull-down resistors.
4. The CL-GD6410 executes eight RAS*-only cycles to initialize DRAMs before executing normal cycles.

6.5 Index of Timing Information

Table 6–1. I/O Write Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{WAS}	Address to IOW* active setup	40		ns
t_{WDH}	Data hold time from IOW* inactive	0		ns
t_{WAH}	Address hold time from IOW* inactive	0		ns
t_{WDD}	Data delay from IOW* active		0	ns
t_{WP}	IOW* pulse width	320		ns
t_{WI}	IOW* inactive to any command	100		ns

NOTES:

1) AEN must be inactive (See Figure 6–16 for AEN timing).
2) See Figure 6–11 for DSELH* timing.
3) See Figure 6–8 for IOCHRDY* timing.

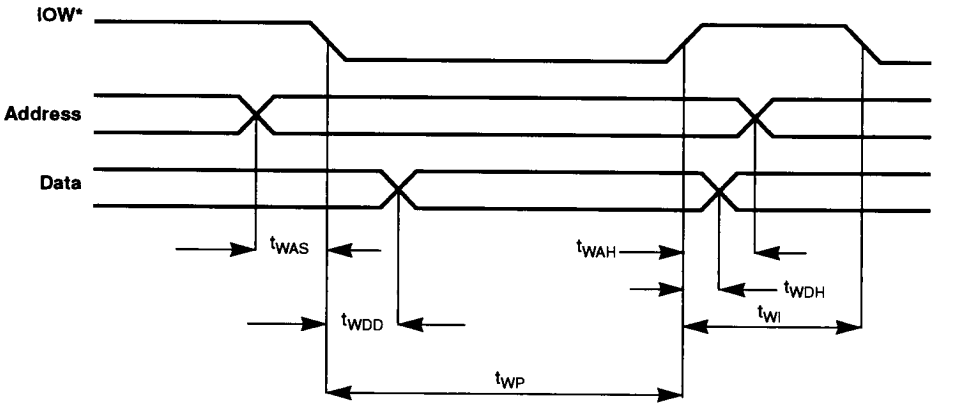


Figure 6–1. I/O Write Timing (ISA Bus)

Table 6–2. I/O Read Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{RRA}	Address setup to IOR* active	10		ns
t_{RDH}	Data hold time from IOR* inactive	0	30	ns
t_{RAH}	Address hold from IOR* inactive	0		ns
t_{RDD}	Data delay from IOR* active		220	ns
t_{RP}	IOR* pulse width	320		ns
t_{RZ}	IOR* active to data active delay	0		ns
t_{RTZ}	IOR* active to tristate delay		30	ns
t_{DDI}	Data delay from IOCHRDY active		25	ns

NOTES:
1) AEN must be inactive.
2) See Figure 6–12 for DSELH* and DIR timing.
3) See Figure 6–8 for IOCHRDY* timing.

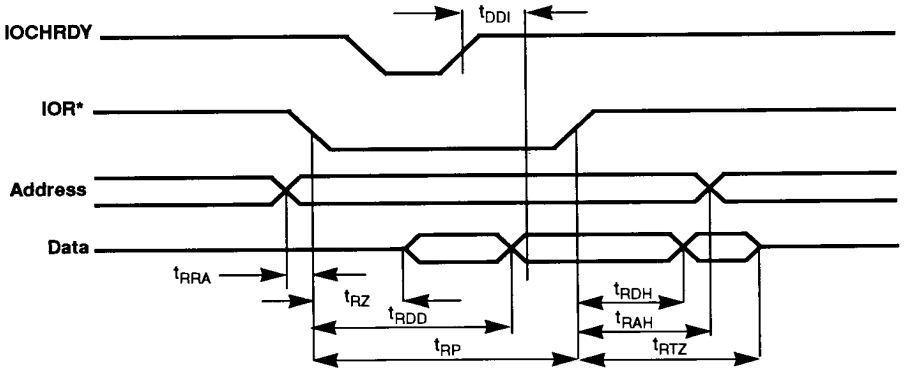


Figure 6–2. I/O Read Timing (ISA Bus)

Table 6–3. Memory Write Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{MWAS}	Address to MEMW* active setup	10		ns
t_{MWDH}	Data hold from MEMW* inactive	0		ns
t_{MWAH}	Address hold from MEMW* inactive	0		ns
t_{MWDD}	Data delay from MEMW* active		40	ns
t_{MWP}	MEMW* pulse width	155		ns
t_{MWI}	MEMW* to any command	100		ns

NOTES:

1) See Figure 6–12 for DSELH* timing.
2) See Figure 6–5 for MEMCS16* timing.
3) See Figure 6–7 for IOCHRDY timing.

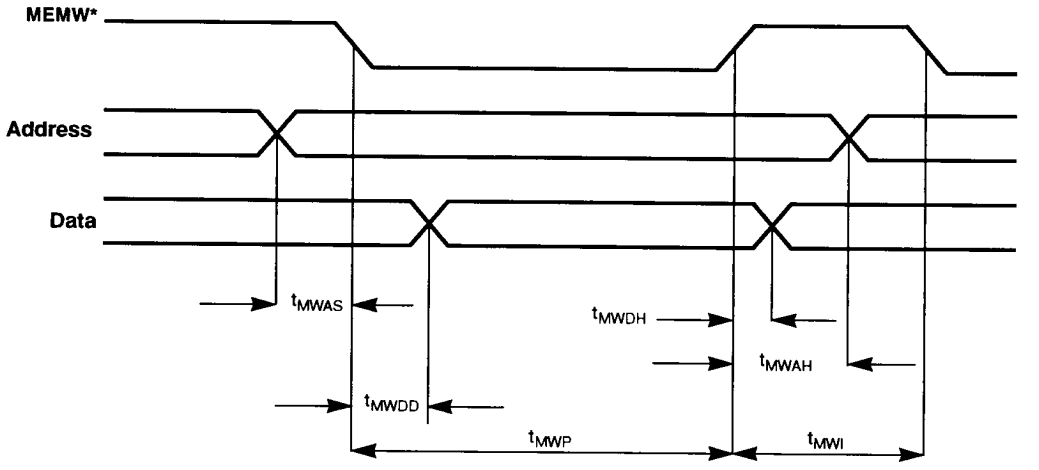


Figure 6–3. Memory Write Timing (ISA Bus)

Table 6–4. Memory Read Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{MRAS}	Address to MEMR* active	10		ns
t_{MRDH}	Data hold from MEMR* inactive	0	30	ns
t_{MRAH}	Address hold from MEMR* inactive	0		ns
t_{MRDI}	Data delay from IOCHRDY active		60	ns
t_{MRP}	MEMR* pulse width	375	2100	ns
t_{MRZ}	MEMR* active to data active delay	0		ns
t_{MRTZ}	MEMR* inactive to tristate delay		30	ns

NOTES:

1) See Figure 6–10 for DSELH* and DIR timing.
2) See Figure 6–5 for MEMCS16* timing.
3) See Figure 6–7 for IOCHRDY timing.

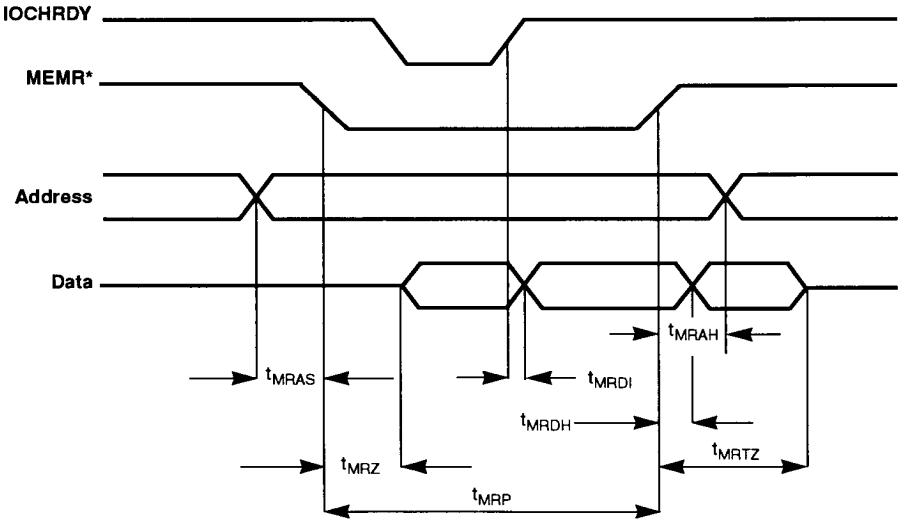


Figure 6–4. Memory Read Timing (ISA Bus)

Table 6–5. MEMCS16* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{MAD}	MEMCS16* active delay from address		60	ns
t_{MID}	MEMCS16* inactive delay from address		60	ns

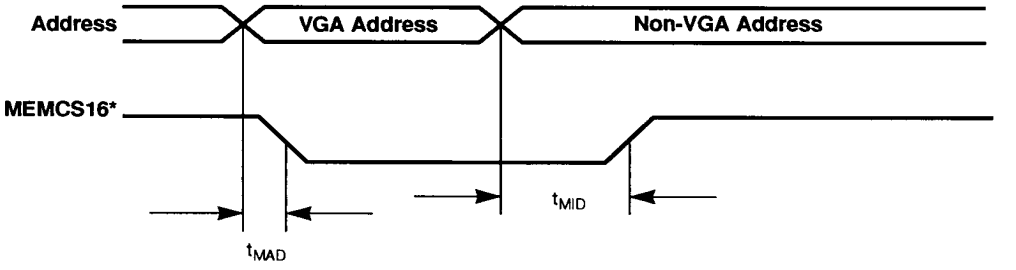


Figure 6–5. MEMCS16* Timing (ISA Bus)

Table 6–6. BALE Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{LAS}	Address setup to BALE	20		ns
t_{LBS}	SBHE* setup to BALE	20		ns
t_{LAH}	Address hold from BALE	20		ns
t_{LBH}	SBHE* hold from BALE	20		ns

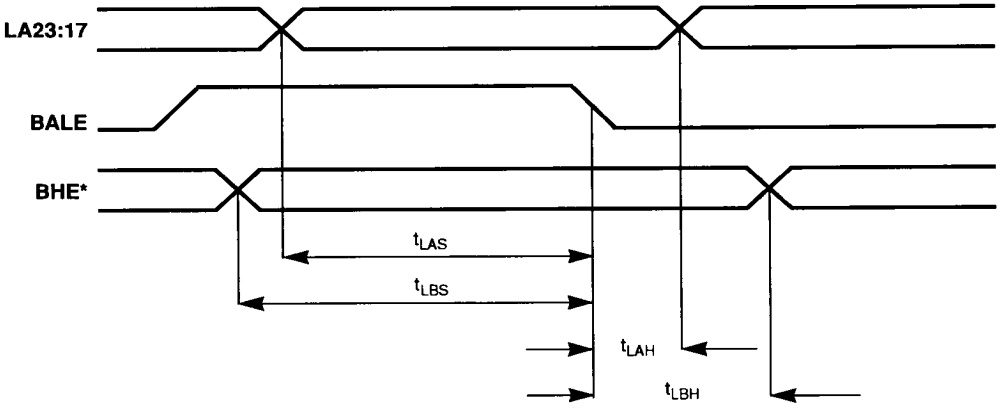


Figure 6–6. BALE Timing (ISA Bus)

Table 6–7. IOCHRDY Timing for Memory Access (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{MA}	MEMW* or MEMR* active to IOCHRDY inactive: 8-bit access 16-bit access		 230 40	 ns ns
t_{ILP}	IOCHRDY inactive pulse width		2100	ns
t_{IMA}	IOCHRDY active from MEMR* or MEMW* active for one additional wait state: 16-bit access	 100	 140	 ns

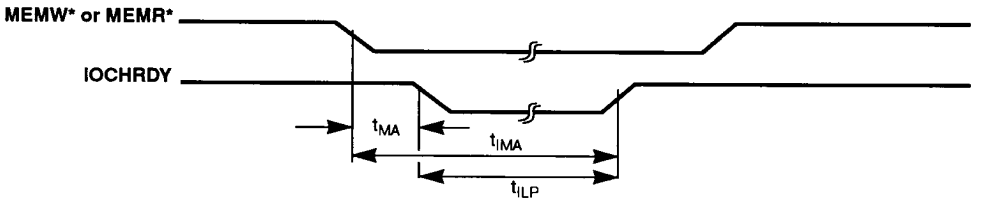


Figure 6–7. IOCHRDY Timing for Memory Access (ISA Bus)

Table 6–8. IOCHRDY Timing for I/O Access (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{IIA}	IOR* or IOW* active to IOCHRDY inactive: 8-bit access		190	ns
t_{ILP}	IOCHRDY inactive pulse width		2100	ns
t_{IIH}	IOCHRDY active from IOR* or IOW* active for one additional wait state: 8-bit access	300	340	ns

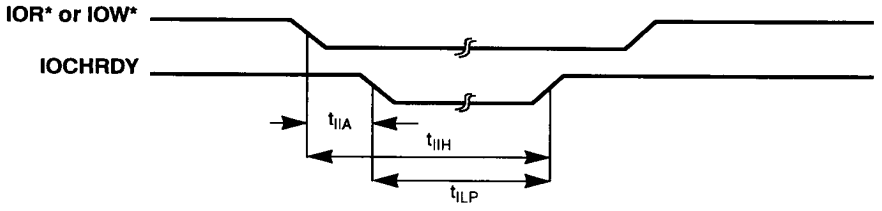


Figure 6–8. IOCHRDY Timing for I/O Access (ISA Bus)

Table 6–9. REFRESH* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{RMA}	REFRESH* active setup to MEMR* active	20		ns
t_{RHM}	REFRESH* active hold from MEMR* inactive	-10		ns

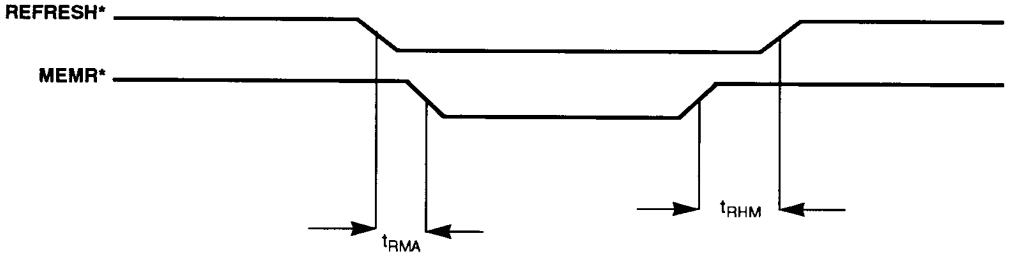


Figure 6–9. REFRESH* Timing (ISA Bus)

Table 6–10. CPWR*/CPRD* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{CDA}	CPWR* active delay from IOW* active CPRD* active delay from IOR* active		60 60	ns ns
t_{CDI}	CPWR* inactive delay from IOW* inactive CPRD* inactive delay from IOR* inactive		30 30	ns ns

NOTE: This is a reference design example. These timing values are not tested or guaranteed.

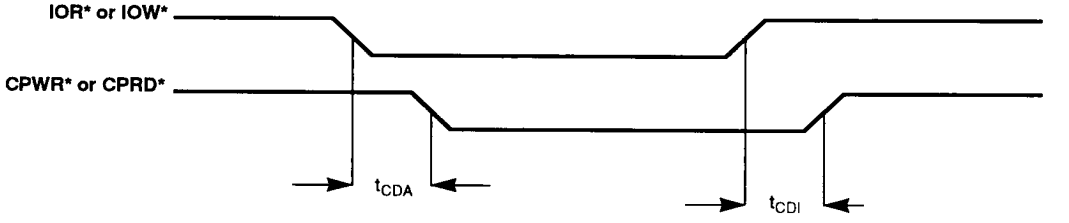


Figure 6–10. CPWR*/CPRD* Timing (ISA Bus)

Table 6–11. DSELH* Timing for 8-Bit Read Access (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{CD8}	Command active to Buffer Control active		60	ns
t_{ICD8}	Command inactive to Buffer Control inactive		20	ns

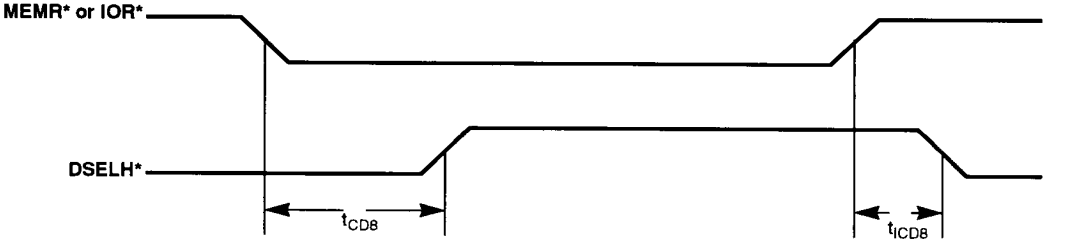
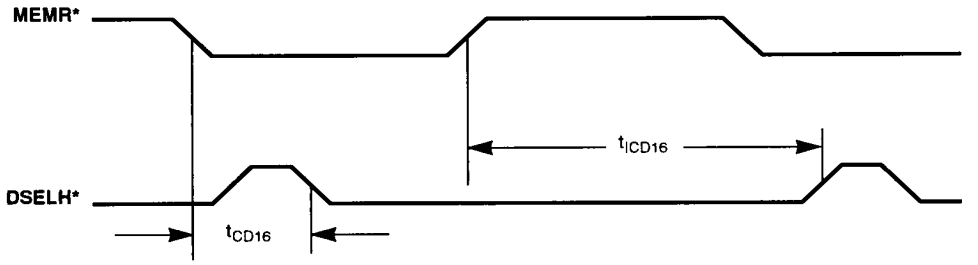


Figure 6–11. DSELH* Timing for 8-Bit Read Access (ISA Bus)

Table 6–12. DSELH* Timing for 16-Bit Memory Read Access (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{CD16}	Command active to Buffer Control active		60	ns
t_{ICD16}	Command inactive to Buffer Control inactive		30	ns



NOTE: DSELH* stays low until the beginning of the next read access.

Figure 6–12. DSELH* Timing for 16-Bit Memory Read Access (ISA Bus)

Table 6–13. DIR Timing for Read Access (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{CD8}	Command active to Buffer Control active		60	ns
t_{ICD8}	Command inactive to Buffer Control inactive		30	ns

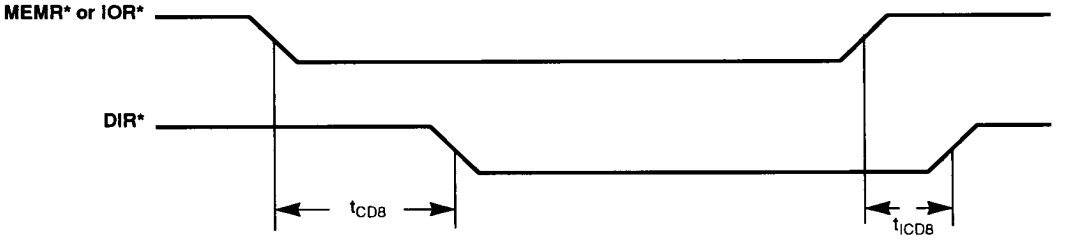


Figure 6–13. DIR Timing for Read Access (ISA Bus)

Table 6–14. DSELH* Timing for Write Access (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{CDS}	Command active to DSELH* active		60	ns
t_{ICDS}	Command inactive to DSELH* inactive		30	ns

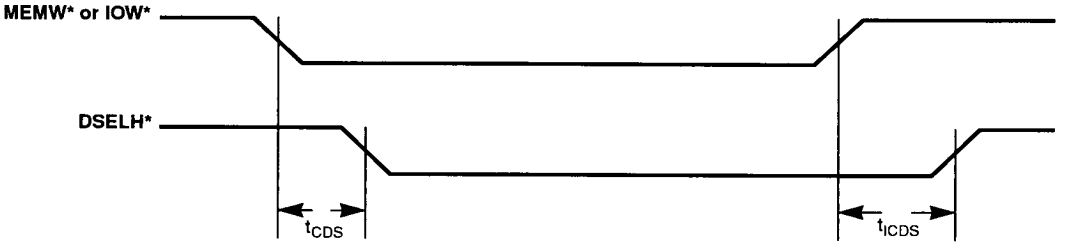


Figure 6–14. DSELH* Timing for Write Access (ISA Bus)

Table 6–15. BIOS-ROMEN* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{RAM}	BIOS-ROMEN* active delay from MEMR* active		30	ns
t_{RIM}	BIOS-ROMEN* inactive delay from MEMR* inactive		30	ns

NOTE: Address to MEMR* setup and hold indicated in Figure 6–4 must be met.

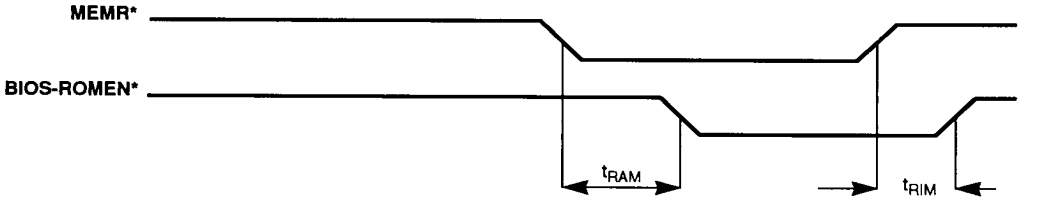


Figure 6–15. BIOS-ROMEN* Timing (ISA Bus)

Table 6–16. AEN Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_{ASI}	AEN active setup to IOR* or IOW* active	20		ns
t_{AHI}	AEN hold from IOR* or IOW* active	0		ns

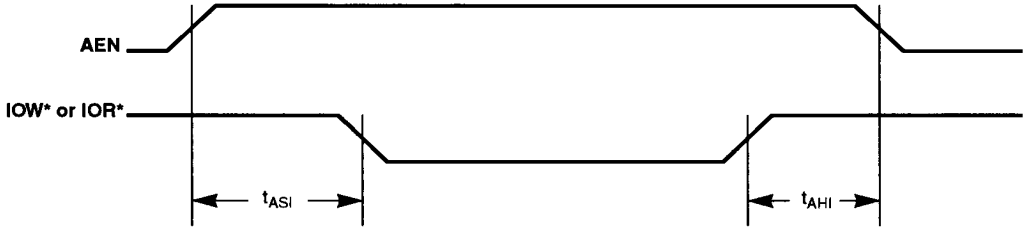


Figure 6–16. AEN Timing (ISA Bus)

Table 6–17. Random Read/Write Cycle Timing

Symbol	Parameter	MIN	MAX	Unit
t_{ASR}	Address setup time to RAS*	5		ns
t_{ASC}	Address setup time to CAS*	5		ns
t_{RCD}	RAS*-to-CAS* delay time	2		T_C
t_{RAH}	Row address hold time	1		T_C
t_{CAH}	Column address hold time	1		T_C
t_{RCS}	Read command setup time	5		ns
t_{DZO}	Data valid from OE* low	†	1.5	T_C
t_{DZR}	Data valid from RAS* low	†	4	T_C
t_{DZC}	Data valid from CAS* low	†	1.5	T_C
t_{DZCA}	Data valid from column address		2.0	T_C
t_{DTO}	Data tristate from OE* high	†	†	ns
t_{RPN}	RAS* precharge time	3		T_C
t_{CR}	Read-write cycle time (random cycle)	7		T_C
t_{RHC}	Read command hold from CAS* high	0.5		T_C
t_{RHR}	Read command hold from RAS* high	1		T_C
t_{RZO}	RAS* hold time from OE* low	2		T_C
t_{CPN}	CAS* precharge time	0.5		T_C
t_{WSC}	WE* setup time to CAS*	0.5		T_C
t_{WHC}	WE* hold time from CAS* low	0.5		T_C
t_{WP}	WE* pulse width	1		T_C
t_{DSC}	Write data setup to CAS*	5		ns
t_{DHC}	Write data hold from CAS*	1		T_C
t_T	Transition time		5	ns
t_{DHR}	Write data hold from RAS* low	3.5		T_C
t_{RP}	RAS* pulse width	4		T_C
t_{CP}	CAS* pulse width	1.5		T_C

NOTES:

1) A (†) indicates the parameter is a device-dependent value.

2) T_C is one SQCLK period.

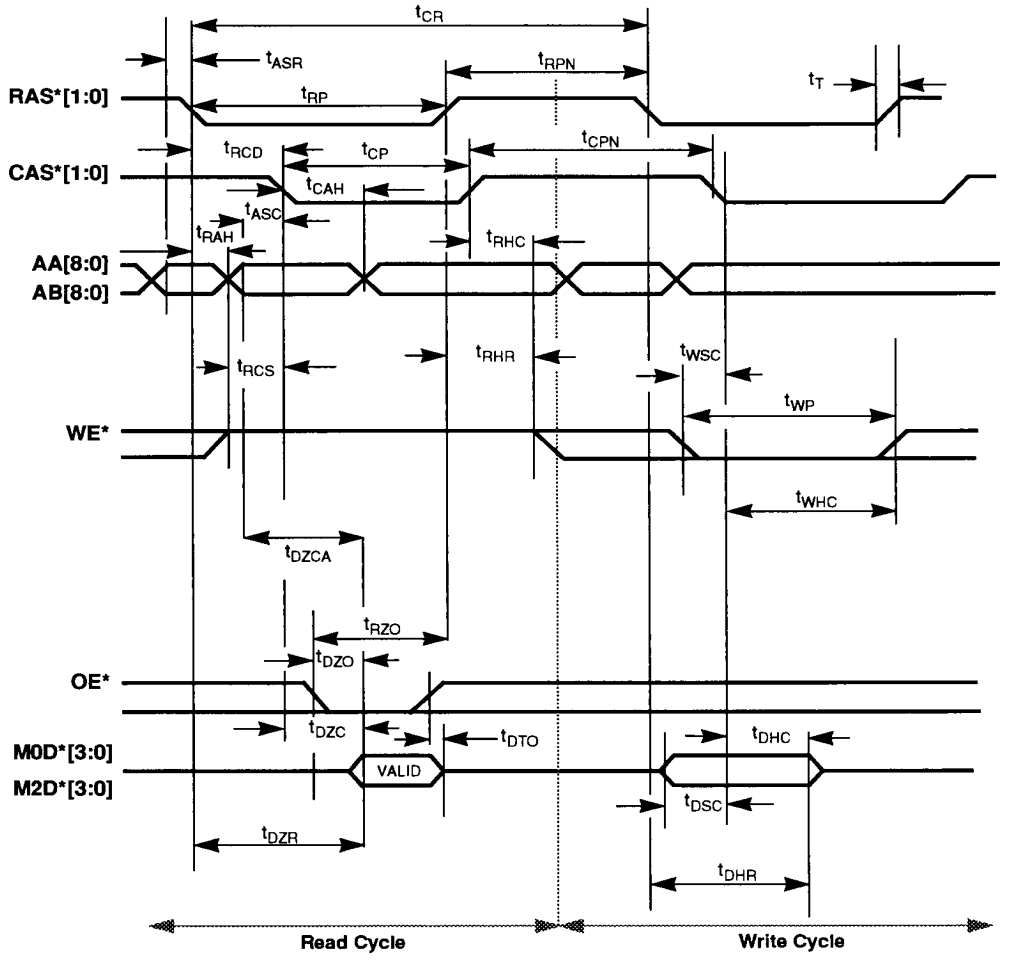


Figure 6–17. Random Read/Write Cycle Timing

Table 6–18. Fast-Page-Mode Read/Write Cycle Timing

Symbol	Parameter	MIN	MAX	Unit
t_{ASR}	Address setup time to RAS*	5		ns
t_{ASC}	Address setup time to CAS*	5		ns
t_{RCD}	RAS* to CAS* delay time	2		T_C
t_{RAH}	Row address hold time	1		T_C
t_{CAH}	Column address hold time	1		T_C
t_{RCS}	Read command setup time	5		ns
t_{DZO}	Data valid from OE* low	†	1.5	T_C
t_{DZR}	Data valid from RAS* low		4	T_C
t_{DZC}	Data valid from CAS* low	†	1.5	T_C
t_{DZCA}	Data valid from column address		2.0	T_C
t_{DTO}	Data tristate from OE* high	†	†	ns
t_{RHC}	Read command hold from CAS* high	0.5		T_C
t_{WSC}	WE* setup time to CAS*	0.5		T_C
t_{WHC}	WE* hold time from CAS* low	0.5		T_C
t_{WP}	WE* pulse width	1		T_C
t_{DSC}	Write data setup to CAS*	5		ns
t_{DHC}	Write data hold from CAS*	1		T_C
t_T	Transition time		5	ns
t_{CP}	Page Mode cycle time	2		T_C
t_{CPN}	CAS* precharge (Page Mode)	0.5		T_C

NOTES:

1) A (†) indicates the parameter is a device-dependent value.

2) T_C is one SQCLK period.

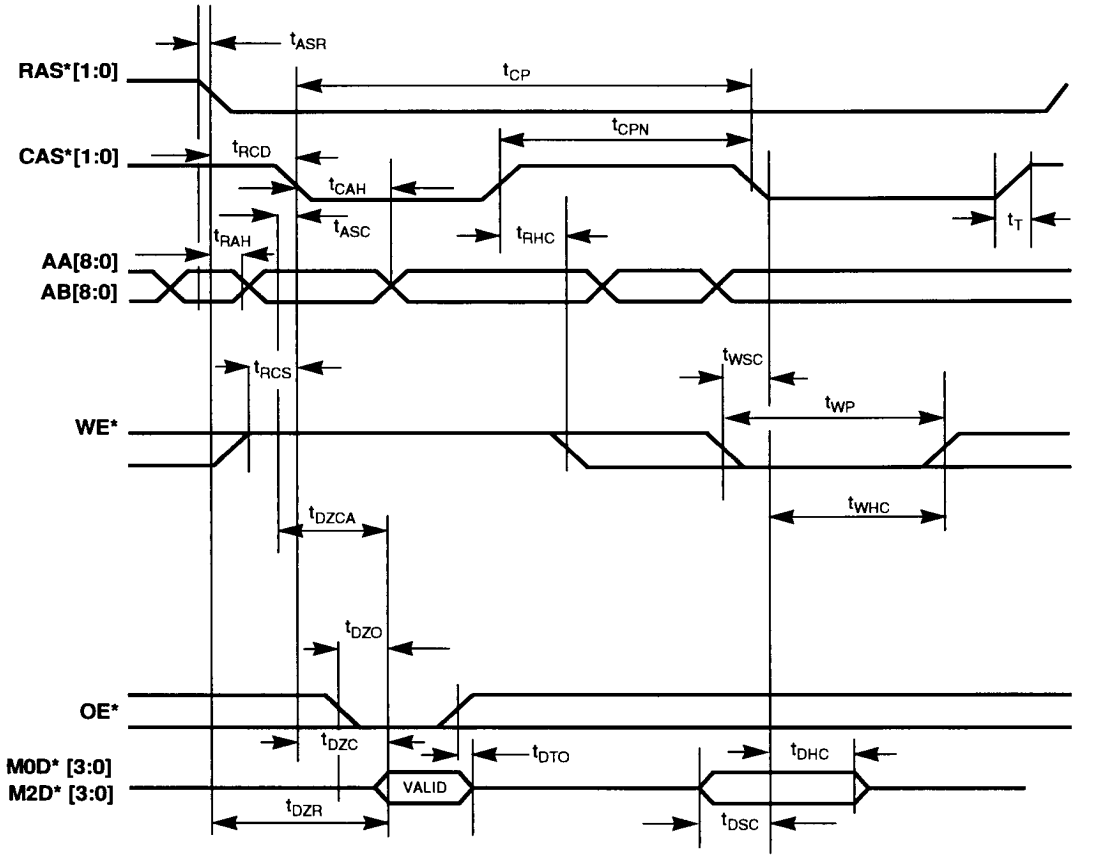


Figure 6-18. Fast-Page-Mode Read/Write Cycle Timing

Table 6–19. CAS*-Before-RAS* Refresh Cycle Timing

Symbol	Parameter	MIN	MAX	Unit
t_{CSR}	CAS* setup before RAS*	1		T_C
t_{CHR}	CAS* hold from RAS*	1.5		T_C
t_{RPL}	RAS* pulse width (low)	6		T_C
t_{RPH}	RAS* pulse width (high)	2		T_C
t_{RC}	Cycle (Refresh)	9		T_C

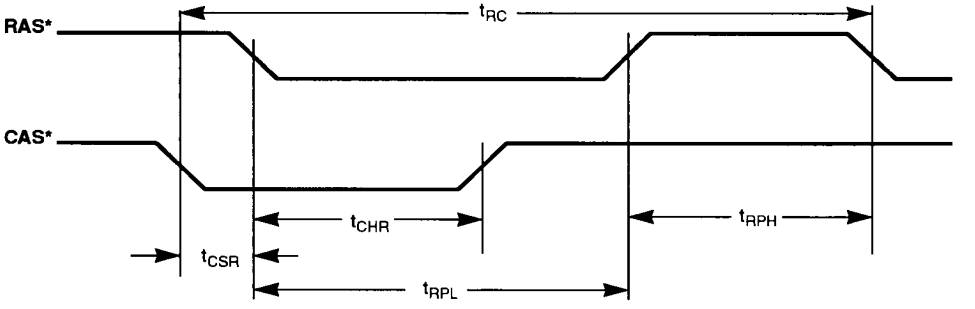


Figure 6–19. CAS*-Before-RAS* Refresh Cycle Timing

Table 6–20. External RAMDAC Timing

Symbol	Parameter	MIN	MAX	Unit
t_{PSV}	Setup before VDCLK	3		ns
t_{PHV}	Hold from VDCLK	3		ns

NOTE: This is a reference design example. These timing values are not tested or guaranteed.

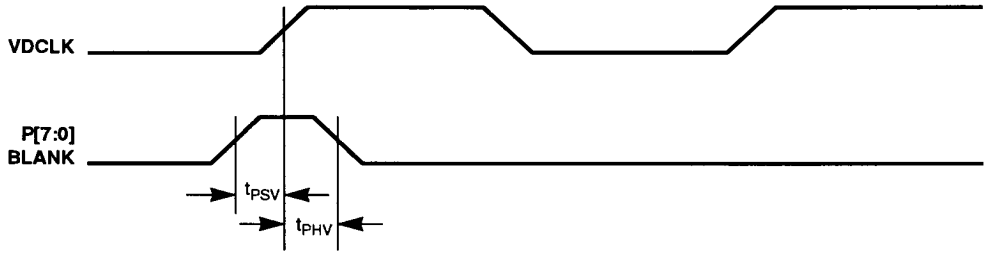


Figure 6–20. External RAMDAC Timing

Table 6–21. Clocks

Symbol	Parameter	MIN	MAX	Unit
t_R	Rise time:			
	SQCLK		6	ns
	VDCLK		6	ns
	OSC (below 25 MHz)		10	ns
	OSC (above 25 MHz)		6	ns
	CLKSEL[3:0] (below 25 MHz)		10	ns
	CLKSEL[3:0] (above 25 MHz)		6	ns
t_F	Fall time:			
	SQCLK		6	ns
	VDCLK		6	ns
	OSC (below 25 MHz)		10	ns
	OSC (above 25 MHz)		6	ns
	CLKSEL[3:0] (below 25 MHz)		10	ns
	CLKSEL[3:0] (above 25 MHz)		6	ns
t_{CP}	Clock Period:			
	SQCLK		44.9	MHz
	OSC (CRT rev A)		32	MHz
	OSC (CRT rev B)		40.0	MHz
	OSC (monochrome LCD)		25.175	MHz
	OSC (512-color TFT LCD)		25.175	MHz
t_H	High Period (Note 1):			
	SQCLK (rev A)	-5% (rev A)	+5% (rev A)	
	SQCLK (rev B)	-10% (rev B)	+10% (rev B)	
	VDCLK (rev A)	-5% (rev A)	+5% (rev A)	
	VDCLK (rev B)	-10% (rev B)	+10% (rev B)	
	OSC (rev A)	-5% (rev A)	+5% (rev A)	
	OSC (rev B)	-10% (rev B)	+10% (rev B)	
	CLKSEL[3:0] (rev A)	-5% (rev A)	+5% (rev A)	
	CLKSEL[3:0] (rev B)	-10% (rev B)	+10% (rev B)	
t_L	Low Period (Note 1):			
	SQCLK (rev A)	-5% (rev A)	+5% (rev A)	
	SQCLK (rev B)	-10% (rev B)	+10% (rev B)	
	VDCLK (rev A)	-5% (rev A)	+5% (rev A)	
	VDCLK (rev B)	-10% (rev B)	+10% (rev B)	
	OSC (rev A)	-5% (rev A)	+5% (rev A)	
	OSC (rev B)	-10% (rev B)	+10% (rev B)	
	CLKSEL[3:0] (rev A)	-5% (rev A)	+5% (rev A)	
	CLKSEL[3:0] (rev B)	-10% (rev B)	+10% (rev B)	

NOTES:

1) The percentages for High and Low Period indicate permissible deviation from $t_{CP}/2$.

2) 25.175 MHz = SimulSCAN.

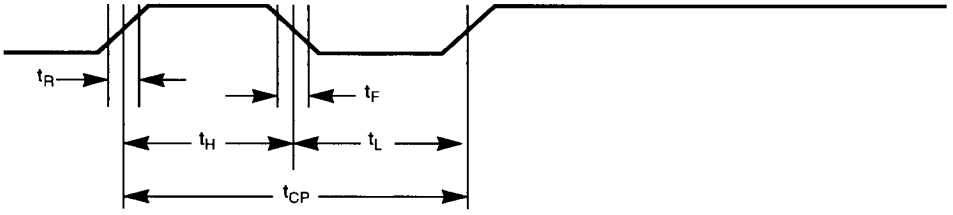


Figure 6–21. Clocks

Table 6–22. Sync, BLANK*, and RGB as Outputs (Internal VDCLK)

Symbol	Parameter	MIN	MAX	Unit
t_{VBD}	VDCLK to BLANK* delay	3	7	ns
t_{VPD}	VDCLK to P[7:0] delay	3	7	ns
t_{VHD}	VDCLK to HSYNC, VSYNC delay	0	5	ns
t_{AND}	VDCLK to R, G, B delay	0	30	ns

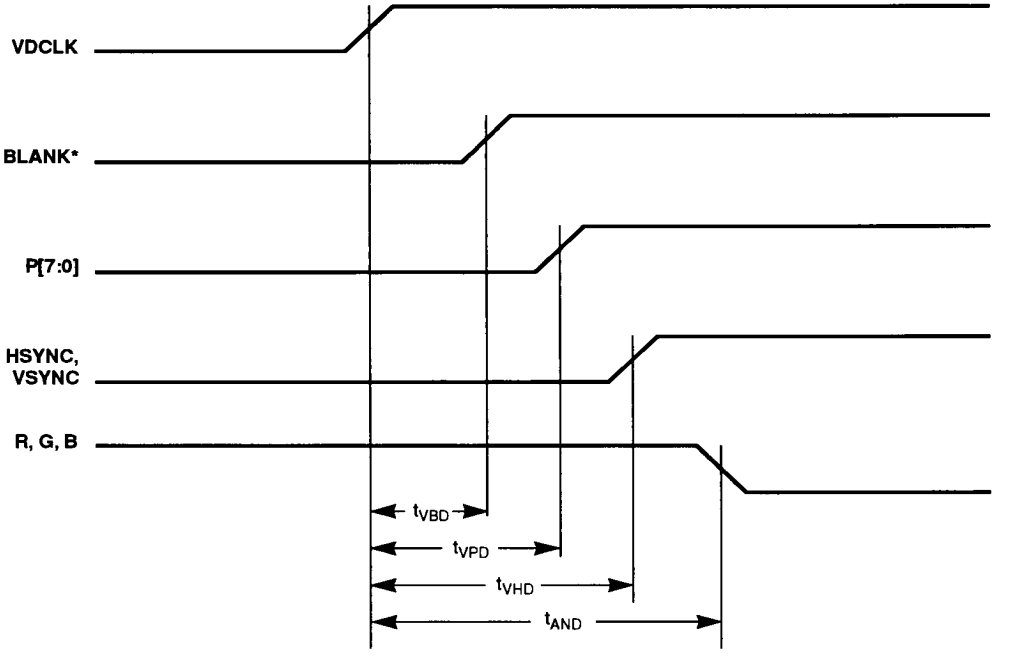


Figure 6–22. Sync, BLANK*, and RGB as Outputs (Internal VDCLK)

Table 6–23. Suspend Mode Timing

Symbol	Parameter	MIN	MAX	Unit
t_{CSR}	CAS* setup to RAS* low	20	200	ns
t_{CHR}	CAS* hold after RAS* low	100	1000	ns
t_{CL}	CAS* low time	120	1000	ns
t_{RL}	RAS* low time	120	1000	ns
t_{REF}	Refresh period (normal)	$T_{SUSP}/2$		ns
t_{REF}	Refresh period (slow)	$T_{SUSP}*4$		ns

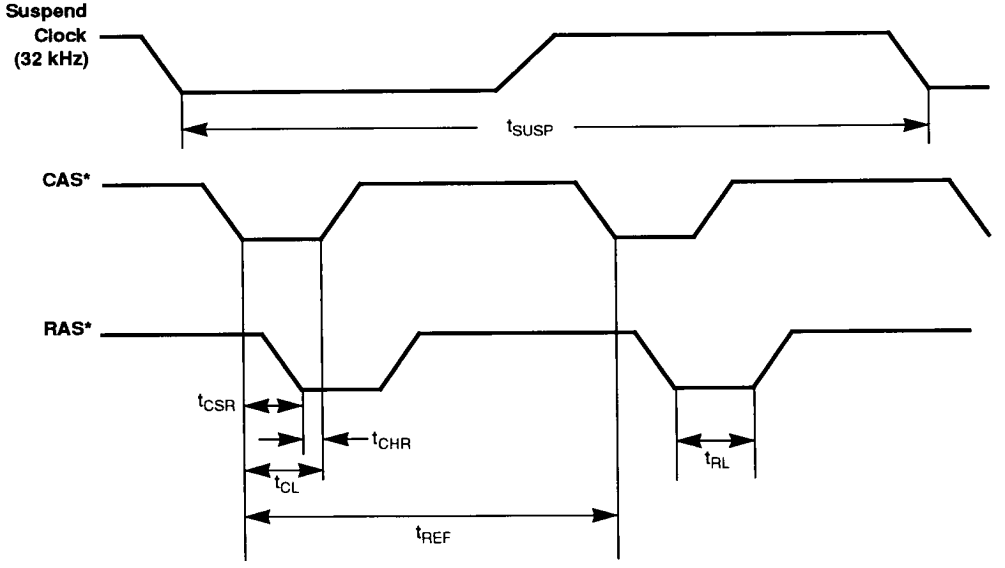


Figure 6–23. Suspend Mode Timing

Table 6–24. Programmable Pins Output Timing

Symbol	Parameter	MIN	MAX	Unit
t_{DWO}	Delay from IOW* inactive to output valid	0	100	ns

NOTE: The programmable pins include PO1, PO2, FC[0]/FPVCC, FC[1]/FPVEE, and CLKSEL [3:0] in Output Mode. CLKSEL [3:0] is in Output Mode at power-on.

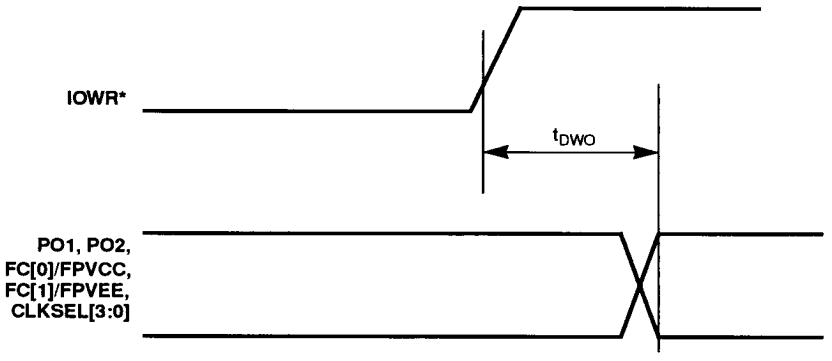


Figure 6–24. Programmable Pins Output Timing

Table 6–25. Frame-Accelerator Interfacing Timing

Symbol	Parameter	MIN	MAX	Unit
t_{FRS}	Row Address valid setup to FRRAS* active	2 T_{SQ}		ns
t_{FRH}	Row Address hold from FRRAS* active	0.5 T_{SQ}		ns
t_{FOD}	Read Data delay from FROE* active	5		ns
t_{FCS}	Column Address valid setup to FRCAS* active	0.5 T_{SQ} -5		ns
t_{FCH}	Column Address valid hold after FRCAS* active	0.5 T_{SQ} -5		ns
t_{FODH}	Read Data hold after FROE* inactive	2	0.5 T_{SQ}	ns
t_{FODS}	Read Data setup to FROE* inactive	5		ns
t_{FCOS}	FRCAS* active delay to FROE* active	0.5 T_{SQ}		ns
t_{FOE}	FROE* active pulse width	1 T_{SQ}		ns
t_{FWS}	Write Data setup to FRWE* active	0.5 T_{SQ} -10		ns
t_{FWH}	Write Data hold from FRWE* inactive	0.5 T_{SQ} -5	0.5 T_{SQ} +5	ns
t_{FWA}	FRWE* active time	0.5 T_{SQ} -5	0.5 T_{SQ} +5	ns
t_{FCC}	FRCAS* cycle time	4 T_{SQ}		ns
t_{FCI}	FRCAS* inactive time	1 T_{SQ} -5		ns
t_{FCA}	FRCAS* active time	3 T_{SQ} -5		ns
t_{FRI}	FRRAS* inactive time	12 T_{SQ} -5		ns
t_{FRA}	FRRAS* active time	641 T_{SQ} -5		ns

NOTE: T_{SQ} = one CRT clock period.

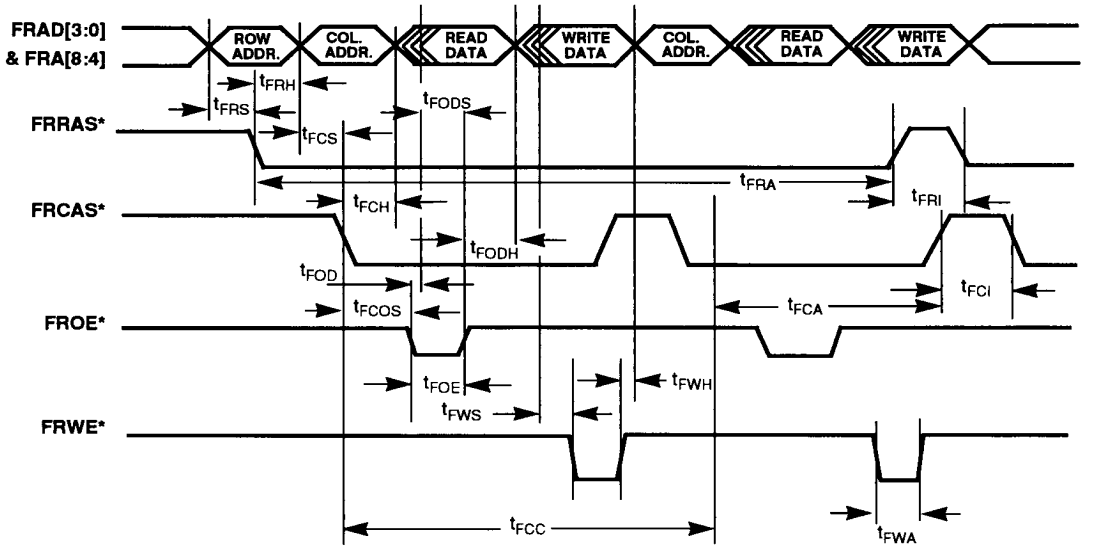


Figure 6–25. Frame-Accelerator Interface Timing

Table 6–26. Monochrome Dual-Scan Passive LCD Interface Timing

Symbol	Parameter	MIN	MAX	Unit
t_{KP}	LLCLK pulse width	T_C		ns
t_{KLK}	FPVDCLK low setup to LLCLK	T_C +20		ns
t_{KC}	FPVDCLK cycle time	T_C -10		ns
t_{KH}	FPVDCLK high time	0.5 T_C -10		ns
t_{KF}	FPVDCLK fall time		5	ns
t_{KR}	FPVDCLK rise time		5	ns
t_{KHL}	FPVDCLK low hold time after LLCLK low	T_C -20		ns
t_{VDS}	Video data setup time	0.5 T_C -5		ns
t_{VDH}	Video data hold time	0.5 T_C -5		ns
t_{LHK}	LFS high hold time after LLCLK low	T_C		ns
t_{LSK}	LFS high setup to LLCLK low	T_C		ns
t_{MDK}	MOD delay from LLCLK high		30	ns

NOTE: T_C = 25.175 MHz/4.

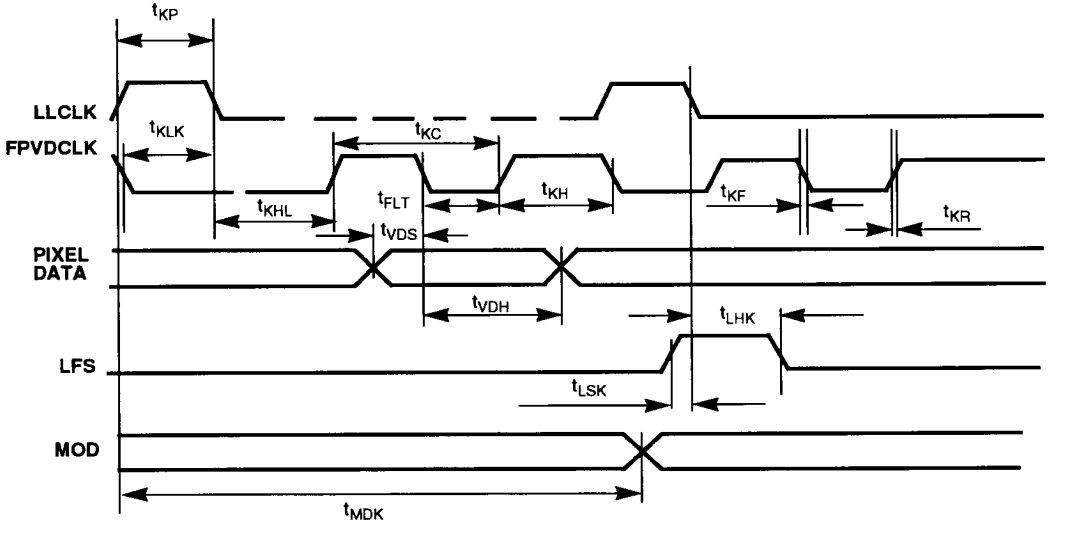


Figure 6–26. Monochrome Dual-Scan Passive LCD Interface Timing

Table 6–27. 512-Color LCD Interface Timing

Symbol	Parameter	MIN	MAX	Unit
t_{KP}	HSYNC pulse width	90		T_C
t_{KC}	FPVDCLK cycle time	0.95 T_C	1.05 T_C	T_C
t_{KH}	FPVDCLK high time	0.5 T_C -5	0.5 T_C +5	T_C
t_{KL}	FPVDCLK low time	0.5 T_C -5	0.5 T_C +5	T_C
t_{KF}	FPVDCLK fall time		10	ns
t_{KR}	FPVDCLK rise time		10	ns
t_{VDS}	Video data setup time	10		ns
t_{VDH}	Video data hold time	10		ns
t_{KLK}	FPVDCLK low to HSYNC active	0.5		T_C
t_{DDS}	Panel Data valid to FPHDE active	0		ns
t_{DDH}	FPHDE inactive to FPVDCLK low	10		ns
t_{BSD}	FPHDE active to FPVDCLK low	8		ns
t_{BSH}	FPVDCLK low to FPHDE inactive	10		ns
t_{BDD}	VSYNC inactive to valid Data	0		ns
t_{BP}	VSYNC pulse width	1600		T_C

NOTE: T_C = 25.175 MHz = SimulSCAN.

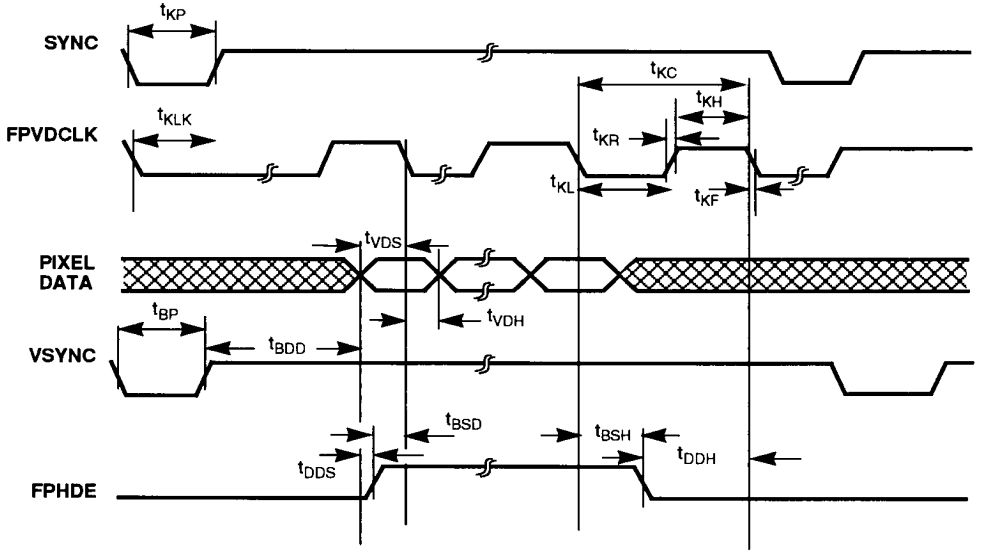


Figure 6–27. 512-Color LCD Interface Timing

7. CL-GD6410 REGISTERS

The following tables list the CL-GD6410 Extension registers.

Extension Registers

Abbreviation	Register Name	Index	Port	Page
ER0A	Extension Control	0A	3CF	55
ER0B	Attribute Controller Index at Extension	0B	3CF	56
ER0C	CR11 Bit 7 at Extension	0C	3CF	57
Reserved	–	0D-0F	3CF	–
Reserved	–	30-5F	3CF	–
ER60	Horizontal Total Extension	60	3CF	58
ER61	Horizontal Blank Start Extension	61	3CF	60
ER62	Horizontal Blank End Extension	62	3CF	61
ER63	Horizontal Retrace Start Extension	63	3CF	62
ER64	Horizontal Retrace End Extension	64	3CF	63
Reserved	–	65-6F	3CF	–
ER70	Vertical Total Extension	70	3CF	64
ER71	Vertical Display Enable Extension	71	3CF	65
ER72	Vertical Blank Start Extension	72	3CF	66
ER73	Vertical Blank End Extension	73	3CF	67
ER74	Vertical Retrace Start Extension	74	3CF	68
ER75	Vertical Retrace End Extension	75	3CF	69
Reserved	–	76-77	3CF	–
ER78	CR07 Extension	78	3CF	70
ER79	Vertical Overflow	79	3CF	71
ER7A	Coarse Vertical Retrace Skew	7A	3CF	72
Reserved	–	7B	3CF	–
ER7C	Screen A Start Address Extension	7C	3CF	73
Reserved	–	7D-7F	3CF	–
ER80	H/V Retrace Polarity Control Register	80	3CF	74
ER81	Display Mode	81	3CF	75
ER82	Character Clock Selection	82	3CF	76
ER83	Write Control	83	3CF	77
ER84	Clock Select	84	3CF	78
Reserved	–	85	3CF	–
ER86	CRTC Test	86	3CF	80
ER87	CRTC Spare Extension (Rev. B Only)	87	3CF	81
Unused	–	88	3CF	–
ER89	CRTC Spare 1	89	3CF	–
ER8A	CRTC Spare 2	8A	3CF	–
Unused	–	8B-8E	3CF	–
ER8F	CRTC BIOS Configuration	8F	3CF	82
ER90	Display Memory Control	90	3CF	84
ER91	CRT-Circular Buffer Policy Selection	91	3CF	86
ER92	Font Control	92	3CF	87
ER95	CRT-Circular Buffer Delta and Burst	95	3CF	88
ER96	Display Memory Control Test	96	3CF	89

7. CL-GD6410 REGISTERS *(cont.)*

Abbreviation	Register Name	Index	Port	Page
ER97	Monitor Switches Read-back	97	3CF	90
ER98	Scratch	98	3CF	91
ER99	Configuration Register	99	3CF	92
ER9A	Display Memory Configuration	9A	3CF	93
ER9B	Miscellaneous Configuration	9B	3CF	94
ER9C	PS/2 Monitor ID	9C	3CF	96
Reserved	–	9D-9F	3CF	–
ERA0	Bus Interface Unit Control	A0	3CF	97
ERA1	Three-State and Test Control	A1	3CF	99
ERA2	BIOS Page Selection	A2	3CF	100
Reserved	–	A3-A5	3CF	–
ERA6	Wait State Control	A6	3CF	101
ERA7	General I/O Controls	A7	3CF	102
Reserved	–	A8	3CF	–
ERA9	Bus Interface Cache Control	A9	3CF	103
ERAA	Design Revision	AA	3CF	105
ERAB	Mask Revision	AB	3CF	106
Reserved	–	AC-B9	3CF	–
ERBA-BF	Scratch Register 5-0	BA-BF	3CF	107
ERC0	Attribute and Graphics Control	C0	3CF	108
ERC1	Cursor Attributes	C1	3CF	109
ERC2-C5	Graphics Controller Memory Latches 0-3	C2-C5	3CF	110
Reserved	–	C6-C7	3CF	–
ERC8	RAMDAC Control	C8	3CF	111
ERC9	Graphics and Attribute Test	C9	3CF	112
Reserved	–	CA-CF	3CF	–
ERD0	Flat Panel Column Offset	D0	3CF	113
ERD1	Flat Panel Horizontal Size	D1	3CF	114
ERD2	Flat Panel Row Offset	D2	3CF	115
ERD3	Flat Panel Vertical Size	D3	3CF	116
ERD4	Flat Panel Overflow	D4	3CF	117
ERD5	Flat Panel Attribute Control	D5	3CF	118
ERD6	Flat Panel Gray Scale Offset	D6	3CF	120
ERD7	Flat Panel Retrace Line Clock Control	D7	3CF	122
ERD8	Flat Panel Frame Color	D8	3CF	123
ERD9	Flat Panel AC Modulation	D9	3CF	124
ERDA	Flat Panel Display Control	DA	3CF	125
ERDB	Standby Timer Control	DB	3CF	127
ERDC	Flat Panel Color Configuration	DC	3CF	128
Reserved	–	DD-DF	3CF	–

7.1 VGA Register Port Map

Table 7–1. VGA Register Port Map

Address	Port
3?4	CRT Controller Index (R/W)
3?5	CRT Controller Data (R/W)
3BA	Feature Control (W), Input Status Register 1 (R) (Monochrome)
3C0	Attribute Controller Index/Data (Write)
3C1	Attribute Controller Index/Data (Read)
3C2	Miscellaneous Output (W), Input Status Register 0 (R)
3C3	VGA Enable (R/W)
3C4	Sequencer Index (R/W)
3C5	Sequencer Data (R/W)
3C6	Video DAC Pixel Mask (R/W), Hidden DAC Register (R/W)
3C7	Pixel Address Read Mode (W), DAC State (R)
3C8	Pixel Mask Write Mode (R/W)
3C9	Pixel Data (R/W)
3CA	Feature Control Readback (R)
3CC	Miscellaneous Output Readback (R)
3CE	Graphics Controller Index (R/W)
3CF	Graphics Controller Data (R/W)
3DA	Feature Control (W), Input Status Register 1 (R) (Color)

NOTE: The '?' in an address would be 'B' for monochrome and 'D' for color

7.2 Register Delta List Between the CL-GD6410-A and the CL-GD6410-B

Table 7–2. Register Delta List

Register	CL-GD6410-A	CL-GD6410-B
ER81[6]	Not Used	Used
ER87[7,4]	Not Used	Used
ER90[6]	Not Used	Used
ER97 and ER99	Pull-Down Resistors May Be Used	Pull-Down Resistors Are Not Necessary
ERD6[5,4]	Not Used	Used
ERD8[6]	Not Used	Used
ERDA[0]	Not Used	Used

7.3 CL-GD6410 Extended Register Details

7.3.1 Extension Control Register: ER0A

I/O Port Address: 3CF

Index: 0A

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Reserved		0
2	Reserved		0
1	Reserved		0
0(LSB)	Extensions Register Access Flag	R/W	0

This register is used to enable or disable access to the Extension Registers.

To enable access to the Extension Registers, write the value EC to this register. A subsequent read from this register will return the value '01', indicating access to the Extension Registers.

To disable access to the Extension Registers, write the value CE to this register. A subsequent read from this register will return the value '00', indicating no access to the Extension Registers.

Bit	Description
Bits 7:1	Reserved
Bit 0	**Extensions Register Access Flag:** A '1' indicates access is allowed to the Extension Registers.

7.3.2 Attribute Controller Index At Extension Register: ER0B

I/O Port Address: 3CF

Index: 0B

Bit	Description	Access	Reset State
7(MSB)	Index/Data State of Attribute Controller	R/W	0
6	Reserved		0
5	Video Enable	R/W	0
4	Attribute Controller Index 4	R/W	x
3	Attribute Controller Index 3	R/W	x
2	Attribute Controller Index 2	R/W	x
1	Attribute Controller Index 1	R/W	x
0(LSB)	Attribute Controller Index 0	R/W	x

This register duplicates the Attribute Controller Index Register (3C0) Bits 5-0. In addition, Bit 7 enables the program to unconditionally determine or force the state of the Index/Data Pointer.

Bit	Description
Bit 7	**Index/Data State of Attribute Controller:** This bit reflects and controls the state of the Index/Data Pointer in the Attribute Controller. When the register is read, the state is returned; when the register is written, the state is forced. 0 = Index 1 = Data
Bit 6	Reserved
Bit 5	**Video Enable:** When this bit is reset to a '0', the screen displays the color indicated by Overscan Register AR11 (normally black); when set to a '1', normal video display is enabled. In the standard VGA, this bit also selects the address source for the Palette Registers (0 = CPU and 1 = Video), which requires that CPU writes to the Palette Registers only occur when this bit is a '0' (or else the data will be written to random Palette Register locations as determined by the Video Data Stream at the time of the write). In the CL-GD64XX, the palette is dual-ported and may be accessed at any time, independent of the state of this bit.
Bits 4:0	**Attribute Controller Indexes:** These five bits form the index to the Data Registers in the Attribute Controller.

7.3.3 CR11 Bit 7 at Extension Register: ER0C

I/O Port Address: 3CF

Index: 0C

Bit	Description	Access	Reset State
7(MSB)	Write Protect CR00-CR07	R/W	0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Reserved		0
2	Reserved		0
1	Reserved		0
0(LSB)	Reserved		0

This register is used to break a deadlock between CR3 and CR11.

Bit	Description
Bit 7	**Write Protect CR00-CR07:** This bit provides write protection for Registers CR00-CR07 (mostly the Horizontal Control Registers). The functionality of this bit is the same as Bit 7 of CR11h. This bit resolves the deadlock issue described in the next paragraph. If CR3[7] is reset to a '0', then CR11 no longer controls write protect for CR0-CR7. If CR11[7] is set to a '1', then CR3[7] is write protected. Since CR3[7] is write protected, CR10 and CR11 cannot be accessed as Vertical Retrace Control Registers, and in particular, CR11[7] cannot be programmed to change the write-protected state of CR3[7]. ER0C[7] is always accessible and breaks the deadlock.
Bits 6:0	Reserved

7.3.4 Horizontal Total Extension Register: ER60

I/O Port Address: 3CF

Index: 60

Bit	Description	Access	Reset State
7(MSB)	Horizontal Total Extension	R/W	0
6	Horizontal Total Extension	R/W	0
5	Horizontal Total Extension	R/W	0
4	Horizontal Total Extension	R/W	0
3	Horizontal Total Extension	R/W	0
2	Horizontal Total Extension	R/W	0
1	Horizontal Total Extension	R/W	0
0(LSB)	Horizontal Total Extension	R/W	0

The registers ER60h to ER64h are grouped as the working set of CRTC horizontal monitor timing, and they always control the CRTC to drive horizontal monitor timing. These registers are the counterpart of the CRTC Standard Registers mapped into Extension Address Spaces and are totally transparent to standard VGA applications.

The data sources are controlled by ER83h[1] when the working set is being updated.

ER83h[1] = 0:

The data will be written to both corresponding standard registers in CRTC and the registers in this working set through standard address path, 3X4h (X = D or B).

ER83h[1] = 1:

The working set registers can only be written from the extension address path. The corresponding standard registers in CRTC will not be changed.

Bit	Description
Bits 7:0	**Horizontal Total Extension:** The value in this register is the least-significant eight bits of a 9-bit field specifying the total number of horizontal character clocks; the most-significant bit is in ER64[5]. This value includes the number of character in the active-display area and the number of characters required for the horizontal blanking period. The actual value programmed is the total number of characters in a horizontal display period minus 5. The total number of characters in a horizontal display period is calculated from dot clock, horizontal frequency, and font width.

7.3.4 Horizontal Total Extension Register: ER60 *(cont.)*

For example:

Dot Clock = 28.322 MHz, Horizontal Frequency = 32.5 kHz, Font Width = 9 Dots.

28322/31.5 = 900 dots approximately per horizontal cycle.
900/9 = 100 characters per horizontal cycle.
100 - 5 = 95 (5Fh) to be programmed into this register.

In standard VGA, horizontal total has an 8-bit value. In the CL-GD64XX family, the horizontal total is extended to up to 512-character clocks.

7.3.5 Horizontal Blank Start Extension Register: ER61

I/O Port Address: 3CF

Index: 61

Bit	Description	Access	Reset State
7(MSB)	Horizontal Blank Start Extension Bit 7	R/W	0
6	Horizontal Blank Start Extension Bit 6	R/W	0
5	Horizontal Blank Start Extension Bit 5	R/W	0
4	Horizontal Blank Start Extension Bit 4	R/W	0
3	Horizontal Blank Start Extension Bit 3	R/W	0
2	Horizontal Blank Start Extension Bit 2	R/W	0
1	Horizontal Blank Start Extension Bit 1	R/W	0
0(LSB)	Horizontal Blank Start Extension Bit 0	R/W	0

Bit	Description
Bits 7:0	**Horizontal Blank Start Extension:** The value in this register is the least-significant eight bits of a 9-bit field specifying horizontal blanking start. The most-significant bit is ER62[7]. This bit is used to indicate in character clock units, based on 0, when the Horizontal Blanking Signal becomes active. When the internal character counter reaches the value programmed into this register, blanking starts. If the Blanking Signal is activated too early, some of the display will be lost. If the Blanking Signal is activated after horizontal display enable ends; the timing gap between horizontal display enable end and horizontal blanking start will be the border. This register is also extended to nine bits instead of the eight bits available to standard VGA.

7.3.6 Horizontal Blank End Extension Register: ER62

I/O Port Address: 3CF

Index: 62

Bit	Description	Access	Reset State
7(MSB)	Horizontal Blank Start Extension Bit 8	R/W	0
6	Reserved		0
5	Reserved		0
4	Horizontal Blank End Bit 4	R/W	0
3	Horizontal Blank End Bit 3	R/W	0
2	Horizontal Blank End Bit 2	R/W	0
1	Horizontal Blank End Bit 1	R/W	0
0(LSB)	Horizontal Blank End Bit 0	R/W	0

Bit	Description
Bit 7	**Horizontal Blank Start Extension:** This is Bit 8 of the Horizontal Blank Start Field. It serves to extend ER61, making a 9-bit field.
Bits 6:5	Reserved
Bits 4:0	**Horizontal Blank End:** These bits are used to indicate in character clocks when the Horizontal Blanking Signal becomes inactive. The value is six bits, with the most-significant bit in ER64[7]. The least-significant bits from the following formula determine the value programmed into this register: Horizontal Blanking Start (ER61 and ER62[7]) + Horizontal Blanking Width. The 6-bit value of horizontal blank end limits the length of the horizontal blanking pulse to 63 character clocks in VGA. The Blanking Signal should go inactive at least one character clock before the next Horizontal Display Signal enable. The timing gap between Blanking Signal inactive and Horizontal Display Signal active is perceived as the left border. For example, Horizontal Total Number of Characters = 100 (64h). The horizontal blanking end should be at Location 98 (62h).

7.3.7 Horizontal Retrace Start Extension Register: ER63

I/O Port Address: 3CF

Index: 63

Bit	Description	Access	Reset State
7(MSB)	Horizontal Retrace Start Bit 7	R/W	0
6	Horizontal Retrace Start Bit 6	R/W	0
5	Horizontal Retrace Start Bit 5	R/W	0
4	Horizontal Retrace Start Bit 4	R/W	0
3	Horizontal Retrace Start Bit 3	R/W	0
2	Horizontal Retrace Start Bit 2	R/W	0
1	Horizontal Retrace Start Bit 1	R/W	0
0(LSB)	Horizontal Retrace Start Bit 0	R/W	0

Bit	Description
Bits 7:0	**Horizontal Retrace Start:** This entire byte is the lower eight bits of the 9-bit location value of Horizontal Retrace Start. The most-significant bit is at ER64[6]. These eight bits are used to indicate the point at which the horizontal synchronization pulse becomes active. The value in the register will affect the centering of the screen horizontally.

7.3.8 Horizontal Retrace End Extension Register: ER64

I/O Port Address: 3CF

Index: 64

Bit	Description	Access	Reset State
7(MSB)	Horizontal Blank End Bit 6	R/W	0
6	Horizontal Retrace Start Extension Bit 8	R/W	0
5	Horizontal Total Extension Bit 8	R/W	0
4	Horizontal Retrace End Bit 4	R/W	0
3	Horizontal Retrace End Bit 3	R/W	0
2	Horizontal Retrace End Bit 2	R/W	0
1	Horizontal Retrace End Bit 1	R/W	0
0(LSB)	Horizontal Retrace End Bit 0	R/W	0

This register contains extension bits for the horizontal parameters of the CRTC.

Bit	Description
Bit 7	**Horizontal Blank End Bit 6:** This bit is the most-significant bit of the horizontal blank end 6-bit field (refer to ER62).
Bit 6	**Horizontal Retrace Start Extension Bit 8:** This is Bit 9 of the Horizontal Retrace Start Field. It serves to extend CR4, making a 9-bit field (refer to ER63).
Bit 5	**Horizontal Total Extension Bit 8:** This is Bit 8 of the Horizontal Total Field. It serves to extend CR0, making a 9-bit field (refer to ER60).
Bits 4:0	**Horizontal Retrace End:** These are the five bits specifying the value for the character clock count when the Horizontal Retrace Signal becomes inactive. The least-significant five bits from the following formula determine the value programmed into this register: Horizontal Retrace Start (ER63 + ER64[6]) + Horizontal Synchronization Width. This 5-bit value limits the length of the Retrace Signal to 32 character clocks. The Horizontal Retrace Signal should always end before the Horizontal Blanking Signal.

7.3.9 Vertical Total Extension Register: ER70

I/O Port Address: 3CF

Index: 70

Bit	Description	Access	Reset State
7(MSB)	Vertical Total Bit 7	R/W	0
6	Vertical Total Bit 6	R/W	0
5	Vertical Total Bit 5	R/W	0
4	Vertical Total Bit 4	R/W	0
3	Vertical Total Bit 3	R/W	0
2	Vertical Total Bit 2	R/W	0
1	Vertical Total Bit 1	R/W	0
0(LSB)	Vertical Total Bit 0	R/W	0

The Registers ER70 through ER75, ER78, and ER79 are grouped as a working set for vertical display timing; they are the correspondent of standard registers in the CRTC, mapped into extension address space. This working set always controls the CRTC and is actually driving vertical monitor timing. The values in the registers of the working set are controlled by either ER83[0]. When these control registers are set, data is read and written to the standard registers without affecting these working set registers. In this case, the only way to affect the values in the working set registers is through the extension address. When the control registers are cleared, the working set registers will be affected by changes made to the standard registers through the standard address path. The registers in this working set can be read or written to through the extension address path at any time, but the standard registers will not be affected.

Bit	Description
Bits 7:0	**Vertical Total Bits 7:0:** These are the least-significant eight bits of the 11-bit value that specifies the total number of vertical scanlines in one frame. The 11-bit value for vertical total scanlines is calculated by subtracting 2 from the actual total number of scanlines in one vertical frame. The functionality of this register is the same as CR06, in the CRTC. The 11-bit value of vertical total scanlines extends the maximum scanline capability to 2048 lines.

7.3.10 Vertical Display Enable Extension Register: ER71

I/O Port Address: 3CF

Index: 71

Bit	Description	Access	Reset State
7(MSB)	Vertical Display Enable End Bit 7	R/W	0
6	Vertical Display Enable End Bit 6	R/W	0
5	Vertical Display Enable End Bit 5	R/W	0
4	Vertical Display Enable End Bit 4	R/W	0
3	Vertical Display Enable End Bit 3	R/W	0
2	Vertical Display Enable End Bit 2	R/W	0
1	Vertical Display Enable End Bit 1	R/W	0
0(LSB)	Vertical Display Enable End Bit 0	R/W	0

Bit	Description
Bits 7:0	**Vertical Display Enable End Bits 7:0:** These are the lower eight bits of the 11-bit vertical display value that are used to specify the total number of displayable scan-lines in one vertical frame. Bits 8 and 9 are at ER78[6,1]. The most-significant bit, Bit 10, is at ER79[1].

7.3.11 Vertical Blank Start Extension Register: ER72

I/O Port Address: 3CF

Index: 72

Bit	Description	Access	Reset State
7(MSB)	Vertical Blank Start Bit 7	R/W	0
6	Vertical Blank Start Bit 6	R/W	0
5	Vertical Blank Start Bit 5	R/W	0
4	Vertical Blank Start Bit 4	R/W	0
3	Vertical Blank Start Bit 3	R/W	0
2	Vertical Blank Start Bit 2	R/W	0
1	Vertical Blank Start Bit 1	R/W	0
0(LSB)	Vertical Blank Start Bit 0	R/W	0

Bit	Description
Bits 7:0	**Vertical Blank Start Bits 7:0:** These are the lower eight bits of an 11-bit value that specify when the Vertical Blanking Signal becomes active. Bit 8 is in ER78[3]; Bits 9 and 10 are at ER79[2,3].

7.3.12 Vertical Blank End Extension Register: ER73

I/O Port Address: 3CF

Index: 73

Bit	Description	Access	Reset State
7(MSB)	Vertical Blank End Bit 7	R/W	0
6	Vertical Blank End Bit 6	R/W	0
5	Vertical Blank End Bit 5	R/W	0
4	Vertical Blank End Bit 4	R/W	0
3	Vertical Blank End Bit 3	R/W	0
2	Vertical Blank End Bit 2	R/W	0
1	Vertical Blank End Bit 1	R/W	0
0(LSB)	Vertical Blank End Bit 0	R/W	0

Bit	Description
Bits 7:0	**Vertical Blank End Bits 7:0:** These bits specify when the Vertical Blanking Signal becomes inactive. The internal Character Clock Counter is compared with this register. As soon as there is a match, the Blanking Signal will be terminated. The value in this register is calculated as follows: Vertical Blanking Start + Blanking Width = Vertical Blanking End.

7.3.13 Vertical Retrace Start Extension Register: ER74

I/O Port Address: 3CF

Index: 74

Bit	Description	Access	Reset State
7(MSB)	Vertical Retrace Start Bit 7	R/W	0
6	Vertical Retrace Start Bit 6	R/W	0
5	Vertical Retrace Start Bit 5	R/W	0
4	Vertical Retrace Start Bit 4	R/W	0
3	Vertical Retrace Start Bit 3	R/W	0
2	Vertical Retrace Start Bit 2	R/W	0
1	Vertical Retrace Start Bit 1	R/W	0
0(LSB)	Vertical Retrace Start Bit 0	R/W	0

Bit	Description
Bits 7:0	**Vertical Retrace Start Bits 7:0:** These bits specify when the Vertical Synchronization Signal becomes active. These bits represent eight of an 11-bit value. Bits 8 and 9 are in ER78[2,7]; Bit 10 is in ER79[4]. The polarity of the Vertical Synchronization Signal is controlled by Bit 7 of the MISC Output Register.

7.3.14 Vertical Retrace End Extension Register: ER75

I/O Port Address: 3CF

Index: 75

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Vertical Retrace End Bit 3	R/W	0
2	Vertical Retrace End Bit 2	R/W	0
1	Vertical Retrace End Bit 1	R/W	0
0(LSB)	Vertical Retrace End Bit 0	R/W	0

Bit	Description
Bits 7:4	Reserved
Bits 3:0	**Vertical Retrace End Bits 3:0:** These bits specify when the Vertical Synchronization Signal becomes inactive. The value programmed into this register is calculated by taking the least-significant four bits of the following: Vertical Retrace Start + Vertical Synchronization Width = Vertical Retrace End. The 4-bit value in this register will allow the Vertical Synchronization Signal width to be up to 16 scanlines wide. The Vertical Synchronization Signal should be inactive before the Vertical Blanking Signal goes inactive.

7.3.15 CR07 Extension Register: ER78

I/O Port Address: 3CF

Index: 78

Bit	Description	Access	Reset State
7(MSB)	Vertical Retrace Start Bit 9	R/W	0
6	Vertical Display Enable End Bit 9	R/W	0
5	Vertical Total Bit 9	R/W	0
4	Line Compare Bit 8	R/W	0
3	Vertical Blanking Start Bit 8	R/W	0
2	Vertical Retrace Start Bit 8	R/W	0
1	Vertical Display Enable End Bit 8	R/W	0
0(LSB)	Vertical Total Bit 8	R/W	0

Bit	Description
Bit 7	**Vertical Retrace Start Bit 9:** This bit is the Overflow Bit 9 of the Vertical Retrace Start Register, ER74.
Bit 6	**Vertical Display Enable End Bit 9:** This bit is the Overflow Bit 9 of the Vertical Display Enable End Register, ER71.
Bit 5	**Vertical Total Bit 9:** This bit is the Overflow Bit 9 of the Vertical Total Register, ER70.
Bit 4	**Line Compare Bit 8:** This bit is the Overflow Bit 9 of the Line Compare Register, CR18. This bit is always identical with CR07[4].
Bit 3	**Vertical Blanking Start Bit 8:** This bit is the Overflow Bit 8 of the Vertical Blanking Start Register, ER78.
Bit 2	**Vertical Retrace Start Bit 8:** This bit is the Overflow Bit 8 of the Vertical Retrace Start Register, ER74.
Bit 1	**Vertical Display Enable End Bit 8:** This bit is the Overflow Bit 8 of the Vertical Display Enable End Register, ER71.
Bit 0	**Vertical Total Bit 8:** This bit is the Overflow Bit 8 of the Vertical Total Register, ER70.

7.3.16 Vertical Overflow Register: ER79

I/O Port Address: 3CF

Index: 79

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Vertical Retrace Start Bit 10	R/W	0
3	Vertical Blank Start Bit 10	R/W	0
2	Vertical Blanking Start Bit 9	R/W	0
1	Vertical Display End Bit 10	R/W	0
0(LSB)	Vertical Total Bit 10	R/W	0

This register contains five overflow bits for the vertical parameters of the CRTC.

Bit	Description
Bits 7:5	Reserved
Bit 4	**Vertical Retrace Start Bit 10:** This is Bit 10 of the Vertical Retrace Start Field. It serves to extend CR7, making an 11-bit field.
Bit 3	**Vertical Blank Start Bit 10:** This is Bit 10 of the Vertical Blank Start Field. It serves to extend CR7, making an 11-bit field.
Bit 2	**Vertical Blanking Start Bit 9:** This is Bit 9 of the Vertical Blank Start Field. It serves to extend CR7.
Bit 1	**Vertical Display End Bit 10:** This is Bit 10 of the Vertical Display End Field. It serves to extend CR7, making an 11-bit field.
Bit 0	**Vertical Total Bit 10:** This is Bit 10 of the Vertical Total Field. It serves to extend CR7, making an 11-bit field.

7.3.17 Coarse Vertical Retrace Skew Register for Interlaced Modes: ER7A

I/O Port Address: 3CF

Index: 7A

Bit	Description	Access	Reset State
7(MSB)	CLKC Skew [7]	R/W	0
6	CLKC Skew [6]	R/W	0
5	CLKC Skew [5]	R/W	0
4	CLKC Skew [4]	R/W	0
3	CLKC Skew [3]	R/W	0
2	CLKC Skew [2]	R/W	0
1	CLKC Skew [1]	R/W	0
0(LSB)	CLKC Skew [0]	R/W	0

This register specifies the skew for the Odd Fields when interlaced video is being generated. In interlaced video, the scanlines of the Odd Field must be positioned (vertically) halfway between the corresponding scanlines of the Even Field. This register introduces up to 255 character-clock-periods of skew.

Bit	Description
Bits 7:0	**Vertical Retrace Skew Bits 7:0:** These eight bits specify the coarse skew in terms of character clock periods.

7.3.18 Screen A Start Address Register: ER7C

I/O Port Address: 3CF

Index: 7C

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Screen A Start Bit 19	R/W	0
2	Screen A Start Bit 18	R/W	0
1	Screen A Start Bit 17	R/W	0
0(LSB)	Screen A Start Bit 16	R/W	0

This register provides the four most-significant bits of the Screen A Start Address. The low-order 16 bits are contained in CRC and CRD in the CRT Controller Group.

Bit	Description
Bits 7:4	Reserved
Bits 3:0	**Screen A Start Bits:** These four bits are the high-order four bits of the 20-bit Screen A Start Address.

7.3.19 H/V Retrace Polarity Control Register: ER80

I/O Port Address: 3CF

Index: 80

Bit	Description	Access	Reset State
7(MSB)	Vertical Retrace Polarity	R/W	0
6	Horizontal Retrace Polarity	R/W	0
5	Source of Polarity Control	R/W	0
4	Enable Expanded Graphics	R/W	0
3	Reserved		0
2	Reserved		0
1	Reserved		0
0(LSB)	Reserved		0

This register contains polarity control bits for the CRTC.

Bit	Description
Bit 7	**Vertical Retrace Polarity:** This is a Control Bit for Vertical Retrace Polarity in the extension address space. If this bit is set to a '1', then polarity is negative (active-low). If this bit is set to a '0', the polarity is positive (active-high).
Bit 6	**Horizontal Retrace Polarity:** This is a control bit for Horizontal Retrace Polarity in the extension address space. If this bit is set to a '1', then polarity is negative (active-low). If this bit is set to a '0', the polarity is positive (active-high).
Bit 5	**Source of Polarity Control:** This bit sets the source of polarity control for both Vertical and Horizontal Sync. If this bit is set to a '1', then the source of control is from ER80[7,6]. If this bit is a '0', the source of control is from MISC[7,6].
Bit 4	**Enable Expanded Graphics:** This bit enables display expansion in Graphics Modes. When this bit is set to a '1', a predetermined ratio (16 to 19) of scanlines will be replicated in Graphics Mode. This bit can be programmed at any time.
Bits 3:0	Reserved

7.3.20 Display Mode Register: ER81

I/O Port Address: 3CF

Index: 81

Bit	Description	Access	Reset State
7(MSB)	SimulSCAN	R/W	0
6	Reserved		
5	Automap Enable	R/W	0
4	LCD Flat Panel Scan Control	R/W	0
3	CL-GD6340 Mode Enable	R/W	0
2	Reserved		
1	Reserved		
0(LSB)	Display Type	R/W	0

This register is used for specific display mode control.

Bit	Description
Bit 7	**SimulSCAN:** This bit determines if display information is being generated for the LCD only or for the LCD and CRT at the same time. A '1' indicates that the display mode is SimulSCAN; a '0' indicates LCD only.
Bit 6	Reserved
Bit 5	**Automap Enable:** This bit enables automatic mapping of color information to shades of gray. If it is set to a '1', AutoMap is enabled. If it is set to a '0', then automatic gray scaling does not occur.
Bit 4	**LCD Flat Panel Scan Control:** This bit determines support for single-scan or dual-scan LCD flat panels. If it is set to a '1', then single-scan flat panels are supported and internal half-frame buffer logic is disabled. If it is set to a '0', then support is set for dual-scan LCD flat panels.
Bit 3	**CL-GD6340 Mode Enable:** This bit affects the definition of Pin 98. If it is set to a '1', then the function of Pin 98 becomes DE (Display Enable for the CL-GD6340). If it is a '0', then Pin 98 becomes LLCLK.
Bits 2:1	Reserved
Bit 0	**Display Type:** This bit sets the active display type. If it is set to a '1', then the LCD flat panel is the active display. If it is set to a '0', then the CRT is active.

7.3.21 Character Clock Selection Register: ER82

I/O Port Address: 3CF

Index: 82

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Reserved		0	0
5	Reserved		0	0
4	Reserved		0	0
3	Disable SR1 Bit 0	R/W	0	
2	Char. Clock Width Select 2	R/W	0	
1	Char. Clock Width Select 1	R/W	0	
0(LSB)	Char. Clock Width Select 0	R/W	0	

This register is used to select the number of dot clocks in each character clock.

Bit	Description
Bits 7:4	Reserved: These bits should be programmed as shown above.
Bit 3	**Disable SR1 Bit 0 Functionality:** If this bit is set to a '1', the character clock width will be determined by Bits 2:0 of this register. If this bit is reset to a '0', the character clock width, Bit 0, will be determined by SR1 Bit 0.
Bits 2:0	**Character Clock Width Selects:** These three bits choose the number of dot clocks per character as indicated in the following table. The three bits are shown as a decimal number where Bit 2 is the MSB.

Table 7–1. Dot Clock/Character Clock

Value	Dot Clocks per Character Clock
0	9 Dots
1	8 Dots
2	4 Dots
3	Reserved
4	11 Dots
5	Reserved
6	Reserved
7	Reserved

7.3.22 Write Control Register: ER83

I/O Port Address: 3CF

Index: 83

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Attribute Registers Write Protect	R/W	0
5	Reserved		0
4	CRTC Total/Retrace Effect Protect	R/W	0
3	CRTC Blank Effect Protect	R/W	0
2	CRTC Vertical Display End Effect Protect	R/W	0
1	CRTC Display Timing Effect Protect	R/W	0
0(LSB)	CRTC Vertical Monitor Write Protect	R/W	0

This register is used to provide write protection for the Horizontal and Vertical Working Sets.

Bit	Description
Bit 7	Reserved
Bit 6	**Attribute Registers Write Protect:** This bit provides hardware-level write protection of the internal attribute controller palette registers, AR00-AR0F, preventing them from being changed by application programs. If this bit is set to a '1', protection is in effect. If the bit is set to a '0', protection is disabled.
Bit 5	Reserved
Bit 4	**CRTC Total/Retrace Effect Protect:** When this bit is set to a '1', the CRTC is controlled by the CRTC extension registers, which now become the Working Set. This, in effect, protects the standard VGA CRTC Registers CR00, CR04, CR05[4:0], CR06, CR07[7,5,2,0], CR10, and CR11. These registers become read-only. Writing to them will not affect the CRTC. When this bit is a '0', the standard CRTC registers have control. Data written to the standard address path, 3x4h, will also be written to the Working Set.
Bit 3	**CRTC Blank Effect Protect:** This bit operates the same as Bit 4 except the registers affected are CR02, CR03[4:0], CR05[7], CR07[3], CR9[5], CR15, and CR16.
Bit 2	**CRTC Vertical Display End Effect Protect:** This bit operates the same as Bits 4 and 3 except the affected registers are CR12 and CR07[6,1].
Bit 1	**CRTC Display Timing Effect Protect:** This bit operates the same as Bits 4, 3, and 2 except the affected registers are CR07[6,1], CR09, CR0A, CR0B, CR12, and CR14.
Bit 0	**CRTC Vertical Parameters Write Protect:** This bit operates the same as Bits 4, 3, 2, and 1 except the affected registers are CR06, CR07[7,5,3,2,0], CR09[5], CR10, CR11[3:0], CR15, and CR16.

7.3.23 Clock Select Register: ER84

I/O Port Address: 3CF

Index: 84

Bit	Description	Access	Reset State
7(MSB)	Source of Clock Selection 1:0	R/W	0
6	Reserved		
5	Clock Selection 3	R/W	1
4	Clock Selection 2	R/W	0
3	Clock Selection 1	R/W	0
2	Clock Selection 0	R/W	0
1	ClkIn /2	R/W	0
0(LSB)	Reserved		

This register is used to program the Video Clock Section of the Dual-frequency Synthesizer. Bits 3:2 of the MISC Register (External Group) can be selected to replace Bits 3:2 of this register. See the description for ER9E for information on programming the SQCLK Section of the Dual-frequency Synthesizer.

Bit **Description**

Bit 7 **Source of Clock Selection:** If this bit is set to a '1', then Bits 5:2 of this register are used to program the synthesizer. If this bit is reset to a '0', then Bits 5:4 of this register and Bits 3:2 of the MISC Register (External/General Registers) are used to program the synthesizer. This is shown in the table below:

Table 7–2. VDCLK Select Code Source

ER84[7]	CLKSEL3	CLKSEL2	CLKSEL1	CLKSEL0
1	ER84[5]	ER84[4]	ER84[3]	ER84[2]
0	ER84[5]	ER84[4]	MISC[3]	MISC[2]

Bit 6 Reserved

7.3.23 Clock Select Register: ER84 *(cont.)*

Bit	Description
Bits 5:2	**Clock Selection 3-0:** These four bits are used to program the Video Clock Section of the Dual-frequency Synthesizer. If Bit 7 is a reset to a '0', then Bits 3:2 of the MISC Register replace Bits 3:2 of this register as shown in Table 7–2 above. The following table enumerates the available frequencies:

Table 7–3. VDCLK Select Code vs. Frequencies

VDCLK Select Code	Frequency (MHz)	Mode(s)	(ER84)
0000	Reserved		80
0001	65.028	1024 x 768 at 60 Hz	84
0010	85 (Future)	1024 x 768 at 76 Hz	88
0011	36	800 x 600 at 56 Hz	8C
0100	25.175	VGA Graphics Modes	90
0101	28.318	VGA Text Modes	94
0110	24.017		98
0111	39.999	800 x 600 at 60 Hz 132-Column Text Modes	9C
1000	44.907	1024 x 768 at 87 Hz, Interlaced	A0
1001	50.344	640 x 480, Direct-Color	A4
1010	31.5	VESA, 72 Hz (Mode 12)	A8
1011	32.514	100-Column Text Modes	AC
1100	63.0	Direct-Color, VESA, 72 Hz	B0
1101	72 (Future)	800 x 600, Direct-Color, 56 Hz	B4
1110	75 (Future)	1024 x 768 at 70 Hz	B8
1111	80 (Future)	800 x 600, Direct-Color, 60 Hz	BC

Bit 1	**ClkIn/2:** This bit, when set to a '1', will implement an additional divide by 2 for the frequency selected by Bits 5:2. This feature is primarily used for 3-MHz LCD panels where SimulSCAN support is not required. When this bit is set to a '0' there is no effect.
Bit 0	Reserved

7.3.24 CRTC Test Register: ER86

I/O Port Address: 3CF

Index: 86

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	CRTC Outputs Three-State Control	R/W	0
3	Reserved		0
2	Reserved		0
1	Reserved		0
0(LSB)	Reserved		0

This register is used to configure the CL-GD6410 during factory testing. This register should never be modified by an application program, and is described here for information only.

Bit	Description
Bits 7:5	Reserved
Bit 4	**CRTC Outputs Three-State Control:** If this bit is set to a '1', the HSYNC and VSYNC Outputs will be placed in the high-impedance (three-state) condition.
Bits 3:0	Reserved

7.3.25 CRTC Spare Extension Register: ER87 (Rev. B Only)

I/O Port Address: 3CF

Index: 87

Bit	Description	Access	Reset State
7(MSB)	Invert VDE* on Pin 99	R/W	0
6	Reserved		0
5	Reserved		0
4	VDE* / LFS Configuration on Pin 99	R/W	0
3	Reserved		0
2	Reserved		0
1	Reserved		0
0(LSB)	Reserved		0

This register is used for pin configuration in the CL-GD6410-B only. ER87 is unused in the CL-GD6410-A.

Bit	Description
Bits 7:5	**Invert VDE on Pin 99:** This bit controls the polarity of Pin 99 when the pin is configured as VDE* according to Bit 4 of this register. If this bit is set to '1', VDE is active-high. If this bit is set to '0', VDE is active-low true.
Bit 4	**VDE* / LFS Configuration of Pin 99:** This bit controls the function of Pin 99. If this bit is set to a '1', Pin 99 is defined as VDE*. If this bit is set to '0', then Pin 99 is defined as LFS.
Bits 3:0	Reserved

7.3.26 CRTC BIOS Configuration Register: ER8F

I/O Port Address: 3CF

Index: 8F

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Clock Select Pinout Configuration	R/W	0
0(LSB)	Clock Select Pinout Configuration	R/W	0

This register is used to select between an external synthesizer and a specific group of external oscillators. It must be reset to a '0' when the Dual-frequency Synthesizer is used.

Bit	Description
Bits 7:2	Reserved
Bits 1:0	**Clock Select Pinout Configuration:** These two bits are used to choose the Clock Select Configuration as shown in the following table:

Table 7–4. Clock Select Configurations

Value	Configuration
0	Clock Synthesizer or Multiplexer
1	External Oscillators Configuration 1
2	External Oscillators Configuration 2
3	External Oscillators Configuration 3

7.3.26 CRTC BIOS Configuration Register: ER8F *(cont.)*

Bit **Description**

The following table indicates the nominal frequencies that are expected on each pin for Configurations 1, 2, and 3:

Table 7–5. External Oscillator Expectations

Input Pin	Config. 1	Config. 2	Config. 3
OSC	14 MHz	36 MHz	36 MHz
CLKSEL0	32 MHz	45 MHz	65 MHz
CLKSEL1	25 MHz	50 MHz	50 MHz
CLKSEL2	28 MHz	56 MHz	56 MHz
CLKSEL3	24 MHz	40 MHz	40 MHz

7.3.27 Display Memory Control Register: ER90

I/O Port Address: 3CF

Index: 90

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6 (-A)	Reserved (Rev. A)		0	0
6 (-B)	Power Sequencing Status Bit (Rev. B)	R	0	
5	Reserved		0	0
4	Reserved		0	0
3	Display Memory Refresh Ext.	R/W	0	
2	Reserved		0	0
1	RAS Precharge	R/W	0	
0(LSB)	Scanline Double Control	R/W	0	

This register is used in the configuration of Display Memory. Each bit used controls an individual element of the configuration.

Bit	Description
Bit 7	Reserved: This bit should be programmed as shown above.
Bit 6 (-A)	Reserved: This bit should be programmed as shown above. (Rev. A only)
Bit 6 (-B)	**Power Sequencing Status BitDisplay:** This bit is read-only.When this bit is high when read, then a power-sequencing cycle is in progress. This bit is used in the CL-GD6410 Revision B only.
Bits 5:4	Reserved: These bits should be programmed as shown above.
Bit 3	**Display Memory Refresh Extension:** This bit is used in conjunction with Bit 6 of CR11 (in the CRTC Group) to specify the number of refresh cycles per scanline. The number is chosen to guarantee an average of one refresh cycle every 16 microseconds (typically). The horizontal period is divided by 16 microseconds, and the result increased to the next integer. The table below indicates the number of refresh cycles executed per horizontal period:

Table 7–6. Refresh Cycle Select

ER90[3]	CR11[6]	Refresh Cycles
0	0	3
0	1	5
1	0	1
1	1	1

7.3.27 Display Memory Control Register: ER90 *(cont.)*

Bit	Description
Bit 2	Reserved: This bit should be programmed as shown above.
Bit 1	**RAS Precharge:** If this bit is set to a '1', the CL-GD6410 will be configured for normal RAS Precharge (three SQCLK cycles). If this bit is set to a '0', the CL-GD6410 will be programmed for Extended-RAS Precharge (four SQCLK cycles).
Bit 0	**Scanline Double Control:** If this bit is set to a '1', each scanline will be sent to the display twice. This is appropriate when displaying Low-resolution Modes (e.g., 640 x 200) on higher-resolution monitors (e.g., 640 x 400). If this bit is reset to a '0', each scanline will be displayed just once per frame.

7.3.28 CRT-Circular Buffer Policy Selection Register: ER91

I/O Port Address: 3CF

Index: 91

Bit	Description	Access	Reset State	Programmed
7(MSB)	CBP7	R	0	
6	CBP6	R	0	
5	CBP5	R/W	0	0
4	CBP4	R/W	0	0
3	CBP3	R/W	0	0
2	CBP2	R/W	0	0
1	CBP1	R/W	0	0
0(LSB)	CBP0	R/W	0	0

This register should never be modified by an application program, and is described here for information only.

Bit	Description
Bits 7:0	**CBP7-CBP0:** These bits should be programmed as shown above, or as determined by the Video BIOS.

7.3.29 Font Control Register: ER92

I/O Port Address: 3CF

Index: 92

Bit	Description	Access	Reset State	Programmed
7(MSB)	Enable Expanded Text	R/W	0	
6	Text Expansion Method Select	R/W	0	
5	Enable Full Height Cursor	R/W	0	
4	Reserved		0	0
3	Enable Software Expanded Text	R/W	0	
2	Reserved		0	0
1	Font Address 17	R/W	0	
0(LSB)	Font Address 16	R/W	0	

Bit	Description
Bit 7	**Enable Expanded Text:** When this bit is set to a '1', the hardware will expand 16-scanline text to 19-scanline text. The three extra scanlines are controlled by Bit 6 of this register. This bit is only used in Text Modes. Setting this bit to a '0' disables text expansion.
Bit 6	**Text Expansion Method Select:** When this bit is set to a '1', Scanlines 0, 8, and 15 are duplicated in expanded text. When this bit is set to a '0', Scanline 0 is repeated twice, and Scanline 15 is repeated once. This bit is effective only when Bit 7 is set to a '1'.
Bit 5	**Enable Full-height Cursor:** When this bit is set to a '1', a full-height cursor will be generated independently of Cursor-start and Cursor-end Registers. The purpose is to make the cursor more easily visible on the LCD panel.
Bit 4	Reserved: This bit should be programmed as shown above.
Bit 3	**Enable Software Expanded Text:** When this bit is set to a '1', the Video BIOS or video drivers have to supply the expanded font. ER30-ER33 will control the CRTC to generate expanded fonts (typically with 19-high character cells) independently. The corresponding standard registers in the CRTC can be read and written to, but they are no longer used to drive the font display. This bit takes effect in Text Modes only.
Bit 2	Reserved: This bit should be programmed as shown above.
Bits 1:0	**Font Address:** These bits are used for font control address extension. These bits are also used for bold-font selection, as an alternate font in 16- and 32-bit-wide video memory configurations.

7.3.30 CRT-Circular Buffer Delta and Burst Register: ER95

I/O Port Address: 3CF

Index: 95

Bit	Description	Access	Reset State	Programmed
7(MSB)	BURST [3]	R/W	0	0
6	BURST [2]	R/W	0	0
5	BURST [1]	R/W	0	0
4	BURST [0]	R/W	0	0
3	DELTA [3]	R/W	0	0
2	DELTA [2]	R/W	0	0
1	DELTA [1]	R/W	0	0
0(LSB)	DELTA [0]	R/W	0	0

This register should never be modified by an application program, and is described here for information only.

Bit	Description
Bits 7:0	**BURST[3:0] and DELTA[3:0]:** These bits should be programmed as shown above.

7.3.31 Display Memory Control Test Register: ER96

I/O Port Address: 3CF

Index: 96

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Reserved		0	0
5	Reserved		0	0
4	Reserved		0	
3	DM Bus Three-State	R/W	0	
2	MD 0,2 Three-State	R/W	0	
1	Reserved		0	
0(LSB)	Latch Monitor ID	R/W	0	

Bit	Description
Bits 7:5	Reserved: These bits should be programmed as shown above.
Bit 4	Reserved
Bit 3	**Display Memory Bus Three-State:** If this bit is set to a '1', the Address and Control Pins of the Memory Sequencer will be put into high-impedance. These are AA[8:0], AB[8:0] OE*, WE*, RAS*, and CAS*. If this bit is reset to a '0', the address and control pins will be active-high or active-low for normal operation.
Bit 2	**Memory Data 0,2 Three-State:** If this bit is set to a '1', the M0D and M2D Buses will be put into high-impedance. If this bit is reset to a '0', these buses will behave normally.
Bit 1	Reserved
Bit 0	**Latch Monitor ID:** If this bit is set to a '1', the Monitor ID Bits will be latched just as if reset was being asserted at power-on time. See the description for ER9C. Before setting this bit to a '1', the program must force the screen to blank. Before reading the MONID Register, the program should wait one full-frame time with no screen-refresh cycles. To initiate the latching mechanism, this bit must be programmed to a '1', then to a '0'. The read function occurs when this bit is a '1'; the latch occurs when this bit returns to a '0'.

7.3.32 Monitor Switches Read-Back Register: ER97

I/O Port Address: 3CF

Index: 97

Bit	Description	Access	Default State
7(MSB)	SW7	R	0
6	SW6	R	0
5	SW5	R	0
4	SW4	R	0
3	Reserved	R	0
2	Reserved	R	0
1	Reserved	R	0
0(LSB)	Reserved	R	0

Bits 7:0 of this register are for read-only configuration. These bits reflect the presence or absence of pull-up resistors on several of the MD Bits (Memory Data). The optional configuration resistors described in Register ER99 have no direct effect on the hardware. They are sensed by the Cirrus Logic BIOS at reset time, and whenever ER96[0] is toggled. The meanings described below are assigned by the Cirrus Logic BIOS.

Bit	Description		
Bits 7:4	**Default**	**Pin**	**Default Meaning**
	0	FRAD0	Reserved for BIOS
	0	FRAD1	Reserved for BIOS
	0	FRAD2	Panel Class
	0	FRAD3	Panel Class
Bits 3:0	Reserved		

7.3.33 Scratch Register: ER98

I/O Port Address: 3CF

Index: 98

Bit	Description	Access	Reset State
7(MSB)	Scratch Bit 7	R/W	x
6	Scratch Bit 6	R/W	x
5	Scratch Bit 5	R/W	x
4	Scratch Bit 4	R/W	x
3	Scratch Bit 3	R/W	x
2	Scratch Bit 2	R/W	x
1	Scratch Bit 1	R/W	x
0(LSB)	Scratch Bit 0	R/W	x

Bit	Description
Bits 7:0	**Scratch Bits 7-0:** This register has no effect on the operation of the CL-GD6410. It is reserved for BIOS use.

7.3.34 Configuration Register: ER99

I/O Port Address: 3CF

Index: 99

Bit	Description	Access	Default State
7(MSB)	Reserved	R	0
6	Reserved	R	0
5	Reserved	R	0
4	BIOS Width	R	0
3	Sleep Location	R	1
2	Reduced Decode	R	0
1	ISA Bus	R	0
0(LSB)	Enable C000:0 BIOS	R	1

This is a read-only configuration register. It reflects the presence or absence of pull-up resistors on several pins. It is updated at reset time or whenever ER96[0] is toggled. The configuration resistors described in this register have a direct effect on the hardware.

Bit	Description		
Bits 7:0	**Default**	**Pin**	**Default State**
	0	PD7	Reserved
	0		Reserved
	0		Reserved
	0	FRA8	BIOS Width (8- or 16-bit)
	1	FRA7	Sleep Location (3C3h or 46E8h)
	0	FRA6	Reserved
	0	FRA5	ISA Bus
	1	FRA4	Enable ROM Decode (C000:0)

7.3.35 Display Memory Configuration Register: ER9A

I/O Port Address: 3CF

Index: 9A

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Reserved		0	0
5	Reserved		0	0
4	Reserved		0	0
3	Reserved		0	0
2	Reserved		0	0
1	Reserved		0	0
0(LSB)	Reserved		0	0

This register is used to choose memory-width configuration.

Bit	Description
Bits 7:0	Reserved: These bits should be programmed as shown above.

7.3.36 Miscellaneous Configuration Register: ER9B

I/O Port Address: 3CF

Index: 9B

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	LLCLK/DE Pin Config.	R/W	0	
5	LLCLK/DE Pin Config.	R/W	0	
4	INTERNAL/MOD Pin Config.	R/W	0	
3	INTERNAL/MOD Pin Config.	R/W	0	
2	Reserved		0	0
1	On-Chip Monitor Sense Ena.	R/W	0	
0(LSB)	SQCLK Inversion	R/W	0	

Bit	Description
Bits 7	Reserved: This bit should be programmed as shown above.
Bits 6:5	**LLCLK/DE Pin Configuration:** These two bits configure the function of Pin 98 as shown in the following table. These bits have no effect if ER81[3] is set to a '1' (CL-GD6340 Mode Enable).

Table 7–7. LLCLK/DE Pin Configuration

Bit 6	Bit 5	Pin Function
0	0	LLCLK (Default at Power-On)
0	1	DE (for the CL-GD6340)
10 - 11		Reserved

Bits 4:3 **INTERNAL/MODULATION Pin Configuration:** These two bits configure the function of Pin 100 as shown in the following table.

Table 7–8. INTERNAL/MODULATION

Bit 4	Bit 3	Pin Function
0	0	INTERNAL (Default at Power-On)
0	1	MODULATION (for the LCD panel)
10 - 11		Reserved

7.3.36 Miscellaneous Configuration Register: ER9B *(cont.)*

Bit	Description
Bit 2	Reserved: This bit should be programmed as shown above.
Bit 1	**On-Chip Monitor Sense Enable:** If this bit is reset to a '0', the On-chip Monitor Sense is enabled.
Bit 0	**SQCLK Phase Inversion:** When this bit is set to '1', the phase of the SQCLK (Memory Clock) is inverted. When this bit is set to '0', SQCLK phase is normal.

7.3.37 PS/2 Monitor ID Register: ER9C

I/O Port Address: 3CF

Index: 9C

Bit	Description	Access	Reset State
7(MSB)	PS/2 Monitor ID 2	R	
6	PS/2 Monitor ID 1	R	
5	PS/2 Monitor ID 0	R	
4	Reserved		0
3	Reserved		0
2	Reserved		0
1	Reserved		0
0(LSB)	Reserved		0

This read-only configuration register returns a value corresponding to the PS/2 Monitor connected to Pins M0D[7:5]. The levels on these pins are sensed when RESET goes active, or whenever ER96[0] is toggled.

Bit	Description		
Bits 7:5	**Description** PS/2 Monitor ID 010: 8514 Monitor 101: 8503 Monitor 110: 8512/8513 Monitor 111: No Monitor	**Default** (none)	**MD Pin** M0D[7:5]
Bits 4:0	Reserved. These bits are reserved, and the value returned is a '0'.		

7.3.38 Bus Interface Unit Control Register: ERA0

I/O Port Address: 3CF

Index: A0

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	CPU Address Scramble Disable	R/W	0
5	Enable 16-bit I/O	R/W	0
4	Enable 16-bit Memory	R/W	0
3	MEMCS16* Mode Select	R/W	0
2	RAMDAC RAM Write Protect	R/W	0
1	Disable Sleep Mechanism	R/W	0
0(LSB)	Disable ROM BIOS	R/W	0

This register is used, in conjunction with other Extension Registers in the ERAX range, to configure the Bus Interface Unit (host interface).

Bit	Description
Bit 7	Reserved
Bit 6	**CPU Address Scramble Disable:** If this is set to a '1', SR3[3,1] address scrambling is disabled.
Bit 5	**Enable 16-bit I/O:** If this is set to a '1', 16-bit I/O response is enabled. If this bit is reset to a '0', all I/O operations will be executed in 8-bit Mode.
Bit 4	**Enable 16 bit Memory:** This bit is used with Bit 4 of ER9A to configure the modes in which the CL-GD64XX will respond to 16-bit memory accesses with MEMCS16*. See the following table for details:

Table 7–9. MEMCS16 Modes

ERA0[4]	ERA9[4]	Description
0	x	8-bit operation in all modes
1	0	16-bit operation in Odd/Even or Chain4 Modes 8-bit operation in Planar Mode
1	1	16-bit operation in all modes

7.3.38 Bus Interface Unit Control Register: ERA0 *(cont.)*

Bit	Description
Bit 3	**MEMCS16* Mode Select:** If this bit is set to a '1', the entire Memory Address Range A000:0 to BFFF:F and C000:0 to C7FF:F will be decoded as valid for 16-bit memory operations. If this bit is reset to a '0', only the sub-range required for the current Video Mode will be decoded as valid for 16-bit memory operations.
Bit 2	**RAMDAC RAM Write Protect:** If this bit is set to a '1', then the internal RAMDAC RAM is write protected. This bit should be set only in LCD Mode when it is preferred that the application program not to change the grayscale values.
Bit 1	**Disable Sleep Mechanism:** If this bit is set to a '1', the Sleep Mechanism is disabled (3C3 or 46E8). Accesses to the Sleep Mechanism Address will be ignored. If this bit is reset to a '0', the Sleep Mechanism is enabled and operates normally.
Bit 0	**Disable ROM BIOS:** If this bit is set to a '1', the ROM BIOS is disabled and accesses in the range C000:0 will be ignored. If this bit is reset to a '0', the ROM BIOS is enabled and operates normally. This bit must be reset to a '0'.

7.3.39 Three-State and Test Control Register: ERA1

I/O Port Address: 3CF

Index: A1

Bit	Description	Access	Reset State	Programmed
7(MSB)	Disable IOR	R/W	0	
6	Reserved		0	0
5	Reserved		0	0
4	Reserved		0	0
3	Three-State Control	R/W	0	
2	Reserved		0	0
1	Reserved		0	0
0(LSB)	Reserved		0	0

This register contains bits that are used for testing the Bus Interface Unit (host interface). This register should never be modified by an application program.

Bit	Description
Bit 7	**Disable IOR*:** When this bit is set to a '1', I/O reads are disable to the CL-GD6410. This feature is used primarily for testing and should not be programmed by any application.
Bits 6:4	Reserved: These bits should be programmed as shown above.
Bit 3	**Three-State Control on I/O Pins:** If this bit is set to a '1', all Output and I/O Pins are forced into the high-impedance state.
Bits 2:0	Reserved: These bits should be programmed as shown above.

7.3.40 BIOS Page Selection Register: ERA2

I/O Port Address: 3CF

Index: A2

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Reserved		0
2	BIOS Page [2]	R/W	0
1	BIOS Page [1]	R/W	0
0(LSB)	BIOS Page [0]	R/W	0

This register contains bits that are used for BIOS pagination in the event that EPROMs are being used for the Video BIOS.

Bit	Description
Bits 7:3	Reserved
Bits 2:0	**BIOS Pagination Bits**: These bits are used as a method of extending the normal VGA address space occupied by the Video BIOS. The pagination method is indicated in the following table:

Table 7–10. BIOS Pagination

Bit 2	Bit 1	Bit 0	Description
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Page 0 (Address Range 25K bytes to 32K bytes)
1	0	0	Page 1 (Address Range 33K bytes to 40K bytes)
1	0	1	Page 2 (Address Range 41K bytes to 48K bytes)
1	1	0	Page 3 (Address Range 49K bytes to 56K bytes)
1	1	1	Page 4 (Address Range 57K bytes to 64K bytes)

7.3.41 Wait State Controls Register: ERA6

I/O Port Address: 3CF

Index: A6

Bit	Description	Access	Reset State	Programmed
7(MSB)	Bus Width Status	R	0	
6	BIOS Wait State Control	R/W	0	
5	Reserved		0	0
4	I/O Write Wait Control	R/W	0	
3	RAMDAC Wait Control	R/W	0	
2	0WS* for Memory Write	R/W	0	
1	I/O Read Wait Control	R/W	0	
0(LSB)	Display Memory Write Wait Control	R/W	0	

This register is used to control the insertion of wait states in various host accesses. This register should never be modified by an application program.

Bit	Description
Bit 7	**Bus Width Status:** This is a read-only bit. If a '1' is returned, the CL-GD6410 has detected at least one transition on SBHE*, indicating it is connected to a 16-bit interface.
Bit 6	**BIOS Wait State Control:** Setting this bit to a '1', allows for the BIOS to operate with zero wait states. In most cases, this bit will be a '0'.
Bit 5	Reserved: This bit should be programmed as shown above.
Bit 4	**I/O Write Wait Control:** If this bit is set to a '1', no wait states will be inserted for I/O writes. If this bit is reset to a '0', wait states corresponding to one additional SQCLK period will be inserted for I/O writes.
Bit 3	**RAMDAC Wait Control:** If this bit is set to a '1', no wait states will be inserted for I/O Read or Write accesses to the external RAMDAC. If this bit is reset to a '0', wait states corresponding to one additional SQCLK period will be inserted for I/O read or write accesses to the external RAMDAC.
Bit 2	**0WS* for Memory Write:** If this bit is set to a '1', 0WS* will be asserted for Display Memory writes (that can be executed immediately). If this bit is reset to a '0', 0WS* will not be asserted for any Display Memory writes.
Bit 1	**I/O Read Wait Control:** If this bit is set to a '1', no wait states will be inserted for I/O reads. If this bit is reset to a '0', wait states corresponding to one additional SQCLK period will be inserted for I/O reads.
Bit 0	**Display Memory Write Wait Control:** If this bit is set to a '1', no wait states will be inserted for Display Memory writes. If this bit is reset to a '0', wait states corresponding to one additional SQCLK period will be inserted for Display Memory writes.

7.3.42 General Programmable I/O Port Control: ERA7

I/O Port Address: 3CF

Index: A7

Bit	Description	Access	Reset State
7(MSB)	PWG Status	R/W	0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Reserved		0
2	PO2 Control	R/W	0
1	PO1 Control	R/W	0
0(LSB)	Reserved		0

Bit	Description
Bit 7	**PWG Status:** This pin indicates the status of the Power-Good Pin (Pin 9). In a normal power-on state, this bit will be a '1'.
Bits 6:4	Reserved
Bits 2:1	**Programmable Output Pin Configuration:** These two bits are used to activate the programmable output pins as shown in the following table:
Bit 0	Reserved

Table 7–11. Programmable Output Pin Configurations

Bit 2	Bit 1	PO1 (Pin10)	PO2 (Pin11)
0	0	Inactive	Inactive
0	1	Active	Inactive
1	0	Inactive	Active
1	1	Active	Active

7.3.43 Bus Interface Unit Cache Controls Register: ERA9

I/O Port Address: 3CF

Index: A9

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Internal BIUC Timing 1	R/W	0	
5	Internal BIUC Timing 0	R/W	0	
4	Reserved		0	0
3	Enable Compaction in Modes 2 and 3	R/W	0	
2	Reserved		0	0
1	Enable Read Cache	R/W	0	
0(LSB)	Reserved		0	0

This register controls options regarding the Bus Interface Unit (host interface). This register should never be modified by an application program.

Bit	Description
Bit 7	Reserved: This bit should be programmed as shown above.
Bits 6:5	**Internal BIUC Timings:** These two bits control the Internal BIU Timing delay, and must be programmed according to the period of the Sequencer Clock (SQCLK). The following table indicates the limits:

Table 7–12. Internal BIUC Timing

Value	SQCLK Period	SQCLK Frequency
00	20-23 ns	49.09
01	23-25 ns	43.90
10	25-29 ns	35.90
11	–	–

Bit 4	Reserved: This bit should be programmed as shown above.
Bit 3	**Enable Compaction in Modes 2 and 3:** If this bit is set to a '1', write-overwrite compaction is enabled for Write Modes 2 and 3. If this bit is reset to a '0', write-overwrite compaction is not enabled for Write Modes 2 and 3.

7.3.43 Bus Interface Cache Controls Register: ERA9 *(cont.)*

Bit	Description
Bit 2	Reserved: This bit should be programmed as shown above.
Bit 1	**Enable Read Cache:** If this bit is set to a '1', the CPU Data Latches can be used as a source of data for CPU reads. If this bit is reset to a '0', the function is disabled and all CPU reads must be satisfied from the Display Memory.
Bit 0	Reserved: This bit should be programmed as shown above.

7.3.44 Design Revision Register: ERAA

I/O Port Address: 3CF

Index: AA

Bit	Description	Access	Reset State
7(MSB)	CL-GD6410 Revision 7	R	0
6	CL-GD6410 Revision 6	R	1
5	CL-GD6410 Revision 5	R	1
4	CL-GD6410 Revision 4	R	0
3	CL-GD6410 Revision 3	R	1
2	CL-GD6410 Revision 2	R	1
1	CL-GD6410 Revision 1	R	1
0(LSB)	CL-GD6410 Revision 0	R	1

This Read-only Register returns a unique value that is factory-programmed into the CL-GD6410.

Bit	Description
Bit 0	**Design Revision:** These eight bits identify the chip revision level.

7.3.45 Mask Revision Register: ERAB

I/O Port Address: 3CF

Index: AB

Bit	Description	Access	Reset State
7(MSB)	CL-GD6410 Mask Revision 7	R	0
6	CL-GD6410 Mask Revision 6	R	1
5	CL-GD6410 Mask Revision 5	R	1
4	CL-GD6410 Mask Revision 4	R	0
3	CL-GD6410 Mask Revision 3	R	1
2	CL-GD6410 Mask Revision 2	R	1
1	CL-GD6410 Mask Revision 1	R	1
0(LSB)	CL-GD6410 Mask Revision 0	R	1

This Read-only Register returns a unique value that is factory-programmed into the CL-GD6410.

Bit	Description
Bit 0	**Mask Revision:** These eight bits identify the chip-mask-revision level.

7.3.46 Scratch Registers 5-0: ERBA-BF

I/O Port Address: 3CF

Index: BA-BF

Bit	Description	Access	Reset State
7(MSB)	Scratch Register 7	R/W	0
6	Scratch Register 6	R/W	0
5	Scratch Register 5	R/W	0
4	Scratch Register 4	R/W	0
3	Scratch Register 3	R/W	0
2	Scratch Register 2	R/W	0
1	Scratch Register 1	R/W	0
0(LSB)	Scratch Register 0	R/W	0

Bit	Description
Bits 7:0	**Scratch Registers:** These six registers have no effect on the operation of the CL-GD6410. These registers are reserved for the exclusive use of the Cirrus Logic BIOS.

7.3.47 Attribute and Graphics Control Register: ERC0

I/O Port Address: 3CF

Index: C0

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Reserved		0	0
5	Reserved		0	0
4	Reserved		0	0
3	Background Color Enhancement	R/W	0	
2	Reserved		0	
1	Bypass Internal Palettes	R/W	0	
0(LSB)	Foreground Color Enhancement	R/W	0	

Bit	Description
Bits 7:4	Reserved: These bits should be programmed as shown above.
Bit 3	**Background Color Enhancement:** If this bit is set to a '1', then the contrast ratio for background and foreground colors is enhanced by the following formula: If Foreground Color = 0 Background Color = 7 else Background Color = 0 If this bit is set to a '0', then normal background color applies.
Bit 2	Reserved
Bit 1	**Bypass Internal Palettes:** If this bit is set to a '1', the Internal Palette (AR0-F) is bypassed. If this bit is reset to a '0', the internal palette is used.
Bit 0	**Background Color Enhancement:** If this bit is set to '1', the intensity bit of the foreground color will be XOR, except when the foreground color = 0 or 8. If this bit is set to a '0', normal foreground color applies.

7.3.48 Cursor Attributes Register: ERC1

I/O Port Address: 3CF

Index: C1

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Reserved		0	0
5	Force Cursor Color	R/W	0	
4	Invert Border Color	R/W	0	
3	Cursor Mode	R/W	0	
2	Cursor Blink Rate 1	R/W	0	
1	Cursor Blink Rate 0	R/W	0	
0(LSB)	Cursor Blink Disable	R/W	0	

This register controls the cursor in CL-GD6410.

Bit	Description
Bits 7:6	Reserved: These bits should be programmed as shown above.
Bit 5	**Force Cursor Color:** If this bit is set to a '1', cursor color is forced to black and white in LCD mode. If set to '0', the cursor color is normal.
Bit 4	**Invert Border Color:** If this bit is set to a '1', the bits of the border color (see AR11) are inverted. If this bit is reset to a '0', the bits of the border color are not inverted.
Bit 3	**Cursor Mode:** If this bit is set to a '1', the cursor is displayed by inverting the screen 'behind' the cursor. If this bit is reset to a '0', the cursor is displayed by replacing the screen 'behind' the cursor.
Bits 2:1	**Cursor Blink Rate:** This two-bit field controls the cursor blinking rate if enabled by Bit 0. The following table shows the blink rates:
Bit 0	**Cursor Blink Disable:** If this bit is set to a '0', cursor blinking is enabled at the rate specified in Bits 2:1. If this bit is reset to a '1', cursor blinking is disabled and Bits 2:1 are ignored.

Table 7–13. Blink Rates

Value	Blink Rate	Note
00	Vertical Scan Rate/16	Normal
01	Vertical Scan Rate/32	Slow
10	Vertical Scan Rate/8	Fast
11	Vertical Scan Rate/4	Frantic

7.3.49 Graphics Controller Memory Latches 0-3 Register: ERC2-C5

I/O Port Address: 3CF

Index: C2-C5

Bit	Description	Access	Reset State
7(MSB)	Reserved	R/W	0
6	Reserved	R/W	0
5	Reserved	R/W	0
4	Reserved	R/W	0
3	Reserved	R/W	0
2	Reserved	R/W	0
1	Reserved	R/W	0
0(LSB)	Reserved	R/W	0

Bit	Description
Bits 7:0	Reserved

7.3.50 RAMDAC Controls Register: ERC8

I/O Port Address: 3CF

Index: C8

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved		0	0
6	Reserved		0	0
5	Blank to RAMDAC	R/W	0	
4	Reserved	R/W	0	0
3	Reserved	R/W	0	0
2	Reserved	R/W	0	0
1	Ext. 16-Color Modes	R/W	0	
0(LSB)	Reserved		0	0

This register is used to control the integrated RAMDAC. This register should never be modified by an application program.

Bit	Description
Bits 7:6	Reserved: These bits should be programmed as shown above.
Bit 5	**Blank to RAMDAC:** If this bit is set to a '1', the internal RAMDAC is forced to the current levels corresponding to BLANK. This must be done if an external RAMDAC is used. If this bit is reset to a '0', the internal RAMDAC operates normally.
Bits 4:3	Reserved: These bits should be programmed as shown above.
Bit 2	Reserved This bit should be programmed as shown above.
Bit 1	**Extended 16-Color (Packed-Pixel) Modes:** This bit should be set to a '1' for any 16-color Packed-pixel Mode.
Bit 0	Reserved: This bit should be programmed as shown above.

7.3.51 Graphics and Attribute Test Register: ERC9

I/O Port Address: 3CF

Index: C9

Bit	Description	Access	Reset State	Programmed
7(MSB)	Reserved	R/W	0	0
6	Reserved	R/W	0	0
5	Reserved	R/W	0	0
4	Three-State P, VDCLK	R/W	0	
3	9-Dot Font Enable	R/W	0	
2	Reserved	R/W	0	0
1	Reserved	R/W	0	0
0(LSB)	Reserved	R/W	0	0

Bit	Description
Bits 7:5	Reserved: These bits must be programmed as shown above.
Bit 4	**Three-State P, VDCLK:** If this bit is set to a '1', then P[7:0], FPVDCLK, and VDCLK are forced into high impedance. If this bit is reset to a '0', then P[7:0], FPVDCLK, and VDCLK operate normally.
Bit 3	**9-Dot Font Enable:** If this bit is set to a '1', the ninth bit of the font is fetched from Bit Plane 3, Bit 7 — M3D[7] — rather than being a replication of the eighth bit.
Bits 2:0	Reserved: These bits should be programmed as shown above.

7.3.52 Flat Panel Column Offset Register: ERD0

I/O Port Address: 3CF

Index: D0

Bit	Description	Access	Reset State
7(MSB)	Flat Panel Column Offset Bit [7]	R/W	0
6	Flat Panel Column Offset Bit [6]	R/W	0
5	Flat Panel Column Offset Bit [5]	R/W	0
4	Flat Panel Column Offset Bit [4]	R/W	0
3	Flat Panel Column Offset Bit [3]	R/W	0
2	Flat Panel Column Offset Bit [2]	R/W	0
1	Flat Panel Column Offset Bit [1]	R/W	0
0(LSB)	Flat Panel Column Offset Bit [0]	R/W	0

This register serves as a panning offset function on the flat panel display. The normal displayed image will be affected according to the values programmed into this register. These are the eight least-significant bits of a 9-bit value. The most significant bit is in Bit 0 of ERD4h. The value is used to indicate when the data begins to be displayed on the flat panel and is represented in nibbles.

Bit	Description
Bits 7:0	**Flat Panel Column Offset:** These are the eight least-significant bits of a 9-bit value. The most-significant bit is in Bit 0 of ERE4h. The value is used to indicate when the data begins to be displayed on the flat panel. If the value = 0Ah : The normal display image will be displayed at the left-most column of flat panel. If the value > 0Ah : The normal display image will be displaced to the left by the difference between the values and 0Ah. If the value < 0Ah : The normal display image will be displaced to the right by the difference between the values and 0Ah.

7.3.53 Flat Panel Horizontal Size Register: ERD1

I/O Port Address: 3CF

Index: D1

Bit	Description	Access	Reset State
7(MSB)	Flat Panel Horizontal Size Bit [7]	R/W	0
6	Flat Panel Horizontal Size Bit [6]	R/W	0
5	Flat Panel Horizontal Size Bit [5]	R/W	0
4	Flat Panel Horizontal Size Bit [4]	R/W	0
3	Flat Panel Horizontal Size Bit [3]	R/W	0
2	Flat Panel Horizontal Size Bit [2]	R/W	0
1	Flat Panel Horizontal Size Bit [1]	R/W	0
0(LSB)	Flat Panel Horizontal Size Bit [0]	R/W	0

This register contains the eight least-significant bits of a 9-bit value for the number of horizontal displayable nibbles on the panel. The most-significant bit (Bit-8), is located in Bit 1 of the LCD Overflow Register (ERD4).

Bit	Description
Bits 7:0	**Flat Panel Horizontal Size:** The value determines the horizontal width of the panel in nibble units. For 640-column panels, this register should be programmed to 640/4 - 1 = 159 decimal (9Fh).

7.3.54 Flat Panel Row Offset Register: ERD2

I/O Port Address: 3CF

Index: D2

Bit	Description	Access	Reset State
7(MSB)	Flat Panel Row Offset Bit [7]	R/W	0
6	Flat Panel Row Offset Bit [6]	R/W	0
5	Flat Panel Row Offset Bit [5]	R/W	0
4	Flat Panel Row Offset Bit [4]	R/W	0
3	Flat Panel Row Offset Bit [3]	R/W	0
2	Flat Panel Row Offset Bit [2]	R/W	0
1	Flat Panel Row Offset Bit [1]	R/W	0
0(LSB)	Flat Panel Row Offset Bit [0]	R/W	0

This register provides vertical centering for the display image. This register is active only if auto-center is disabled.

Bit	Description
Bits 7:0	**Flat Panel Row Offset:** These bits are eight least-significant bits of a 10-bit value. The most-significant bits are located at ERD4[3:2]. The 10-bit value determines the row location of the display image, calculated from the top of the flat panel.

7.3.55 Flat Panel Vertical Size Register: ERD3

I/O Port Address: 3CF

Index: D3

Bit	Description	Access	Reset State
7(MSB)	Flat Panel Vertical Size Bit [7]	R/W	0
6	Flat Panel Vertical Size Bit [6]	R/W	0
5	Flat Panel Vertical Size Bit [5]	R/W	0
4	Flat Panel Vertical Size Bit [4]	R/W	0
3	Flat Panel Vertical Size Bit [3]	R/W	0
2	Flat Panel Vertical Size Bit [2]	R/W	0
1	Flat Panel Vertical Size Bit [1]	R/W	0
0(LSB)	Flat Panel Vertical Size Bit [0]	R/W	0

This register provides the number of vertical lines for the display image.

Bit	Description
Bits 7:0	**Flat Panel Vertical Size:** These bits are eight least-significant bits of a 10-bit value. The most-significant bits are located at ERD4[6:4]. If using a single-scan panel, the 10-bit value determines the number of rows minus 1; or if using a dual-scan panel, the 10-bit value determines the number of half-panel rows divided by 2, minus 1.

7.3.56 Flat Panel Overflow Register: ERD4

I/O Port Address: 3CF

Index: D4

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Flat Panel Vertical Size Overflow Bit [10]	R/W	0
5	Flat Panel Vertical Size Overflow Bit [9]	R/W	0
4	Flat Panel Vertical Size Overflow Bit [8]	R/W	0
3	Flat Panel Row Offset Overflow Bit [9]	R/W	0
2	Flat Panel Row Offset Overflow Bit [8]	R/W	0
1	Flat Panel Horizontal Size Overflow Bit [8]	R/W	0
0(LSB)	Flat Panel Column Offset Overflow Bit [8]	R/W	0

This register provides overflow bits for other registers.

Bit	Description
Bit 7	Reserved
Bits 6:4	**Flat Panel Vertical Size Overflow:** Bits 10:8. Refer to ERD3.
Bits 3:2	**Flat Panel Row Offset Overflow:** Bits 9:8. Refer to ERD2.
Bit 1	**Flat Panel Horizontal Size Overflow:** Bit 8. Refer to ERD1.
Bit 0	**Flat Panel Column Offset Overflow:** Bit 8. Refer to ERD0.

7.3.57 Flat Panel Attribute Control Register: ERD5

I/O Port Address: 3CF

Index: D5

Bit	Description	Access	Reset State
7(MSB)	Enable AutoMap	R/W	0
6	Enable Reverse Video in Text Mode	R/W	0
5	Enable Reverse Video in Graphics Mode	R/W	0
4	Extra Line Clock Enable	R/W	0
3	Attribute Emulation Enable	R/W	0
2	Standby Mode Status	R	0
1	9-Dot Text Compression Control Bit 1	R/W	0
0(LSB)	9-Dot Text Compression Control Bit 0	R/W	0

Bit	Description
Bit 7	**Enable AutoMap:** When this bit is set to a '1', the internal grayscale palette is enabled. This palette stores sum-to-gray data mapped from the RAMDAC, allowing 256-color graphics to be automatically mapped to 64 grayscales. When this bit is set to a '0', the internal LCD palette is bypassed.
Bit 6	**Enable Reverse Video in Text Mode:** Setting this bit to a '1' enables reverse video in Text Mode for flat panels only.
Bit 5	**Enable Reverse Video in Graphics Mode:** Setting this bit to a '1' enables reverse video in Graphics Mode for flat panels only.
Bit 4	**Extra Line Clock Enable (FPLCLK):** If this bit is set to a '1', an extra line-clock pulse is generated on the lower half of dual-scan flat panels. This feature is provided for those flat panels that have the first row-driver of the lower panel disconnected. If this bit is set to a '0', no extra line-clock pulse is generated.
Bit 3	**Attribute Emulation Enable:** If this bit is set to a '1', attribute emulation is enabled (a function used only in text modes), which optimizes the contrast of the displayed text by taking background and foreground colors into consideration. If this bit is set to a '0', then colors are freely mapped into shades of gray under control of the attribute controller palette registers and the LCD palette RAM.
Bit 2	**Standby Mode Status:** This is a read-only bit, indicating that the CL-GD6410 is in Standby Mode.

7.3.57 Attribute Flat Panel Control Register: ERD5 *(cont.)*

Bit	Description
Bits 1:0	**9-Dot Text Compression Control:** These bits control the compression methods used to allow a 720-pixel display image to fit into a 640-pixel display. In SimulSCAN, these bits allow for the simultaneous display of 9-dot text on the CRT and 8-dot text on an LCD. These bits are defined as follows:

Table 7–14. 9-Dot Text Compression Control

ERD5[1]	ERD5[0]	Meaning
0	X	Display 640 pixels out of 720-pixel image to be panned with the Column Offset Register (ERD0h). Only a partial image will be displayed.
1	0	Skip every ninth pixel. The whole 720-pixel image will be compressed into a 640-pixel display.
1	1	Logical-OR the eighth pixel and the ninth pixel and place the result back into the eighth pixel.

7.3.58 Flat Panel Gray Scale Offset Register: ERD6

I/O Port Address: 3CF

Index: D6

Bit	Description	Access	Reset State
7(MSB)	Enable Vertical Stippling	R/W	0
6	Enable Horizontal Stippling	R/W	0
5 (-A)	Reserved (Rev. A)		0
5 (-B)	Enable Intermodulation (Rev. B)	R/W	0
4 (-A)	Reserved (Rev. A)		0
4 (-B)	Enable 8-bit Plasma Interface (Rev. B)	R/W	0
3	Reserved		0
2	Power Sequencing Time Control	R/W	0
1	Power Sequencing Control	R/W	0
0(LSB)	Grayscale Offset value	R/W	0

Bit	Description
Bit 7	**Enable Vertical Stippling:** When this bit is set to a '1', vertical stippling is enabled, increasing the effective number of shades of gray applied to the flat panel.
Bit 6	**Enable Horizontal Stippling:** When this bit is set to a '1', horizontal stippling is enabled, increasing the effective number of shades of gray applied to the flat panel.
Bit 5 (-A)	Reserved. (Rev. A only)
Bit 5 (-B)	**Enable Intermodulation for 512-Color Flat Panels:** This bit is used in the CL-GD6410 Revision B only. When this bit is set to '1', intermodulation is applied to 512-color TFT flat panels, providing a color pallette of approximately 185,000 colors.
Bit 4 (-A)	Reserved. (Rev. A only)
Bit 4 (-B)	**Enable 8-bit Interface for Plasma Flat Panels:** This bit is used in the CL-GD6410 Revision B only. This bit is used for plasma flat panels that require an 8-bit interface instead of a 4-bit interface. The default is '0' for a 4-bit data interface. When this bit is set to '1', the data interface for a plasma flat panel is defined to be 8-bits-wide.
Bit 3	Reserved
Bit 2	**Power Sequencing Time Control:** This bit, which is a flat-panel-dependant parameter, controls the length of the time interval between two power sequencing steps. If this bit is set to a '1', 128-136 milliseconds is selected. If this bit is set to a '0', 32-40 milliseconds is selected.

7.3.58 Flat Panel Gray Scale Offset Register: ERD6 *(cont.)*

Bit	Description
Bit 1	**Power Sequencing Control:** This bit can be used by the BIOS or a utility program to control when the flat-panel power-sequencing on or off sequence starts. It is typically set by the BIOS after POST or at any time there is a power UP/DOWN sequence. Setting this bit allows the power-sequencing state machine to proceed; otherwise, the flat panel will not be powered on. This bit will initiate the power-sequencing timer if 'power-good' input (PWG) is a '1'.
Bit 0	**Grayscale Offset Value:** This bit is normally set to a '0', selecting a value of 13. Optionally, this bit could be programmed to a '1', selecting a value of 4, to reduce flicker on some flat panels.

7.3.59 Retrace Line Clock Control Register: ERD7

I/O Port Address: 3CF

Index: D7

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Retrace Line Clocks [4]	R/W	0
3	Retrace Line Clocks [3]	R/W	0
2	Retrace Line Clocks [2]	R/W	0
1	Retrace Line Clocks [1]	R/W	0
0(LSB)	Retrace Line Clocks [0]	R/W	0

Bit	Description
Bits 7:5	Reserved
Bits 4:0	**Retrace Line Clocks:** These bits define a number (from 1 to 32) of extra Line Clocks (LLCLKs) that are required during vertical retrace (actually between flat-panel frames). These extra Line Clocks are generated at an accelerated rate compared to normal Line Clocks and use a different pulse width.

7.3.60 Flat Panel Frame Color Register: ERD8

I/O Port Address: 3CF

Index: D8

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6 (-A)	Reserved (Rev. A)		0
6 (-B)	Enable EPSON FPLCLK (Rev. B)	R/W	0
5	Reserved		0
4	Enable Frame Color	R/W	0
3	Frame Color Bit [3]	R/W	0
2	Frame Color Bit [2]	R/W	0
1	Frame Color Bit [1]	R/W	0
0(LSB)	Frame Color Bit [0]	R/W	0

Bit	Description
Bit 7	Reserved
Bit 6 (-A)	Reserved (Rev. A only)
Bit 6 (-B)	**Extra Line Clock Enable (FPLCLK):** This bit is used in the CL-GD6410 Revision B only. This bit is used for flat panels that require two extra line clock pulses to be generated on the lower half of the dual-scan panel. ERD5[4] provides the first of the two extra FPLCLKs. This bit (Bit 6) provides the second FPLCLK. If this bit is set to a '1', an extra line-clock pulse is generated on the lower half of dual-scan flat panels. This feature is provided for those flat panels that have the first row-driver of the lower panel disconnected. If this bit is set to a '0', no extra line-clock pulse is generated.
Bit 5	Reserved
Bit 4	**Enable Frame Color:** Setting this bit to a '1' enables setting the frame color.
Bits 3:0	**Frame Color bits:** This register provides control of the color for the non-displayed portion of the flat panel. This register will track the reverse video in text and graphics modes.

7.3.61 Flat Panel AC Modulation Register: ERD9

I/O Port Address: 3CF

Index: D9

Bit	Description	Access	Reset State
7(MSB)	AC Modulation [7]	R/W	0
6	AC Modulation [6]	R/W	0
5	AC Modulation [5]	R/W	0
4	AC Modulation [4]	R/W	0
3	AC Modulation [3]	R/W	0
2	AC Modulation [2]	R/W	0
1	AC Modulation [1]	R/W	0
0(LSB)	AC Modulation [0]	R/W	0

This register specifies the value applied for AC Modulation.

Bit	Description
Bits 7:0	**Flat Panel AC Modulation:** These eight bits determine the half period of the square wave applied to the MOD output pin, measured in line clocks. Normally this value is one that does not divide evenly into the panel size.

7.3.62 Flat Panel Display Control Register: ERDA

I/O Port Address: 3CF

Index: DA

Bit	Description	Access	Reset State
7(MSB)	RGB Weight Control [2]	R/W	0
6	RGB Weight Control [1]	R/W	0
5	RGB Weight Control [0]	R/W	0
4	Flat Panel Size Select [1]	R/W	0
3	Flat Panel Size Select [0]	R/W	0
2	Vertical Alignment Control [1]	R/W	0
1	Vertical Alignment Control [0]	R/W	0
0(LSB) (-A)	Reserved (Rev. A)		0
0(LSB) (-B)	Force 32 Grayshades (Rev. B)	R/W	0

This register provides miscellaneous control functions.

Bit **Description**

Bits 7:5 **RGB Weight Control:** Programming these three bits provides for the following control over the RGB color weighting (the shaded area is the default):

Table 7–15. RGB Weight Control

Bit 7	Bit 6	Bit 5	R	G	B
0	0	0	11%	30%	59%
0	0	1	30%	11%	59%
0	1	0	11%	59%	30%
0	1	1	30%	59%	11%
1	0	0	59%	11%	30%
1	0	1	59%	30%	11%
110 through 111			Reserved		

7.3.62 Display Control Register: ERDA *(cont.)*

Bit	Description
Bits 4:3	**Flat Panel Size Select:** These bits select the default panel size.

Table 7–16. Flat Panel Size Select

Bit 4	Bit 3	Meaning
0	0	640 x 480
0	1	640 x 400
10 through 11		Reserved

Bits 2:1 **Vertical Alignment Control:** These two bit control vertical alignment according to the following table:

Table 7–17. Vertical Alignment Control

Bit 2	Bit 1	Meaning
0	0	Top Alignment
0	1	Bottom Alignment
1	X	Center Alignment

Bit 0 (-A) Reserved (Rev. A only)

Bit 0 (-B) **Force 32 Grayshades:** This bit is used in the CL-GD6410 Revision B only. If this bit is set to '1', the number of shades of gray is limited to 32. This bit may be set to enhance contrast in 16-color text modes so that the text colors are selected from 32 possible combinations instead of the default of 64 combinations.

7.3.63 Standby Timer Control Register: ERDB

I/O Port Address: 3CF

Index: DB

Bit	Description	Access	Reset State
7(MSB)	Standby Timer Mode Selection [1]	R/W	0
6	Standby Timer Mode Selection [0]	R/W	0
5	Standby Timer Interval [5]	R/W	0
4	Standby Timer Interval [4]	R/W	0
3	Standby Timer Interval [3]	R/W	0
2	Standby Timer Interval [2]	R/W	0
1	Standby Timer Interval [1]	R/W	0
0(LSB)	Standby Timer Interval [0]	R/W	0

Bit **Description**

Bits 7:6 **Standby Timer Mode Selection:** When activated, these bits control the CL-GD6410 internal Standby Timer as follows:

Table 7–18. Standby Timer Mode Selection

Bit 7	Bit 6	Meaning
0	0	Disable Standby Timer.
0	1	The timer will run and time-outs will be reset by the Screen Save Clock Pin (SSCLK) (Pin 80).
1	0	Reset timer on Video Memory CPU requests (Read or Write).
1	1	Reserved.

Bits 5:0 **Standby Timer Interval:** This register specifies the time interval for the Standby Timer in units of one minute. The range is from 0 to 63 minutes.

7.3.64 Flat Panel Color Configuration Register: ERDC

I/O Port Address: 3CF

Index: DC

Bit	Description	Access	Reset State
7(MSB)	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Reserved		0
2	Reserved		0
1	MOD/FPHDE/P8 Pin Control	R/W	0
0(LSB)	9-Bit Color Panel Select	R/W	0

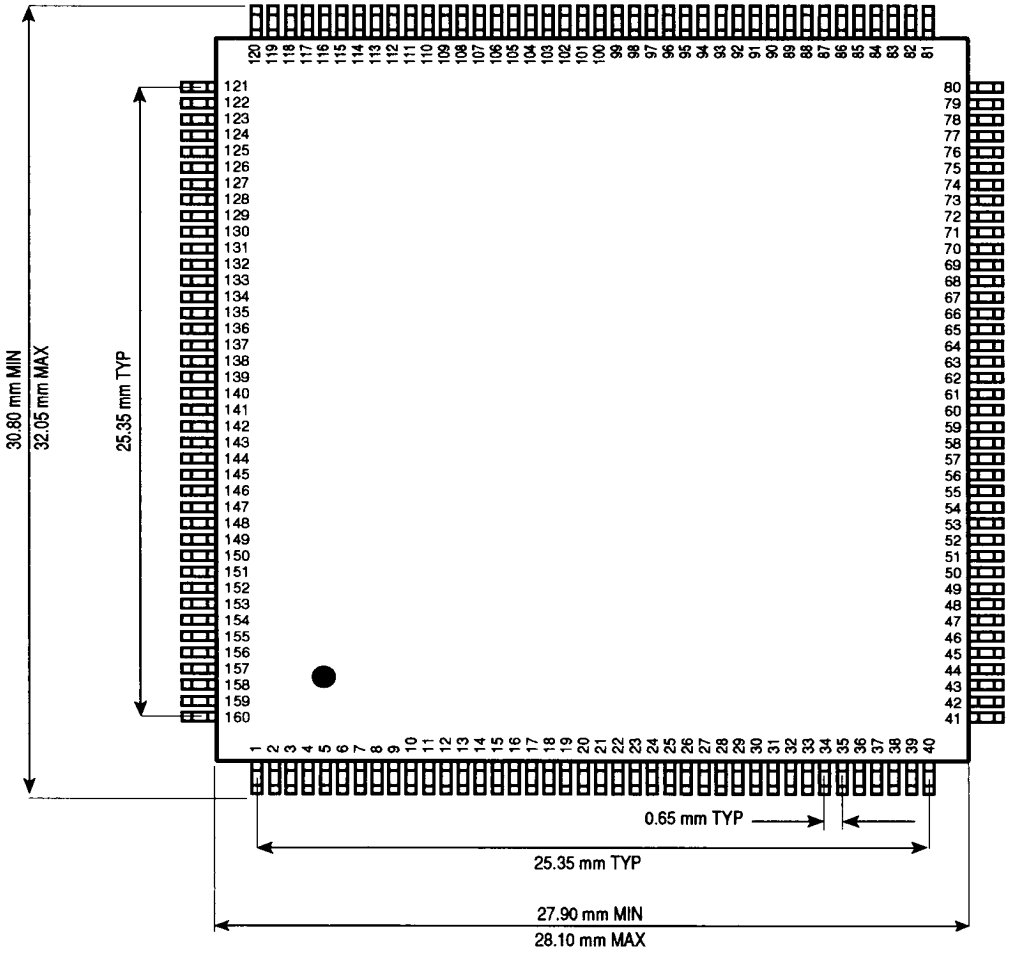
Bit	Description
Bits 7:2	Reserved
Bit 1	**MOD/FPHDE/P8 Pin Function Control:** This bit, along with Bit 0, selects the function of the MOD/FPHDE/P8 Pin (Pin 100).
Bit 0	**9-Bit Color Panel Select:** When a color TFT 9-bit flat panel is used, this bit must be set to a '1'. This bit overrides Bit 1.

Table 7–19. MOD/FPHDE/P8 Select

Bit 1	Bit 0	Meaning
0	0	MOD
0	1	FPHDE
1	X	9-Bit Color Flat Panel

8. SAMPLE PACKAGE

8.1 160-Pin Quad Flat Pack (QFP, EIAJ)



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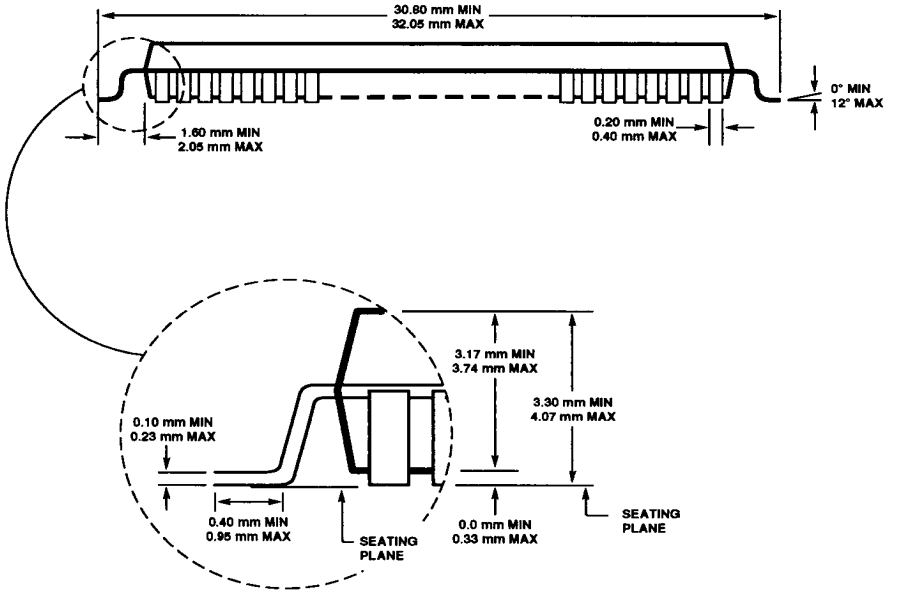
8.2 160-Pin Quad Flat Pack Expanded View (QFP, EIAJ)



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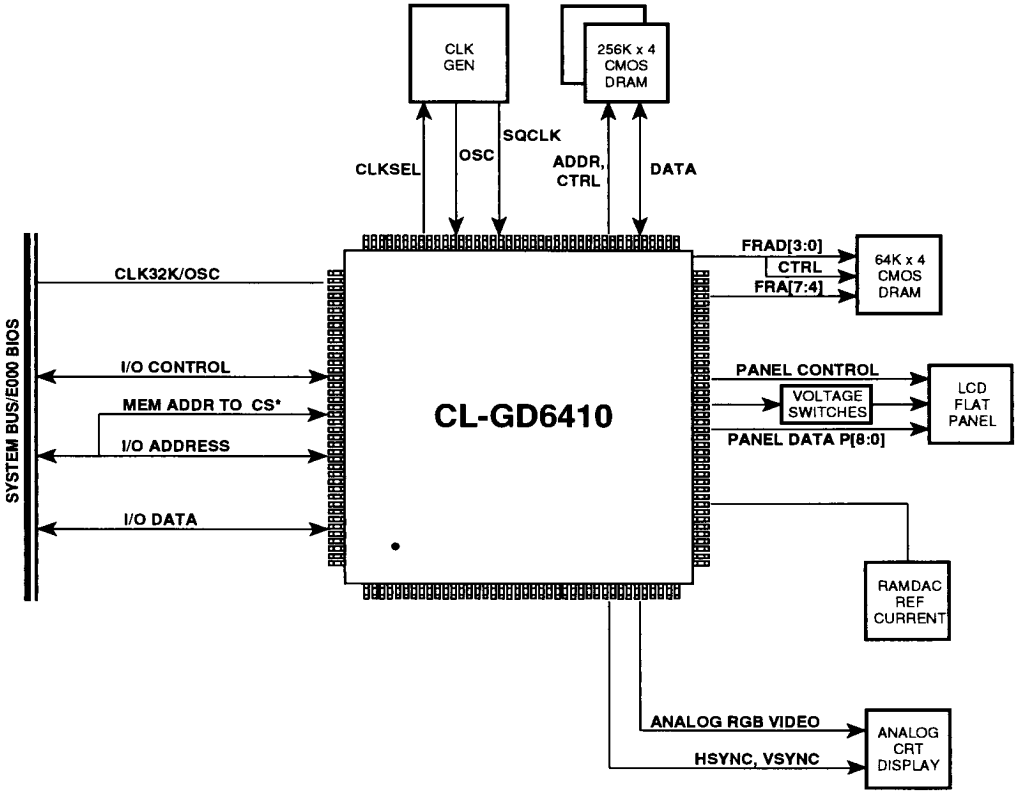
9. TYPICAL APPLICATION



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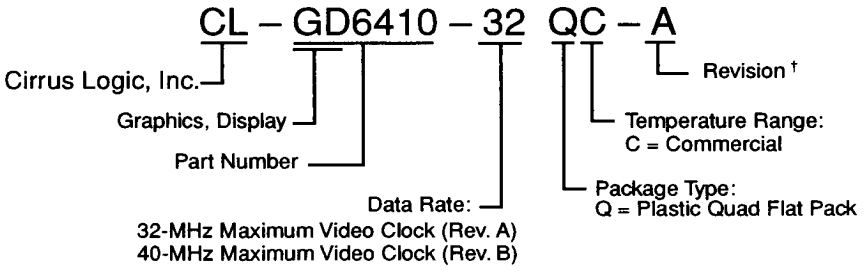
10. ORDERING INFORMATION

10.1 Cirrus Logic Numbering Guide



† Contact Cirrus Logic, Inc. for up-to-date information on revisions.

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