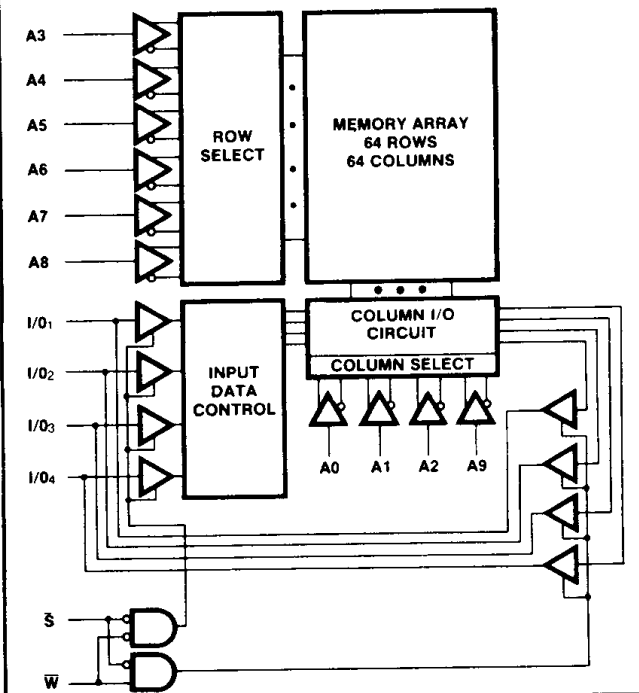# INTERSIL

M2148
4096 Bit (1024 X 4) HMOS Static RAM

FEATURES
- High speed - 70ns maximum access time (-3)
- Automatic low-power standby - 165mW maximum
- Completely static - no clock required
- Single +5V supply
- TTL compatible inputs and outputs
- Three-state outputs
- HMOS Technology
- Pin compatible with industry standard 2114M and M2148 devices
- Full Mil Temp Range - 55°C to +125°C
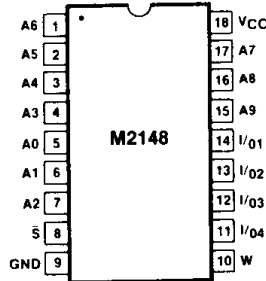- Full 883B Class B Processing Available

GENERAL DESCRIPTION

The Intersil M2148 is a high-speed 4096-bit static RAM organized 1024 words by 4 bits. It is a single-layer poly HMOS version of the industry standard 2114 and pin compatible with both the 2114M and M2148. Innovative design techniques result in minimum cell area and optimum circuit performance.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.
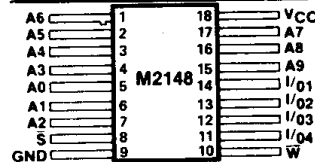
An automatic low-power standby mode is controlled by chip select $\bar{S}$; less than one cycle time after $\bar{S}$ goes high, operating current drops from a maximum of 180mA to a standby current of 30mA.

The standard device operates over the 5V ± 10% range with a worst-case access time of 85ns; a "-3" device offers a worst-case access time 70ns. Each is available in 18 pin ceramic dips and 18 pin flatpaks.
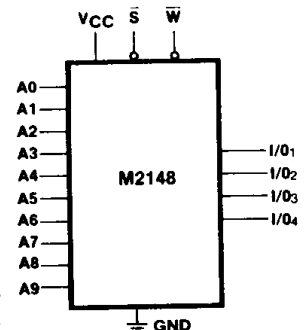
BLOCK DIAGRAM

PIN CONFIGURATION

(outline drawings JN, FN)

LOGIC SYMBOL

PIN NAMES

PIN NAMES	
$A_0 - A_9$	Address Inputs
$I/O_1 - I/O_4$	Data Input/Output
$\bar{S}$	Chip Select
$\bar{W}$	Write Enable

TRUTH TABLE

$\bar{S}$	$\bar{W}$	MODE	I/O	POWER
H	X	Not Selected	High-Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

ORDERING INFORMATION

PART NO.	ACCESS TIME	ACTIVE CURRENT	STANDBY CURRENT	PACKAGE	TEMP. RANGE
MD2148-3	70ns	180mA	30mA	18-pin CERDIP	-55°C to +125°C
MD2148	85ns	180mA	30mA	18-pin CERDIP	-55°C to +125°C
MF2148-3	70ns	180mA	30mA	18-pin FLATPACK	-55°C to +125°C
MF2148	85ns	180mA	30mA	18-pin FLATPACK	-55°C to +125°C

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ABSOLUTE MAXIMUM RATINGS

Voltage on any Pin Relative to GND[1] .... −1.5 to +7V
D.C. Output Current 20mA
Storage Temperature .... −65 to +150°C
Ambient Temperature Under Bias .... −65 to +135°C
Power Dissipation 1.2W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES:
1. This device contains internal circuitry to protect against damage due to static charge. Conventional precautions should be observed, however, during storage, handling, and use to avoid exposure to excessive voltages.

ELECTRICAL PARAMETERS V_{CC} = 5V ± 10%, T_A = −55°C to +125°C, unless otherwise noted

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
V_{IH}	Input HIGH Voltage	2.0	6.0	V	
V_{IL}	Input LOW Voltage	−1.0	0.8	V	
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −1.0mA
V_{OL}	Output LOW Voltage		0.45	V	I_{OL} = 5.0mA
I_{ILK}	Input Leakage Current		10	μA	V_{CC} = 5.5V, GND ≤ V_{IN} ≤ V_{CC}
I_{OLK}	Output Leakage Current		50	μA	$\overline{S}$ = V_{IH}, V_{CC} = 5.5V, GND ≤ V_O ≤ 4.5V
I_{OS}	Output Short Circuit Current	−200	200	mA	V_{OUT} = GND to V_{CC}

SYMBOL	DESCRIPTION	MAXIMUM VALUES M2148, M2148-3	UNITS	NOTES
I_{CCOP1}	Operating Supply Current	160	mA	1, 2
I_{CCOP2}	Operating Supply Current	180	mA	1, 3
I_{CCSB}	Standby Supply Current	30	mA	4
I_{CCPON}	Peak Power-On Supply Current	70	mA	5

NOTES:
1. V_{CC} = 5.5V, $\overline{S}$ = V_{IL}, I_O = 0mA
2. T_A = 25°C
3. T_A = −55°C
4. V_{CC} = 4.5 to 5.5V, $\overline{S}$ = V_{IH}
5. V_{CC} = GND to 4.5V, $\overline{S}$ = lower of V_{CC} or V_{IH} min. A pullup resistor on $\overline{S}$ is required during power-on in order to keep the device deselected; otherwise I_{CCPON} approaches I_{CCOP}. V_{CC} slew ≥ 1V/μs.

TIMING PARAMETERS V_{CC} = 5V ± 10%, T_A = −55°C to +125°C

Unless otherwise noted, 1, 4

| SYMBOL	DESCRIPTION	JEDEC SYMBOL	M2148 MIN	M2148 MAX	M2148-3 MIN	M2148-3 MAX	UNITS	NOTES
t_{rc}	READ CYCLE Read Cycle Time		85		70			
t_{aa}	Address Access Time	TAVQV		85		70		
t_{acs1}	Chip Select Access Time	TSLQV		85		70		2
t_{acs2}	Chip Select Access Time	TSLQV		100		80		3
t_{oh}	Output Hold from Address Change	TAXQX	5		5			
t_{lz}	Chip Selection to Output Enabled	TSLQX	10		10			5, 6
t_{hz}	Chip Deselection to Output Disabled	TSHQZ	0	25	0	25		5, 6
t_{pu}	Chip Selection to Power Up Time		0		0			
t_{pd}	Chip Deselection to Power Down Time			30		30	ns	
t_{wc}	WRITE CYCLE Write Cycle Time		85		70			
t_{cw}	Chip Selection to End of Write	TSLWH	70		65			
t_{aw}	Address Valid to End of Write	TAVWH	70		65			
t_{as}	Address Setup Time	TAVWL	0		0			
t_{wp}	Write Pulse Width	TWLWH	55		50			
t_{wr}	Write Recovery Time	TWHAX	15		5			
t_{dw}	Data Valid to End of Write	TDVWH	30		25			
t_{dh}	Data Hold Time	TWHDX	10		5			
t_{wz}	Write Enabled to Output Disabled	TWLQZ	0	25	0	25		5
t_{ow}	Output Active from End of Write	TWHQX	0		0			

NOTES:
1. t_r = t_f = 10ns. Input and output timing reference level = 1.5V. V_{IL} = 0V, V_{IH} = 3.0V.
2. Device deselected for 55ns or more prior to selection.
3. Device deselected for less than 55ns prior to selection. For deselect time of 0ns prior to select, read cycle (address) applies.
4. Operating temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
5. t_{lz} and t_{hz} are measured from 1.5V level of $\overline{S}$ to ±500mV from high impedance voltage of load circuit. t_{lz} and t_{hz} are sampled and not 100% tested.
6. At any given temperature and voltage conditions, t_{hz} max is less than t_{lz} min both for a given device and from device to device.
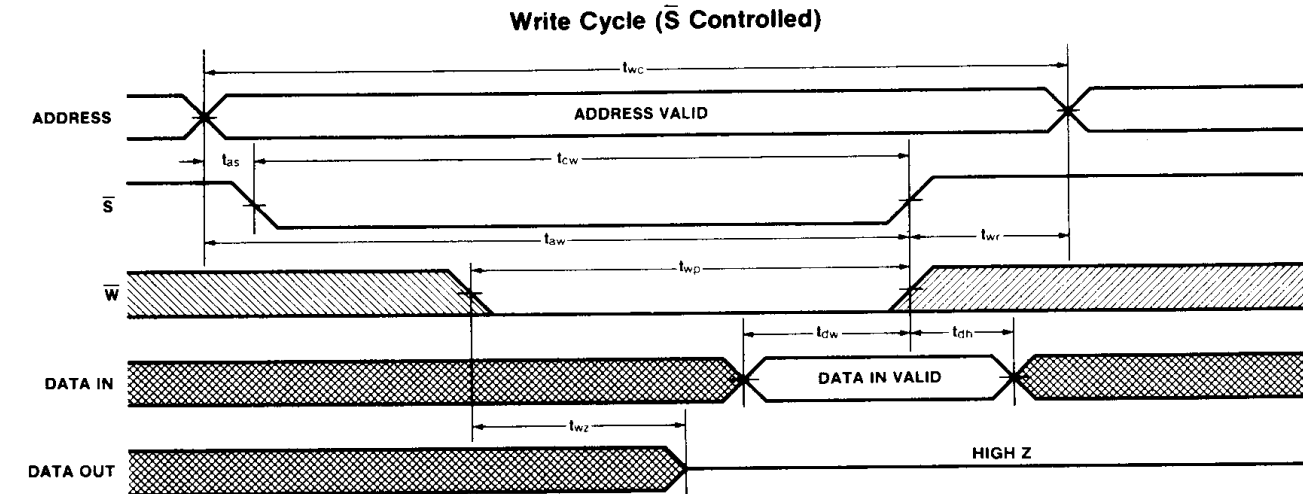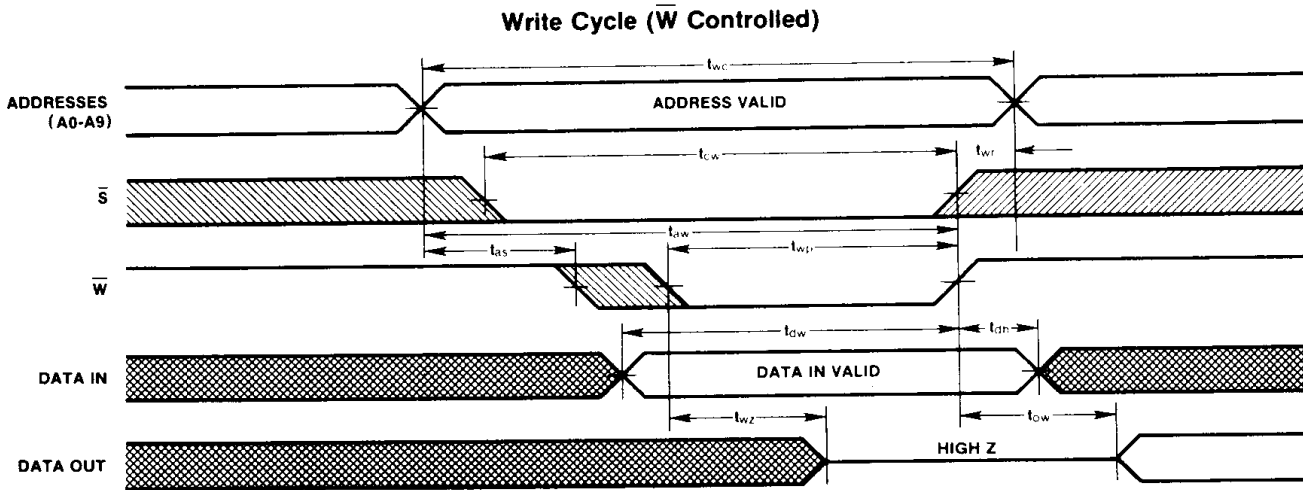
TIMING DIAGRAMS
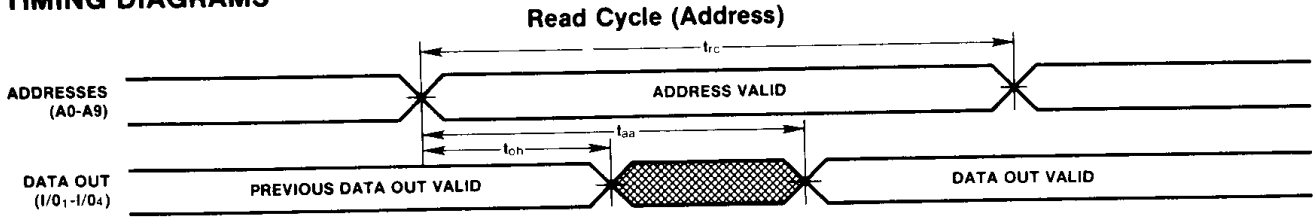
Read Cycle (Address)

Notes: 1. Device is continuously selected, $\bar{S}$ = V_{IL}.
     2. Write enable is high for read cycle, $\bar{W}$ = V_{IH}.

Read Cycle (Chip Select)
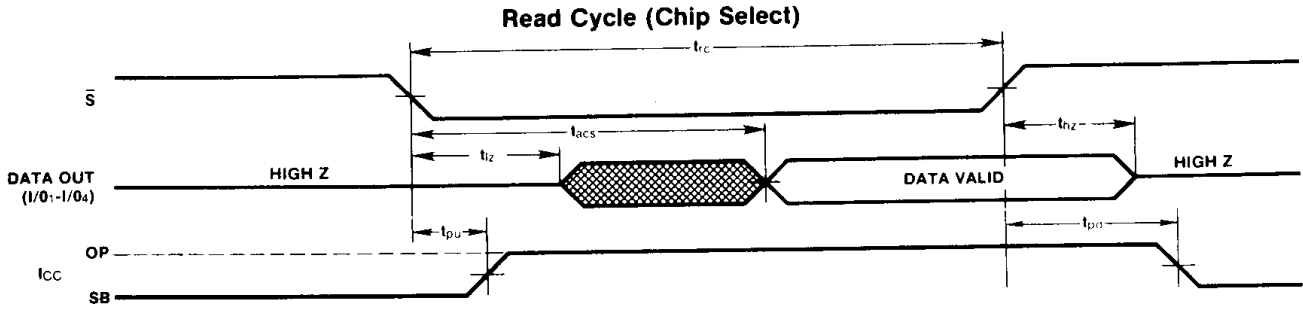
Notes:
1. Address is valid prior to or coincident with $\bar{S}$ transition low.
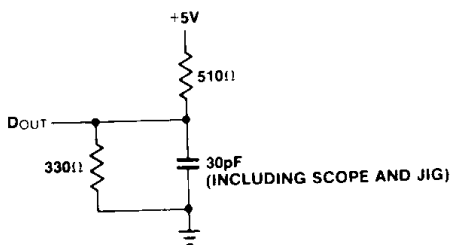2. Write enable is high for read cycle, $\bar{W}$ = V_{IH}.

Write Cycle ($\bar{W}$ Controlled)

Write Cycle ($\bar{S}$ Controlled)

Note: Outputs remain high-Z if $\bar{S}$, $\bar{W}$ go high simultaneously.

M2148

TEST LOADS

+5V

510Ω

D_OUT

330Ω

30pF
(INCLUDING SCOPE AND JIG)

AC PARAMETER LOAD CIRCUIT

+5V

510Ω

D_OUT

330Ω

5pF
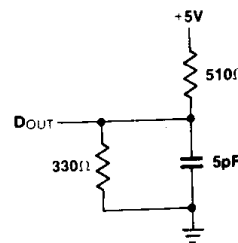
t_{lz}, t_{hz} LOAD CIRCUIT

CAPACITANCE $T_A = 25°C$, $f = 1.0mHz$

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	7	pF	$V_{OUT} = 0V$

Note: Capacitance sampled and not 100% tested.

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