Flash-ROM Module 8MByte (2Mx32Bit), 80Pin-MMC, 3.3V Design
Part No. HMF2M32F4VSA

GENERAL DESCRIPTION

The HMF2M32F4V is a high-speed flash read only memory (FROM) module containing 2,097,152 words organized in a x32bit configuration. The module consists of four 1M x 16 FROM mounted on a 80-pin stackable type, double - sided, FR4-printed circuit board.

Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.

Output enable (/OE) and write enable (/WE) can set the memory input and output. The host system can detect a program or erase operation is complete by observing the Ready Pin, or reading the DQ7(Data # Polling) and DQ6(Toggle) status bits. When FROM module is disable condition the module is becoming power standby mode, system designer can g et low-power design. All module components may be powered from a single + 3.0V DC power supply and all inputs and outputs are LVTTL-compatible.

FEATURES

- Part Identification
  - HMF2M32F4VSA : Socket 5mm
- Access time: 70, 80, 90, 120ns
- High-density 8MByte design
- High-reliability, low-power design
- Single + 3.0V ± 0.5V power supply
- All in/outputs are LVTTL-compatible
- FR4-PCB design
- 80-pin Designed by
  40-pin Fine Pitch Connector (x 2EA)
- Minimum 1,000,000 write/erase cycle
- Sector erases architecture

OPTIONS MARKING

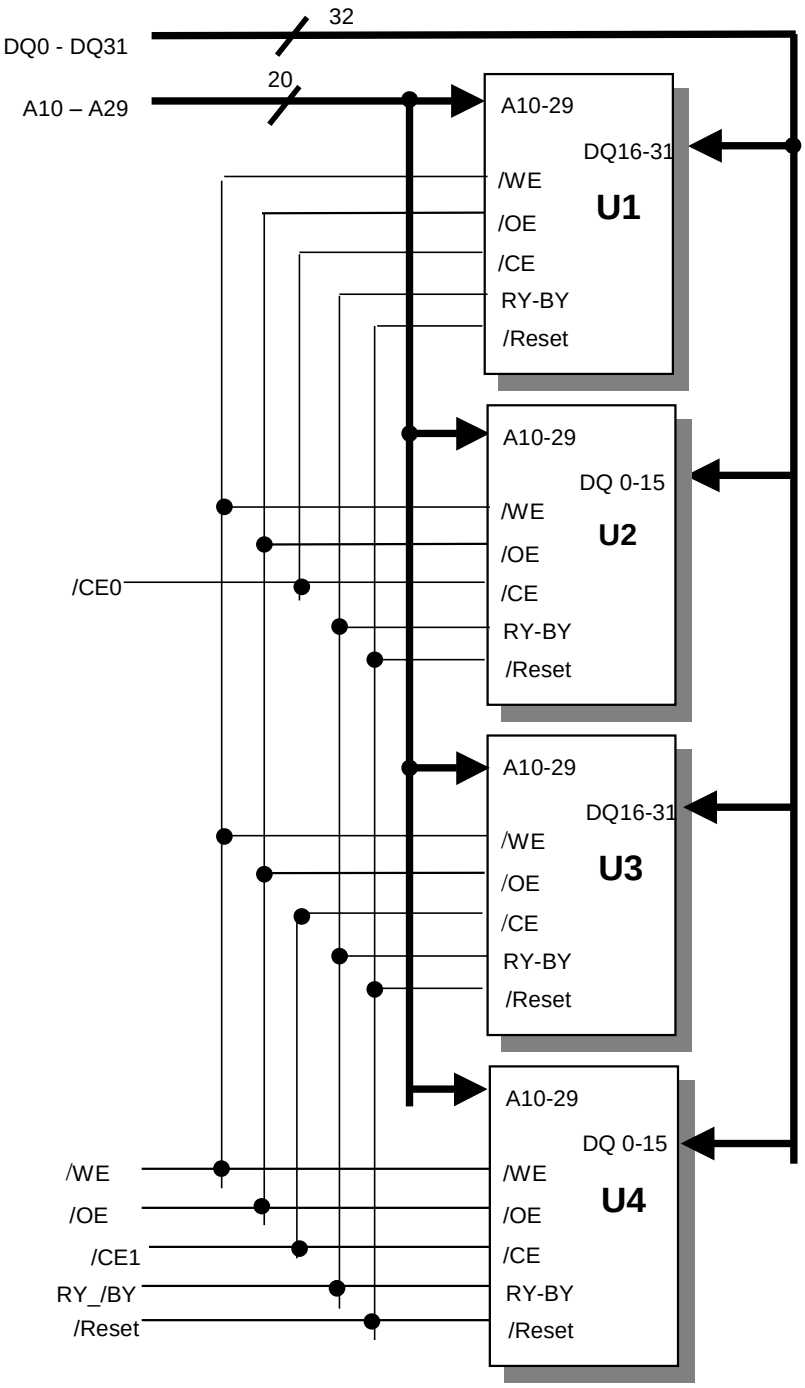
- Timing
  - 70ns access -70
  - 80ns access -80
  - 90ns access -90
  - 120ns access -120
- Packages
  - 80-pin MMC F

PIN ASSIGNMENT

P1				P2			
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	VCC	21	VCC	1	VCC	21	VCC
2	CE0*	22	DQ16	2	DQ15	22	NC
3	NC	23	DQ24	3	DQ7	23	NC
4	NC	24	DQ17	4	DQ14	24	BYTE*
5	NC	25	DQ25	5	DQ6	25	OE*
6	RY_BY*	26	DQ18	6	DQ13	26	CE1*
7	VSS	27	VSS	7	VSS	27	VSS
8	RESET*	28	DQ26	8	DQ5	28	A13
9	WE*	29	DQ19	9	DQ12	29	A29
10	A10	30	DQ27	10	DQ4	30	A11
11	A21	31	DQ20	11	DQ11	31	A12
12	A20	32	DQ28	12	DQ3	32	A22
13	A19	33	DQ21	13	DQ10	33	A23
14	VSS	34	VSS	14	VSS	34	VSS
15	A18	35	DQ29	15	DQ2	35	A24
16	A17	36	DQ22	16	DQ9	36	A25
17	A16	37	DQ30	17	DQ1	37	A26
18	A15	38	DQ23	18	DQ8	38	A27
19	A14	39	DQ31	19	DQ0	39	A28
20	VCC	40	VCC	20	VCC	40	VCC

4 cf : Address & Data Bus is organized for LG Specification.
(A10 & DQ0 are MSB, A29 & DQ31 a re LSB)

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	/RESET	DQ (/BYTE=L)	POWER
STANDBY	X	H	X	Vcc±0.3V	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	H	HIGH-Z	ACTIVE
READ	L	L	H	H	D_{OUT}	ACTIVE
WRITE or ERASE	X	L	L	H	D_{IN}	ACTIVE

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage with respect to ground all other pins	$V_{IN,OUT}$	-0.5V to Vcc+0.5V
Voltage with respect to ground Vcc	V_{CC}	-0.5V to +4.0V
Storage Temperature	T_{STG}	-65°C to +150°C
Operating Temperature	T_A	-55°C to +125°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
Vcc for ± 10% device Supply Voltages	Vcc	2.7V		3.6V
Ground	V_{SS}	0	0	0

DC AND OPERATING CHARACTERISTICS ($0^oC \leq T_A \leq 70\ ^oC$)

PARAMETER	TEST CONDITIONS		SYMBOL	MIN	MAX	UNIT
Input Load Current	Vcc=Vcc max, V_{IN}= GND to Vcc		I_{L1}		±1.0	μA
Output Leakage Current	Vcc=Vcc max, V_{OUT}= GND to Vcc		I_{L0}		±1.0	μA
Output High Voltage	I_{OH} = -2.0mA, Vcc = Vcc min		V_{OH}	2.4		V
Output Low Voltage	I_{OL} = 4.0mA, Vcc =Vcc min		V_{OL}		0.45	V
Vcc Active Read Current (1)	/CE = V_{IL},	5MHZ	I_{CC1}	18	32	mA
	/OE = V_{IH},	1MHZ		4	8	
Vcc Active Write Current (2)	/CE = V_{IL}, /OE=V_{IH}		I_{CC2}	40	60	mA
Vcc Standby Current	/CE, /RESET=Vcc±0.3V		I_{CC3}		60	mA
Low Vcc Lock-Out Voltage			V_{LKO}	2.3	2.5	V

Notes: 1. The Icc current listed is typically less than 2mA/MHz, with /OE at V_{IH}.

2. Icc active while embedded algorithm (program or erase) is in progress

3. Maximum Icc current specifications are tested with Vcc=Vcc max

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Sector Erase Time	-	0.7	15	sec	Excludes 00H programming prior to erasure
Chip Erase Time		25		sec	
Byte Programming Time	-	9	300	μs	Excludes system-level overhead
Chip Programming Time	-	18	54	sec	

TSOP CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes : Test conditions T_A = 25°C, f=1.0 MHz.

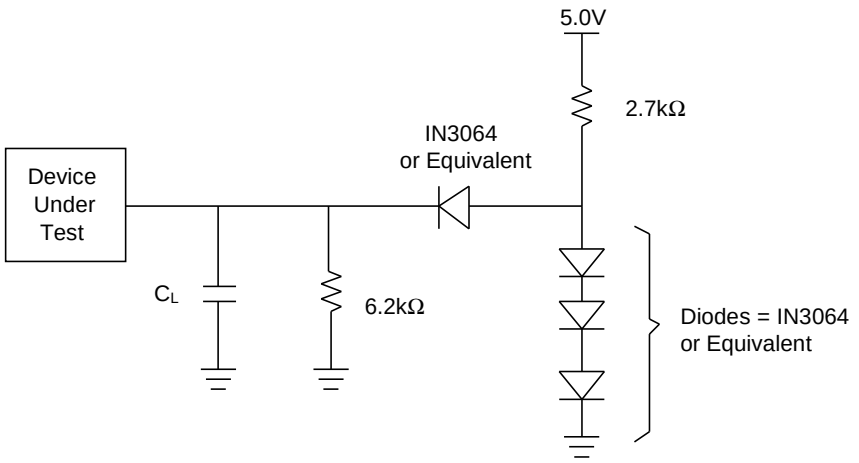
AC CHARACTERISTICS

u Read Only Operations Characteristics

PARAMETER SYMBOLS		DESCRIPTION	TEST SETUP		Speed Options				UNIT
JEDEC	STANDARD				-70R	-80	-90	-120	
t_{AVAV}	t_{RC}	Read Cycle Time		Min	70	80	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	/CE = V_{IL} /OE = V_{IL}	Max	70	80	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	/OE = V_{IL}	Max	70	80	90	120	ns
t_{GLQV}	t_{OE}	Chip Enable to Output Delay		Max	30	30	35	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z		Max	25	25	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z		Max	25	25	30	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First		Min	0				ns

TEST SPECIFICATIONS

TEST CONDITION	70R, 80	90, 120	UNIT
Output load	1TTL gate		
Output load capacitance,C_L (Including jig capacitance)	30	100	pF
Input rise and full times	5		ns
Input pulse levels	0.0-3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V



Note : C_L = 100pF including jig capacitance

u Erase/Program Operations

PARAMETER SYMBOLS		DESCRIPTION		Speed Options				UNIT
JEDEC	STANDARD			70R	80	90	120	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	80	90	12	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	35	35	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OES}	Output Enable Setup Time	Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min	0				ns
t_{ELWL}	t_{CS}	/CE Setup Time	Min	0				ns
t_{WHEH}	t_{CH}	/CE Hold Time	Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	35	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30				ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	9				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note1)	Typ	0.7				sec
	t_{VCS}	Vcc set up time	Min	50				µs

Notes : 1 . This does not include the preprogramming time

2 . This timing is only for Sector Protect operations

u Erase/Program Operations

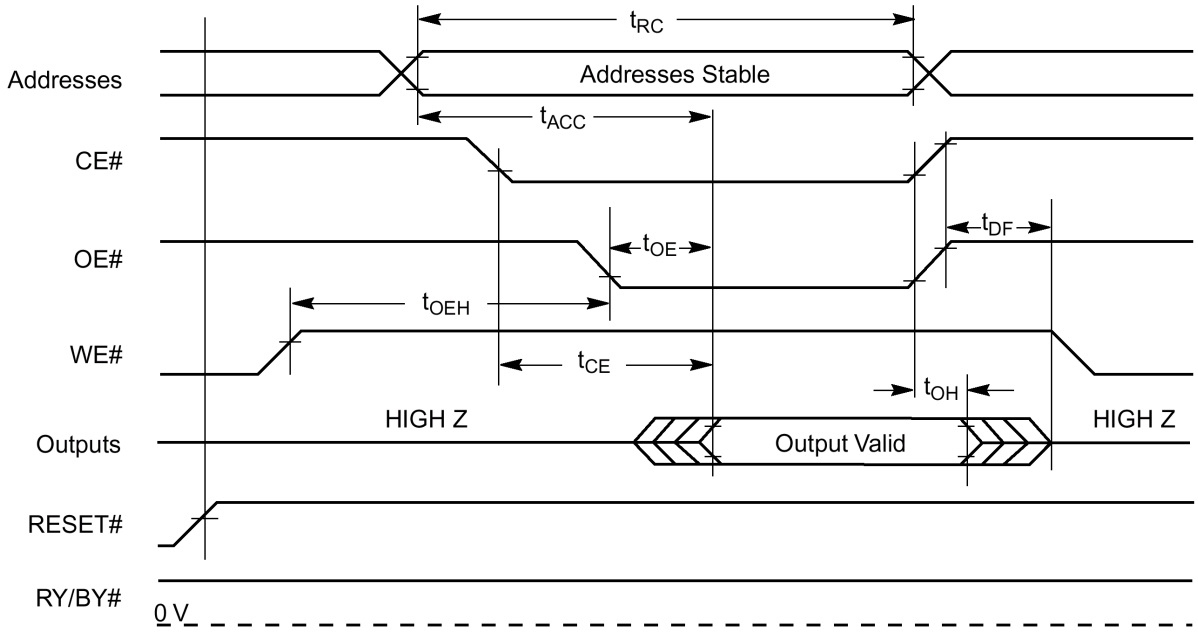
Alternate /CE Controlled Writes

PARAMETER SYMBOLS		DESCRIPTION		Speed Options				UNIT
JEDEC	STANDARD			-70R	-80	-90	120	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	80	90	12	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	35	35	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OES}	Output Enable Setup Time	Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min	0				ns
t_{ELWL}	t_{CS}	/CE Setup Time	Min	0				ns
t_{WHEH}	t_{CH}	/CE Hold Time	Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	35	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30				ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	9				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note1)	Typ	0.7				sec

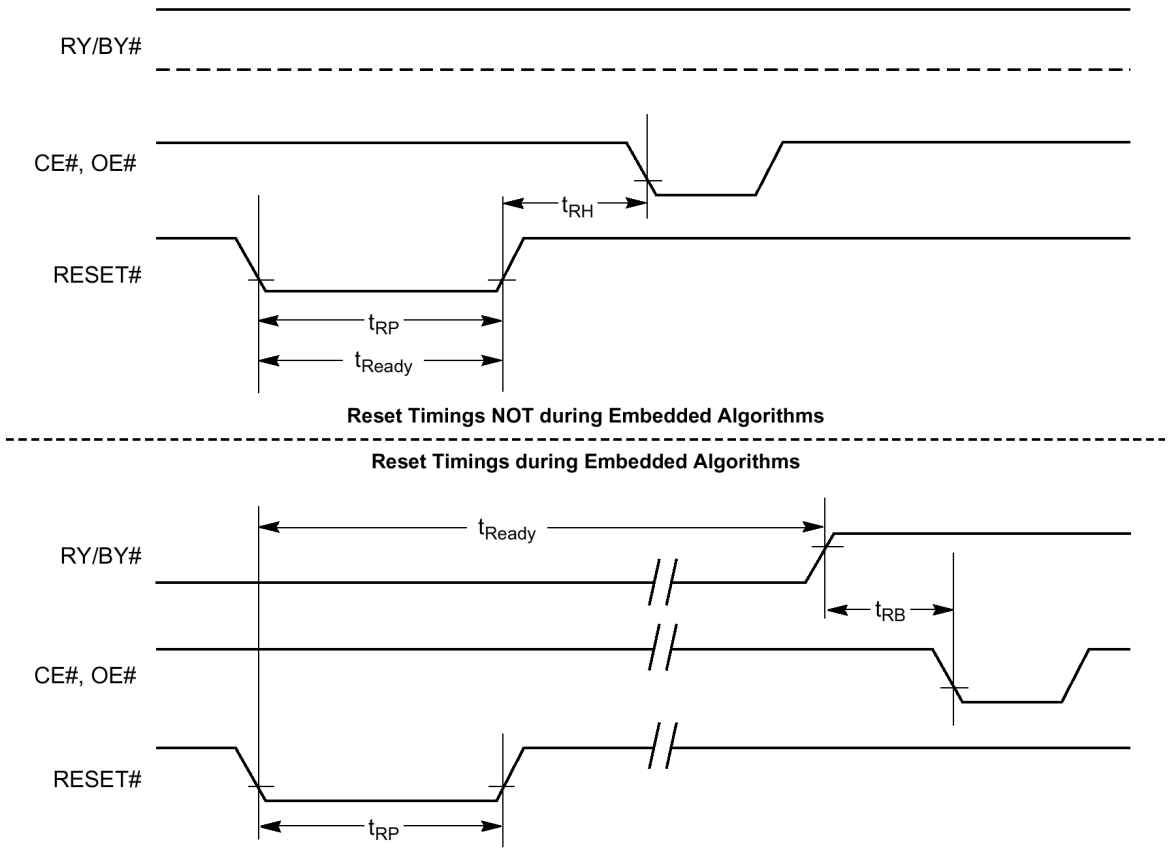
Notes : 1. This does not include the preprogramming time

2 . This timing is only for Sector Protect operations

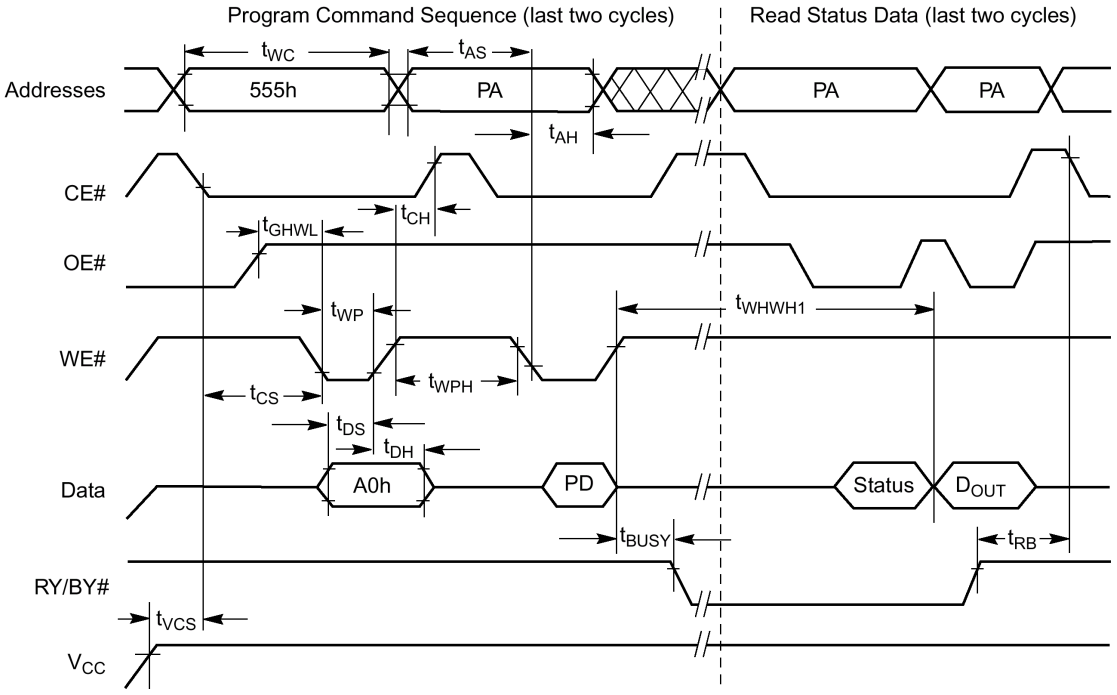
u READ OPERATIONS TIMING



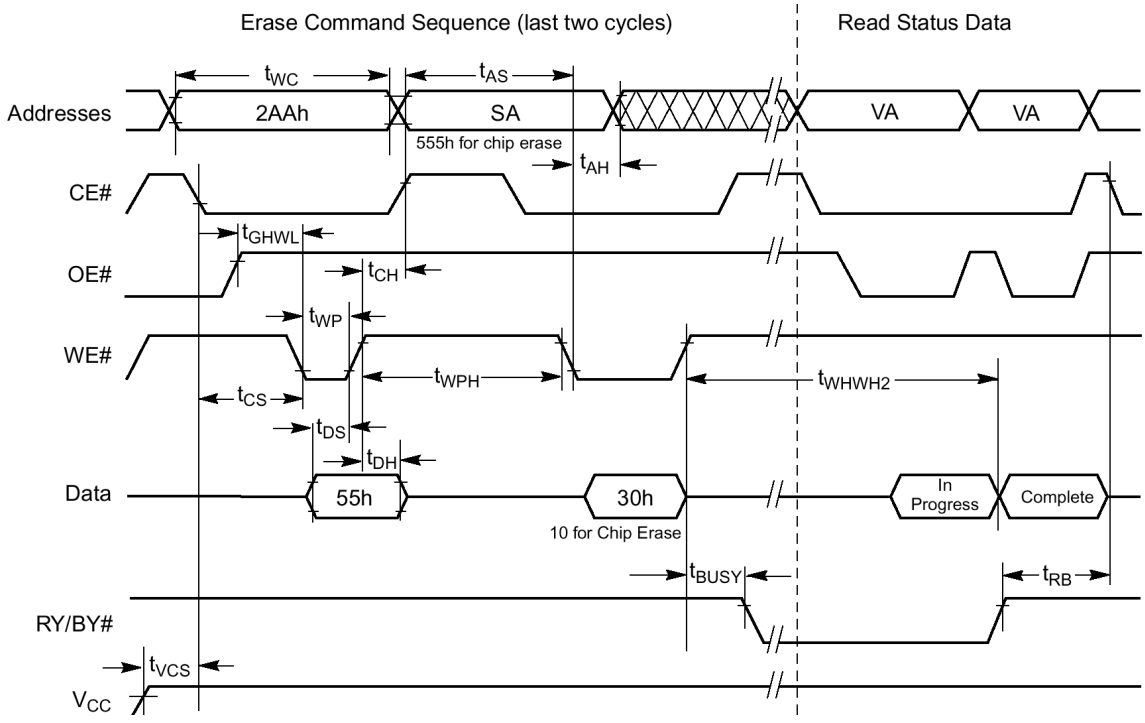
u RESET TIMING



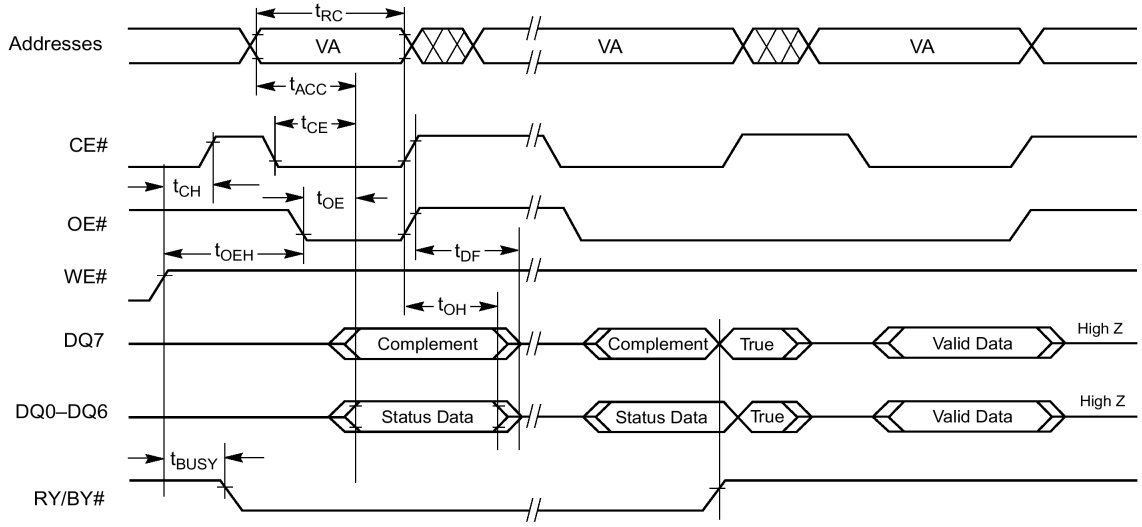
u PROGRAM OPERATIONS TIMING



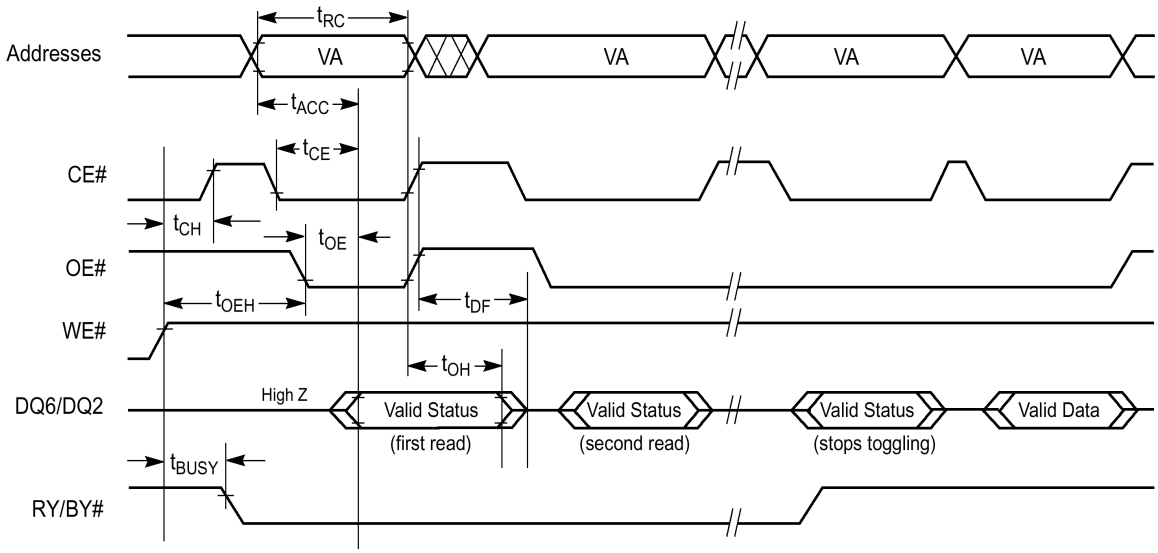
u CHIP/SECTOR ERASE OPERATION TIMINGS



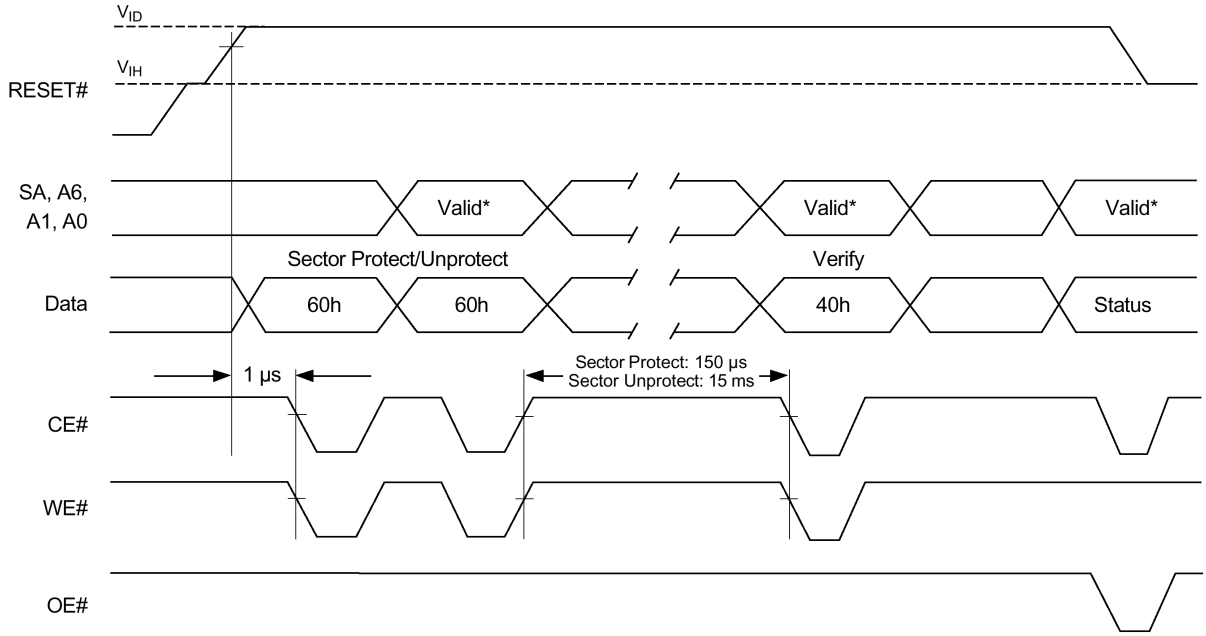
u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



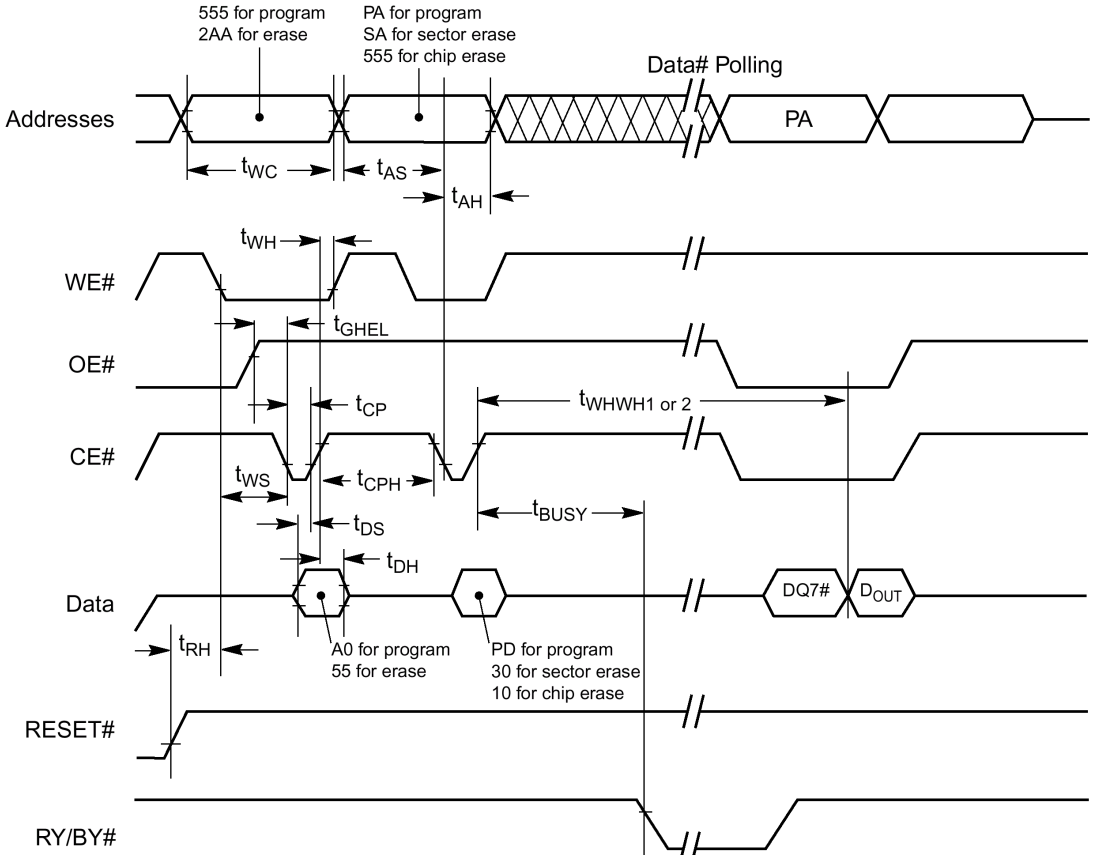
u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM

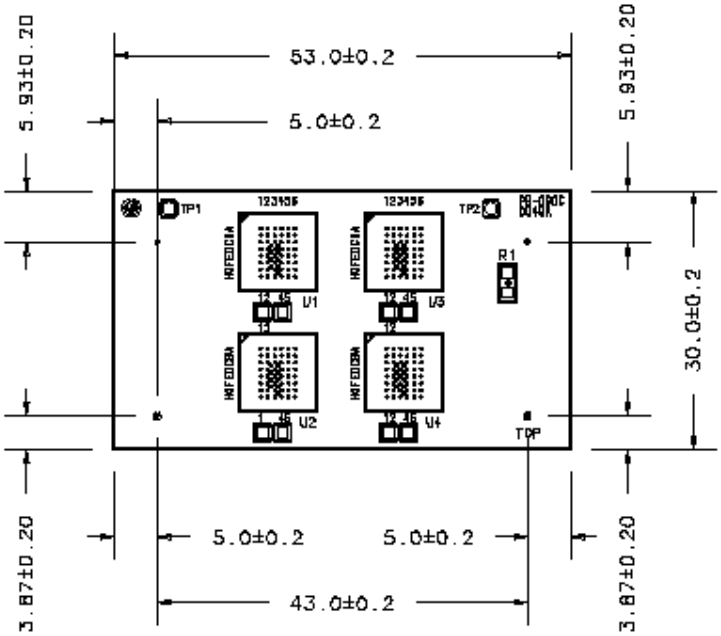


u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS

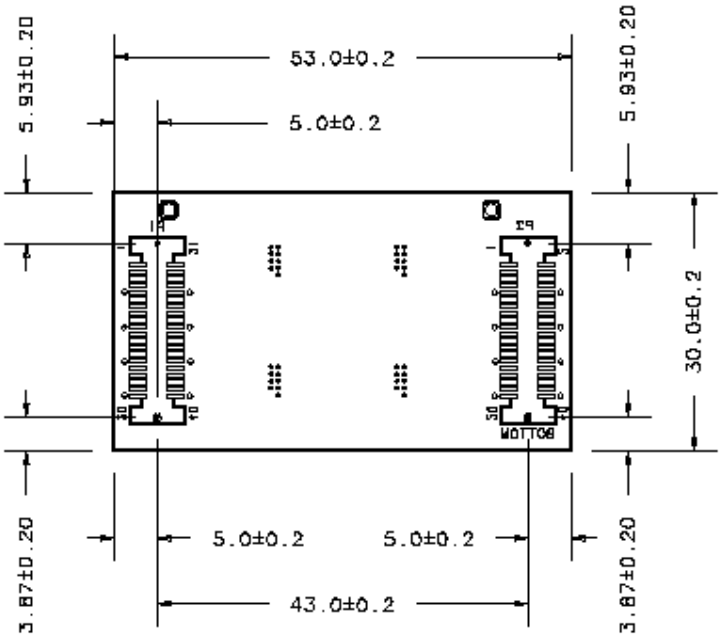


PACKAGE DIMMENSIONS

FRONT-SIDE



REAR-SIDE



ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMF2M32F2V-70	4MByte	x 32	80Pin -MMC	2EA	3.3V	70ns
HMF2M32F2V-80	4Mbyte	x 32	80Pin –MMC	2EA	3.3V	80ns
HMF2M32F2V-90	4Mbyte	x 32	80Pin –MMC	2EA	3.3V	90ns
HMF2M32F2V-120	4Mbyte	x 32	80Pin -MMC	2EA	3.3V	120ns