HT24LC08/16

8K/16K 2-Wire CMOS Serial EEPROM

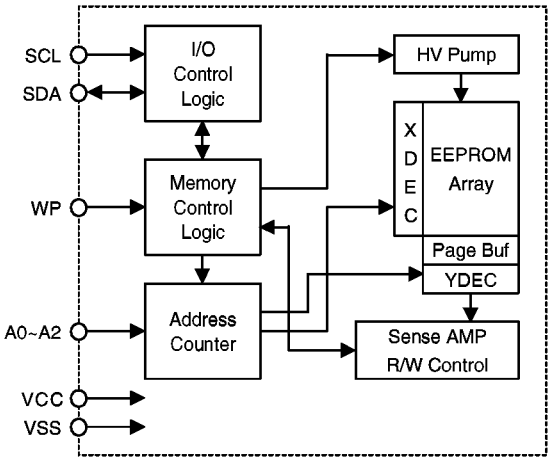
Features

- Operating voltage: 2.4V~5.5V
- Low power consumption
  - Operation: 5mA max.
  - Standby: 5μA max.
- Internal organization
  - 8K (HT24LC08): 1024×8
  - 16K (HT24LC16): 2048×8
- 2-wire Serial Interface
- Write cycle time: 5ms max.
- Automatic erase-before-write operation
- Partial page write allowed
- 16-byte Page Write Mode
- Write operation with built-in timer
- Hardware controlled write protection
- 40-year data retention
- 10^6 rewrite cycles per word
- 8-pin DIP/SOP package
- Commerical temperature range (0°C to +70°C)

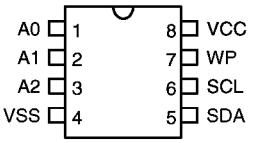
General Description

The HT24LC08/16 is an 8K/16K-bit serial read/write non-volatile memory device using the CMOS floating gate process. Its 8192/16384 bits of memory are organized into 1024/2048 words and each word is 8 bits. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. Up to two HT24LC08 devices and only one HT24LC16 device may be connected to the same two wire bus. The HT24LC08/16 is guaranteed for 1M erase/write cycles and 40-year data retention.

Block Diagram



Pin Assignment



HT24LC08/16
– 8 DIP/SOP

Pin Description

Pin Name	I/O	Description
A0~A2	I	Address input
SDA	I/O	Serial data
SCL	I	Serial clock input
WP	I	Write protect
VSS	I	Negative power supply
VCC	I	Positive power supply

Absolute Maximum Ratings

Operating Temperature (Commercial) ..... 0°C to 70°C

Storage Temperature ..... –50°C to 125°C

Applied VCC Voltage with Respect to VSS ..... –0.3V to 6.0V

Applied Voltage on any Pin with Respect to VSS ..... –0.3V to V_{CC}+0.3V

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=0°C to 70°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{CC}	Operating Voltage	—	—	2.4	—	5.5	V
I_{CC1}	Operating Current	5V	Read at 100kHz	—	—	2	mA
I_{CC2}	Operating Current	5V	Write at 100kHz	—	—	5	mA
V_{IL}	Input Low Voltage	—	—	–1	—	$0.3V_{CC}$	V
V_{IH}	Input High Voltage	—	—	$0.7V_{CC}$	—	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	2.4V	I_{OL}=2.1mA	—	—	0.4	V
I_{LI}	Input Leakage Current	5V	V_{IN}=0 or V_{CC}	—	—	1	μA
I_{LO}	Output Leakage Current	5V	V_{OUT}=0 or V_{CC}	—	—	1	μA
I_{STB1}	Standby Current	5V	V_{IN}=0 or V_{CC}	—	—	5	μA
I_{STB2}	Standby Current	2.4V	V_{IN}=0 or V_{CC}	—	—	4	μA
C_{IN}	Input Capacitance (See Note)	—	f=1MHz 25°C	—	—	6	pF
C_{OUT}	Output Capacitance (See Note)	—	f=1MHz 25°C	—	—	8	pF

Note: These parameters are periodically sampled but not 100% tested

A.C. Characteristics

Ta=0°C to 70°C

Symbol	Parameter	Remark	Standard Mode*		V_{CC}=5V±10%		Unit
			Min.	Max.	Min.	Max.	
f_{SK}	Clock Frequency		—	100	—	400	kHz
t_{HIGH}	Clock High Time		4000	—	600	—	ns
t_{LOW}	Clock Low Time		4700	—	1200	—	ns
t_R	SDA and SCL Rise Time	Note	—	1000	—	300	ns
t_F	SDA and SCL Fall Time	Note	—	300	—	300	ns
$t_{HD:STA}$	START Condition Hold Time	After this period the first clock pulse is generated	4000	—	600	—	ns
$t_{SU:STA}$	START Condition Setup Time	Only relevant for repeated START condition	4000	—	600	—	ns
$t_{HD:DAT}$	Data Input Hold Time		0	—	0	—	ns
$t_{SU:DAT}$	Data Input Setup Time		200	—	100	—	ns
$t_{SU:STO}$	STOP Condition Setup Time		4000	—	600	—	ns
t_{AA}	Output Valid from Clock		—	3500	—	900	ns
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4700	—	1200	—	ns
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	100	—	50	ns
t_{WR}	Write Cycle Time		—	5	—	5	ms

Notes: These parameters are periodically sampled but not 100% tested

* The standard mode means V_{CC}=2.4V to 5.5V

For relative timing, refer to timing diagrams

Functional Description

- Serial clock (SCL)

  The SCL input is used for positive edge clock data into each EEPROM device and negative edge clock data out of each device.

- Serial data (SDA)

  The SDA pin is bidirectional for serial data transfer. The pin is open drain driven and may be write-OR with any number of other open drain or open collector devices.

- A0, A1, A2

  The HT24LC08 only uses the A2 input for hard wire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins have no connection.

  The HT24LC16 does not use the device address pins which limits the number of devices on a single bus to one. The A0, A1 and A2 pins have no connection.

- Write protect (WP)

  The HT24LC08/16 has a write protect pin that provides hardware data protection. The write protect pin allows normal read/write operations when the connection is grounded. When the write protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

WP Pin Status	Protect Array	
	HT24LC08	HT24LC16
At V_{CC}	Full Array (8K)	Full Array (16K)
At V_{SS}	Normal Read/Write Operations	

Memory organization

- HT24LC08, 8K Serial EEPROM

  Internally organized with 1024 8-bit words, the 8K requires a 10-bit data word address for random word addressing.

- HT24LC16, 16K Serial EEPROM

  Internally organized with 2048 8-bit words, the 16K requires an 11-bit data word address for random word addressing.

Device operations

- Clock and data transition

  Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is high. Changes in data line while the clock line is high will be interpreted as a START or STOP condition.

- Start condition

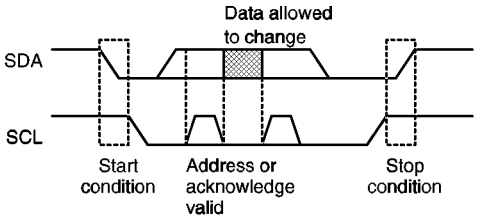
  A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition Timing diagram).

- Stop condition

  A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition Timing Diagram).

- Acknowledge

  All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.



Device addressing

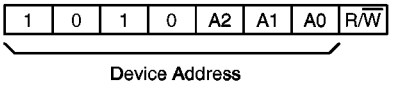
The 8K and 16K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation. The device address word consist of a mandatory one, zero sequence for the first four most significant bits (refer to the diagram showing the Device Address). This is common to all the EEPROM device.

The 8K EEPROM only use the A2 device address bit with the next two bits for memory page addressing. The A2 bit must compare its corresponding hard-wired input pin. The A1 and A0 pins have no connection.

The 16K does not use any device address bits but instead the 3 bits are used for memory page addressing. These page addressing bits on the 8K and 16K devices should be considered the most significant bits of the data word address which follows. The A0, A1 and A2 pins have no connection.

The 8th bit device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

If the comparison of the device address succeed the EEPROM will output a zero at ACK bit. If not, the chip will return to a standby state.



Write operations

- Byte write

  A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. After receiving the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and EEPROM will not respond until write is complete (refer to Byte write timing).

- Page write

  The 8K/16K EEPROM is capable of a 16-byte page write.

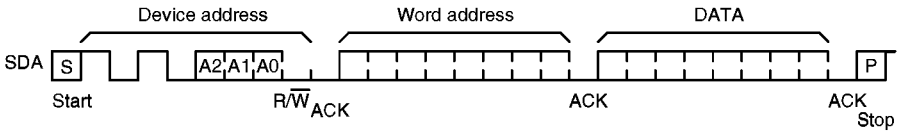
  A page write is initiated in the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges the receipt of the first data word, the microcontroller can transmit up to 15 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Page write timing).

  The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location.

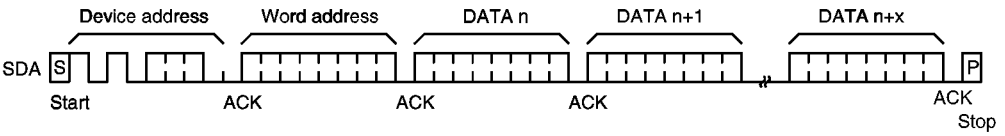
- Acknowledge polling

  Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves

Byte write timing



Page write timing



the master sending a start condition followed by the control byte for a write command (R/W=0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is completed, then the device will return the ACK and the master can then proceed with the next read or write command.

- Write protect

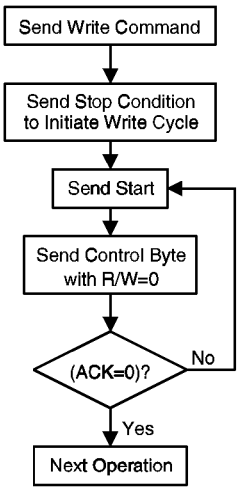
  The HT24LC08/16 can be used as a serial ROM when the WP pin is connected to VCC . Programming will be inhibited and the entire memory will be write-protected.

- Read operations

  Read operations are initiated in the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

- Current address read

  The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll over during read from the last byte of the last memory page to the first byte of the first page. The address roll over during write from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Current read timing).

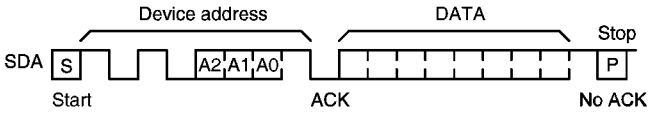


Acknowledge polling flow

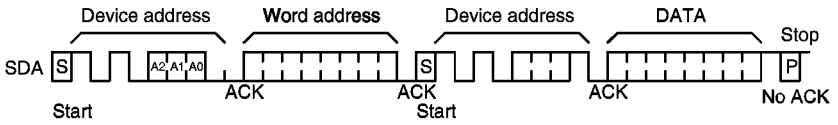
- Random read

  A random read requires a dummy byte write sequence to load in the data word address which is then clocked in and acknowledged by the EEPROM. The microcontroller must then generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Random read timing).

Current read timing



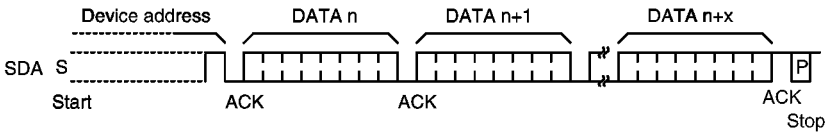
Random read timing



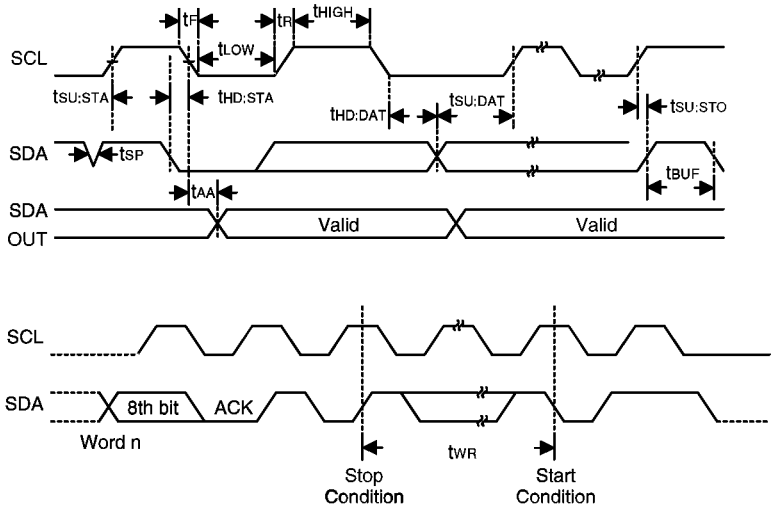
- Sequential read

  Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledgment. As long as the EEPROM receives an acknowledgment, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll over and the sequential read continues. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition.

Sequential read timing



Timing Diagrams



Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the valid start condition of sequential command.

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