

**52A, 55V, 0.019 Ohm, N-Channel UltraFET[™]
Power MOSFETs**


These N-Channel power MOSFETs are manufactured using the innovative UltraFET[™] process.

This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75332.

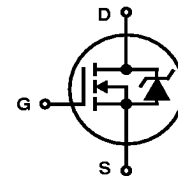
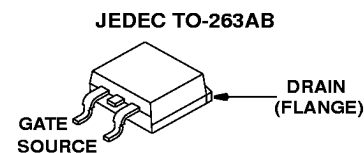
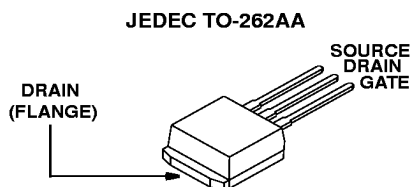
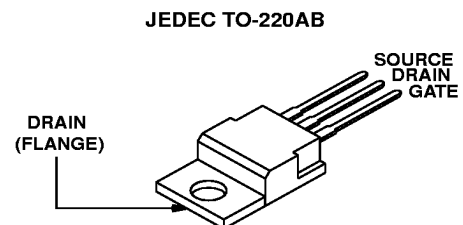
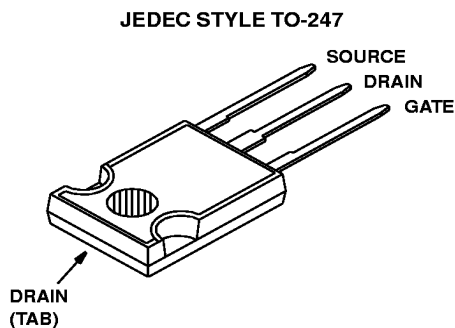
Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75332G3	TO-247	75332G3
HUF75332P3	TO-220AB	75332P3
HUF75332S3	TO-262AA	75332S3
HUF75332S3S	TO-263AB	75332S3

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF75332S3ST.

Features

- 52A, 55V
- *Ultra Low On-Resistance*, $r_{DS(ON)} = 0.019\Omega$
- Diode Exhibits Both High Speed and Soft Recovery
- *Temperature Compensating* PSpice Model
- *Thermal Impedance* SPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

Packaging


HUF75332G3, HUF75332P3, HUF75332S3, HUF75332S3S

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	55 V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	55 V
Gate to Source Voltage	V_{GS}	± 20 V
Drain Current		
Continuous (Figure 2)	I_D	52 A
Pulsed Drain Current	I_{DM}	Figure 5
Pulsed Avalanche Rating	E_{AS}	Figures 6, 14, 15
Power Dissipation	P_D	110 W
Derate Above 25°C		0.74 W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334.	T_{pkg}	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied

NOTE:

1. $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ (Figure 11)	55	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ (Figure 10)	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 50\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 45\text{V}$, $V_{GS} = 0\text{V}$, $T_C = 150^\circ\text{C}$	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 52\text{A}$, $V_{GS} = 10\text{V}$ (Figure 9)	-	0.016	0.019	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30\text{V}$, $I_D \cong 52\text{A}$, $R_L = 0.577\Omega$, $V_{GS} = 10\text{V}$, $R_{GS} = 6.8\Omega$ (Figures 16, 17)	-	-	100	ns
Turn-On Delay Time	$t_{d(ON)}$		-	12	-	ns
Rise Time	t_r		-	55	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	11	-	ns
Fall Time	t_f		-	25	-	ns
Turn-Off Time	t_{OFF}		-	-	55	ns
Total Gate Charge	$Q_g(TOT)$	$V_{GS} = 0\text{V}$ to 20V	-	70	85	nC
Gate Charge at 10V	$Q_g(10)$	$V_{GS} = 0\text{V}$ to 10V	-	40	50	nC
Threshold Gate Charge	$Q_g(TH)$	$V_{GS} = 0\text{V}$ to 2V	-	2.5	3.0	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 12)	-	1300	-	pF
Output Capacitance	C_{OSS}		-	480	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	115	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	1.36	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247	-	-	30	$^\circ\text{C/W}$
		TO-220, TO-262 and TO-263	-	-	62	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 52\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 52\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	75	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 52\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	140	nC

Typical Performance Curves

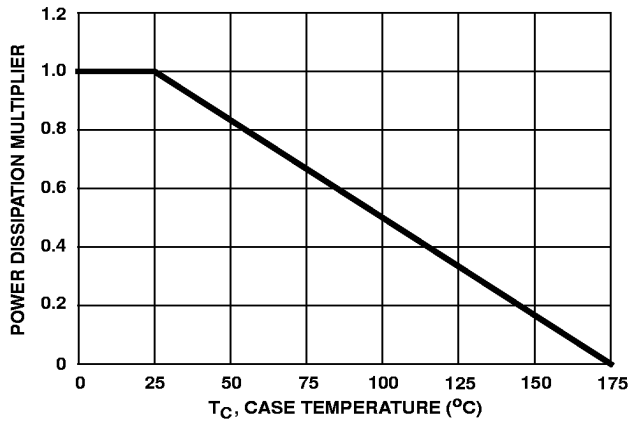


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

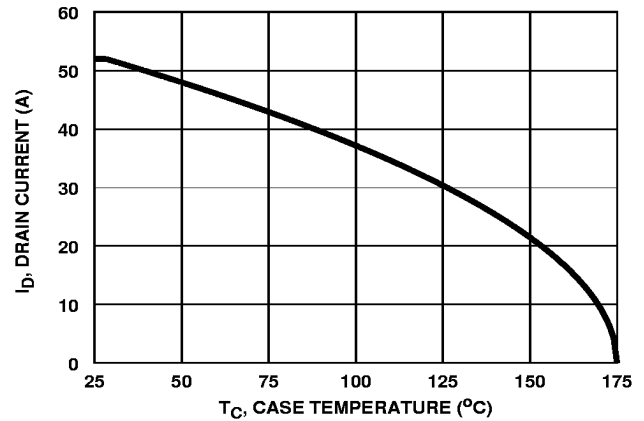


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

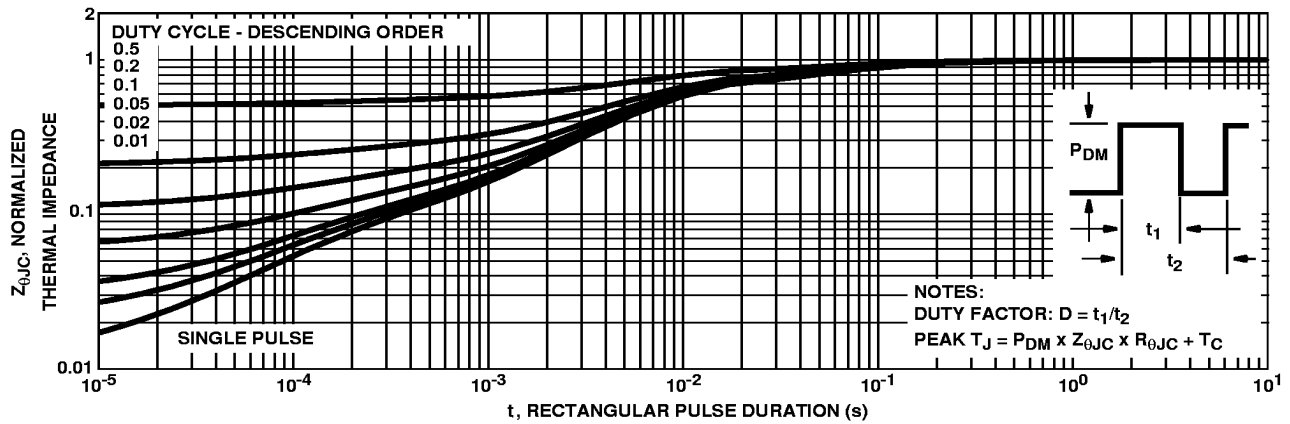


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

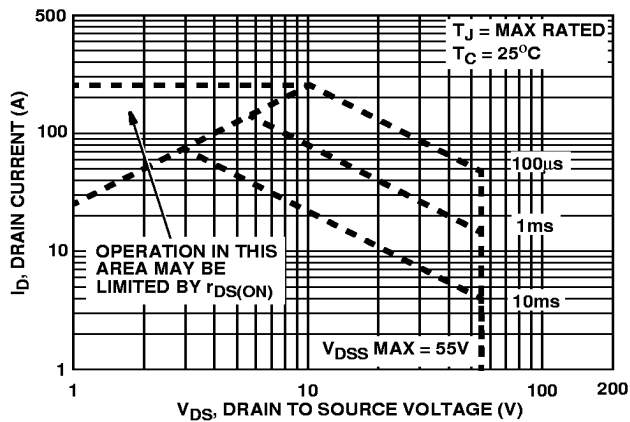


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

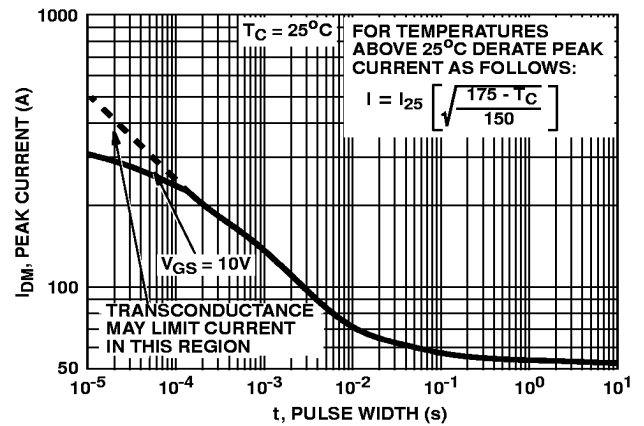
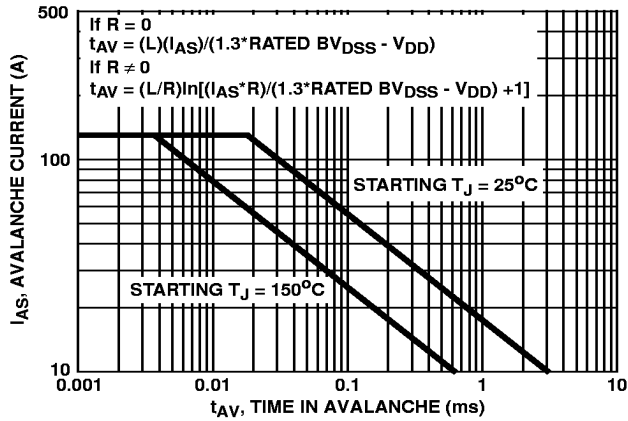


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Harris Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

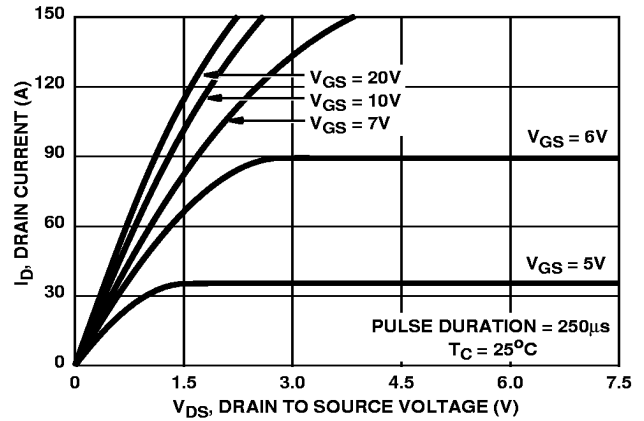


FIGURE 7. SATURATION CHARACTERISTICS

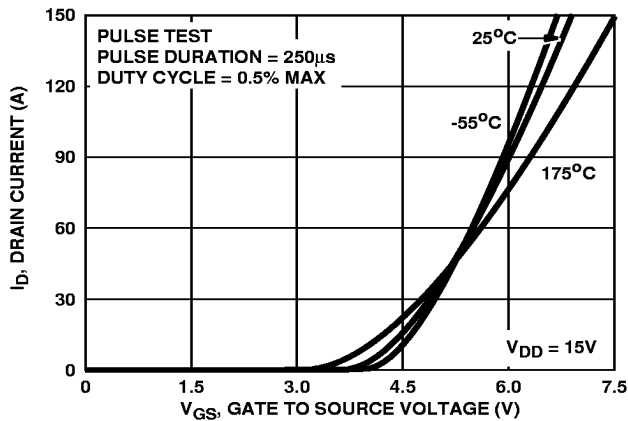


FIGURE 8. TRANSFER CHARACTERISTICS

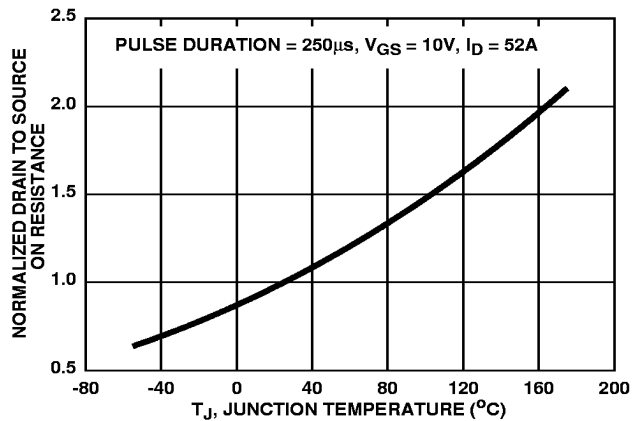


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

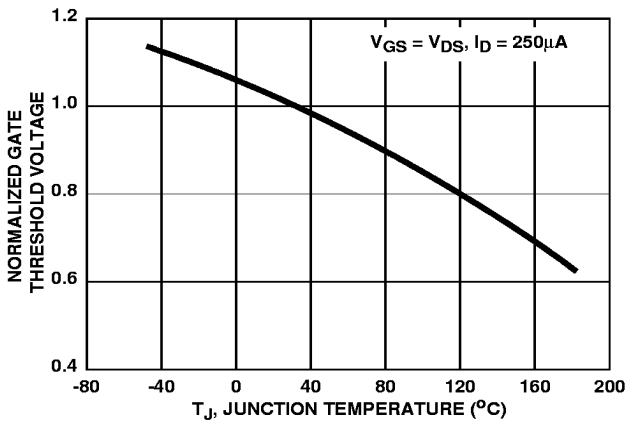


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

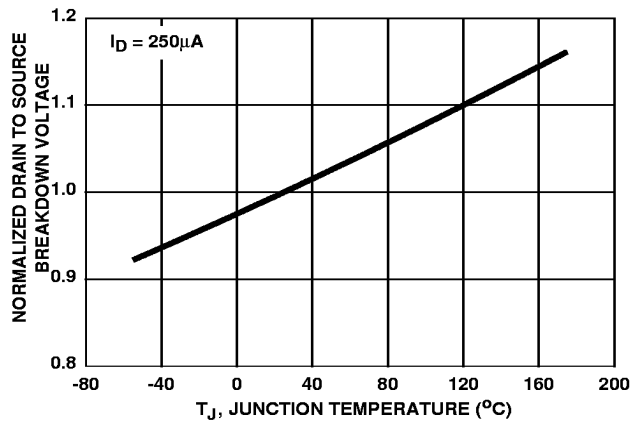


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

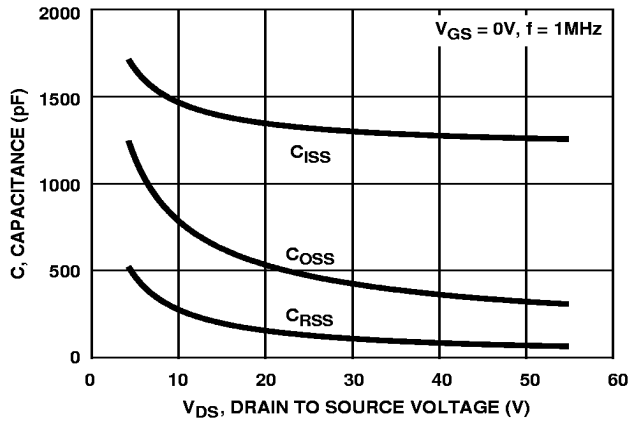
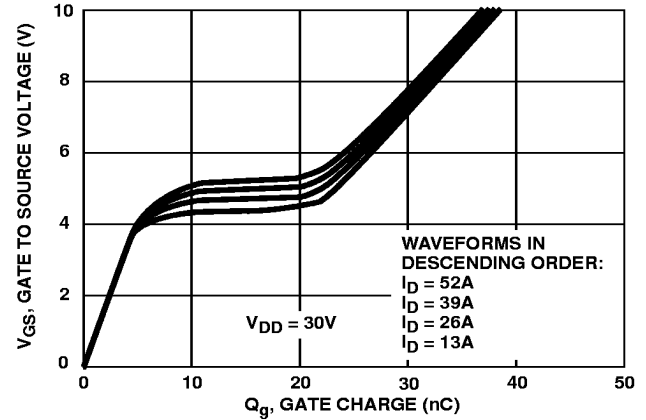


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

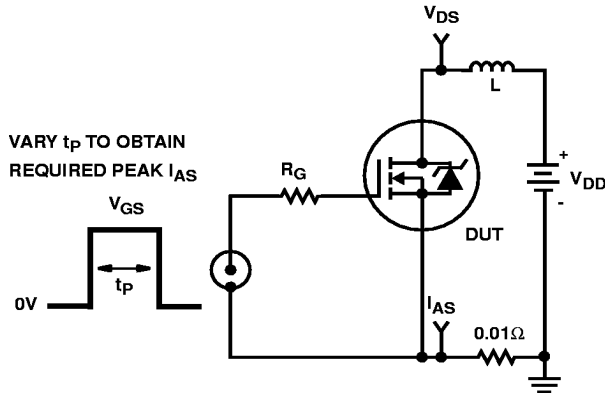


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

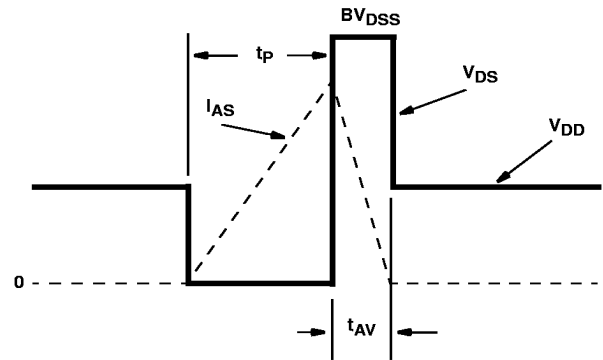


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

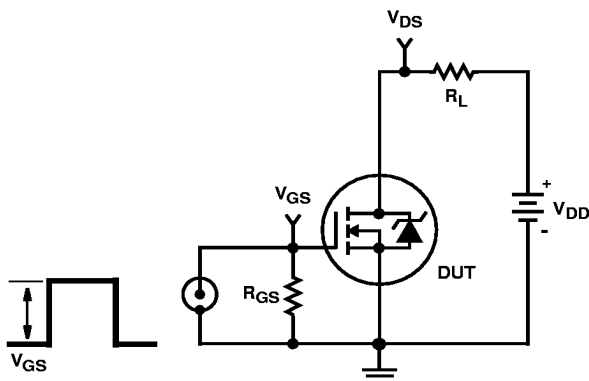


FIGURE 16. SWITCHING TIME TEST CIRCUIT

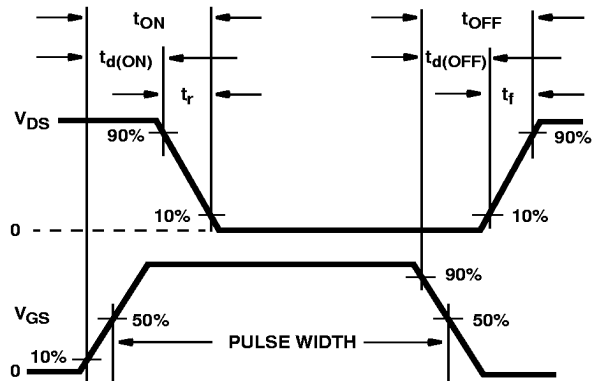


FIGURE 17. RESISTIVE SWITCHING WAVEFORM

Test Circuits and Waveforms (Continued)

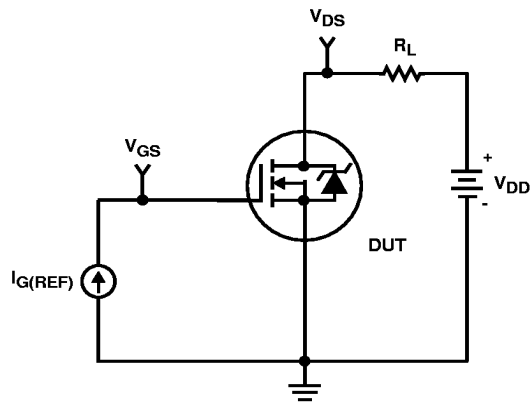


FIGURE 18. GATE CHARGE TEST CIRCUIT

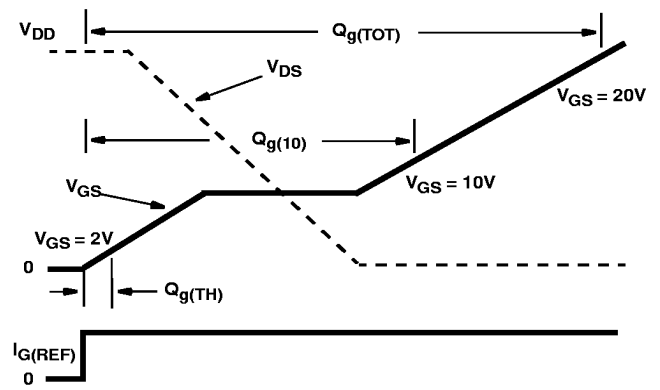


FIGURE 19. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

.SUBCKT HUF75332 2 1 3 ; rev Jan 98

CA 12 8 2.23e-9
CB 15 14 2.23e-9
CIN 6 8 1.51e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 58.3
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 3.58e-9
LSOURCE 3 7 7.7e-10

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 3.4e-3
RGATE 9 20 1.3
RLDRAIN 2 5 10
RLGATE 1 9 35.8
RLSOURCE 3 7 7.7
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 6.0e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

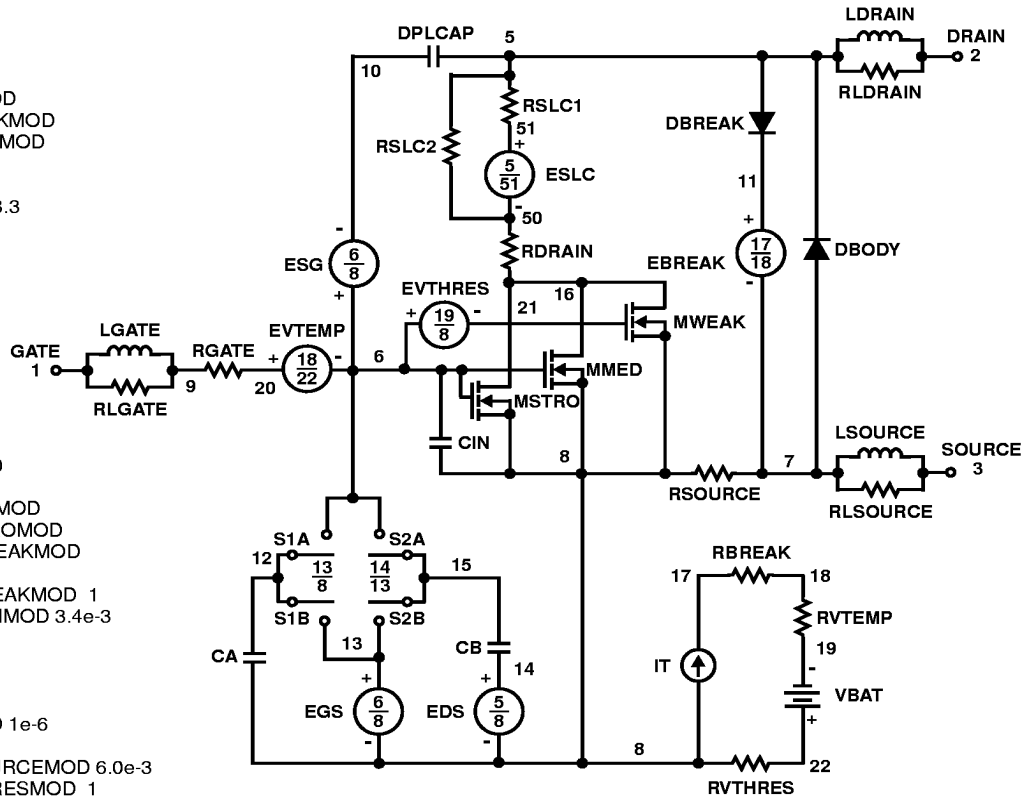
ESLC 51 50 VALUE={((V(5,51)/ABS(V(5,51)))^(PWR(V(5,51)/(1e-6*180),4.6)))}

.MODEL DBODYMOD D (IS = 1.6e-12 RS = 3e-3 IKF = 20 XTI = 5.25 TRS1 = 2.35e-3 TRS2 = 1e-7 CJO = 2.2e-9 TT = 2.6e-7 M = 0.47)
.MODEL DBREAKMOD D (RS = 1e-1 IKF = 9.5e-6 TRS1 = 1.5e-3 TRS2 = -3.1e-5)
.MODEL DPLCAPMOD D (CJO = 2.2e-9 IS = 1e-30 N = 1 M = 0.94 VJ = 1.45)
.MODEL MMEDMOD NMOS (VTO = 3.2 KP = 2 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.3)
.MODEL MSTROMOD NMOS (VTO = 3.7 KP = 58 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.7 KP = 0.008 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 13 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.1e-3 TC2 = -1.25e-6)
.MODEL RDRAINMOD RES (TC1 = 1.6e-2 TC2 = 1.1e-5)
.MODEL RSLCMOD RES (TC1 = 3.4e-3 TC2 = 1e-6)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-5)
.MODEL RVTHRESMOD RES (TC = -1.5e-3 TC2 = -2e-6)
.MODEL RVTEMPMOD RES (TC1 = -2.8e-3 TC2 = 1e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -8 VOFF = -3.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.5 VOFF = -8)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0 VOFF = 1)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1 VOFF = 0)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



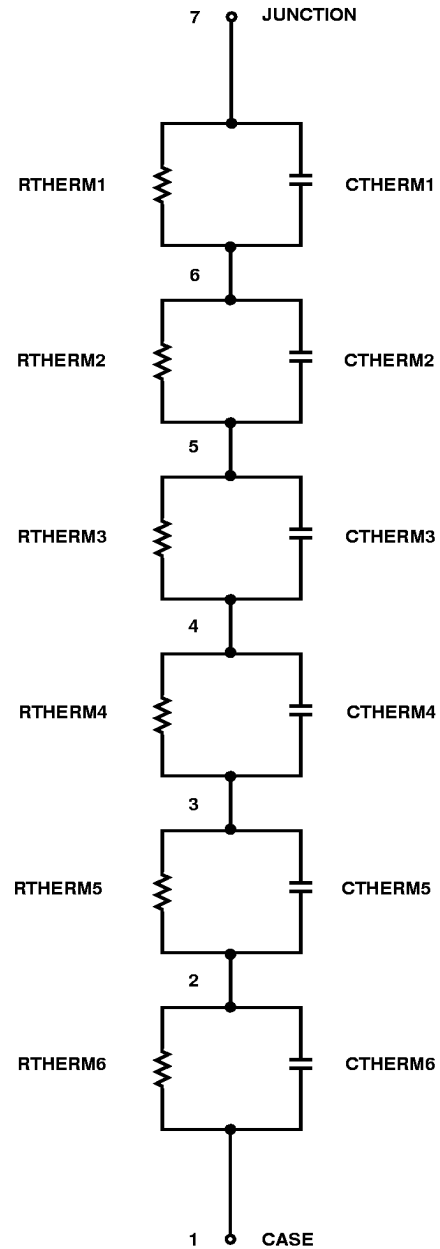
SPICE Thermal Model

rev Jan 98

HUF75332

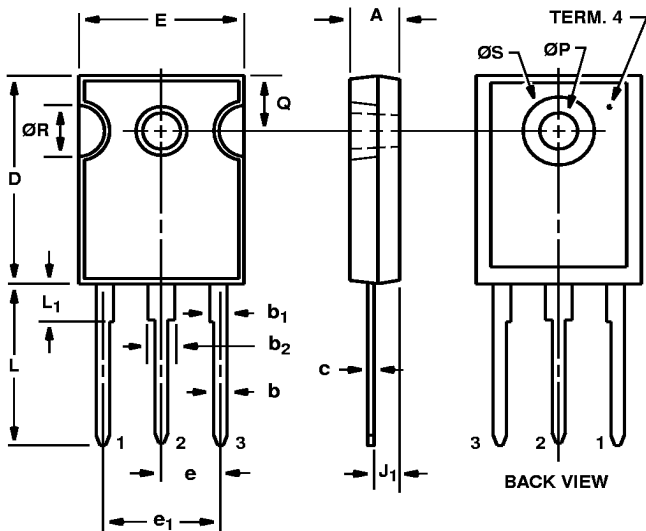
CTHERM1 7 6 4.9e-7
 CHERM2 6 5 4.5e-4
 CHERM3 5 4 1.8e-3
 CHERM4 4 3 8.5e-3
 CHERM5 3 2 1.35e-1
 CHERM6 2 1 3

RHERM1 7 6 6e-6
 RHERM2 6 5 7e-3
 RHERM3 5 4 5.5e-2
 RHERM4 4 3 5.4e-1
 RHERM5 3 2 3.5e-1
 RHERM6 2 1 4.5e-2



TO-247

3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



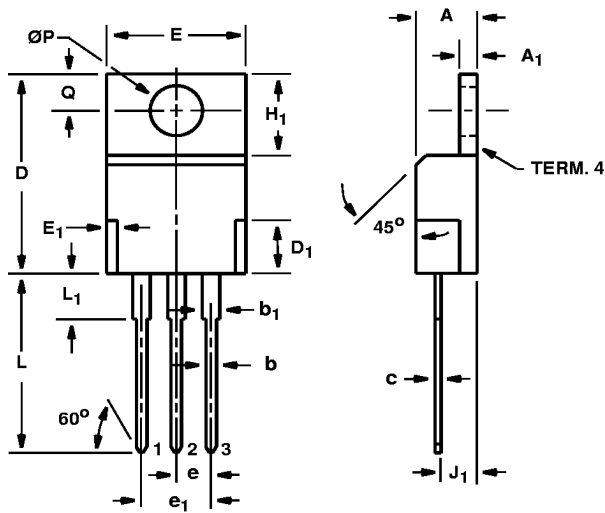
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b ₁	0.060	0.070	1.53	1.77	1, 2
b ₂	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e ₁	0.438 BSC		11.12 BSC		4
J ₁	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L ₁	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L₁.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

TO-220AB

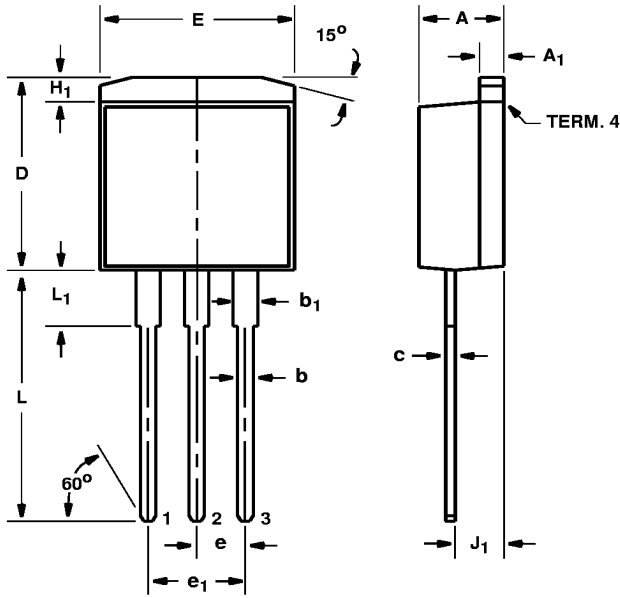
3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D ₁	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E ₁	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.235	0.255	5.97	6.47	-
J ₁	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.130	0.150	3.31	3.81	2
$\varnothing P$	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

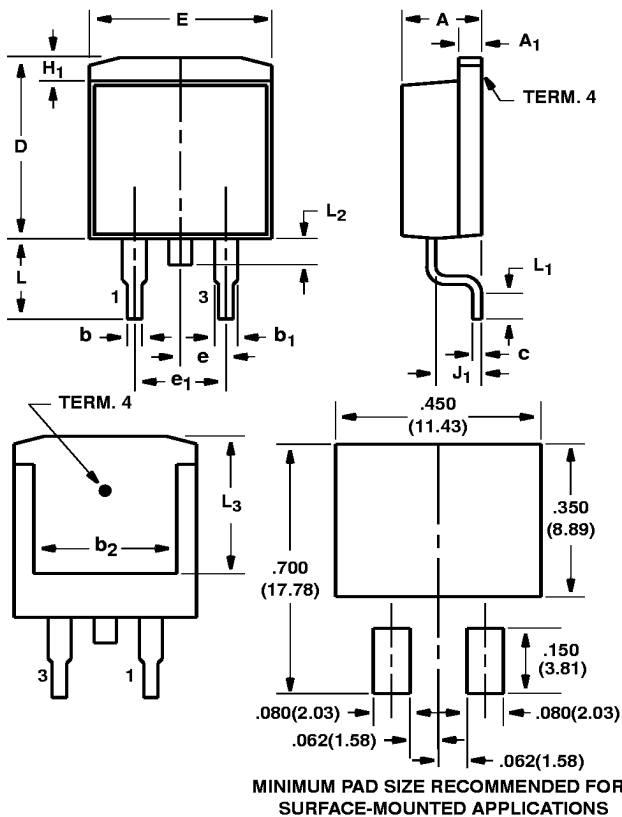
1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1 .
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

TO-262AA 3 LEAD JEDEC TO-262AA PLASTIC PACKAGE


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.110	0.130	2.80	3.30	2

NOTES:

- These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
- Solder finish uncontrolled in this area.
- Dimension (without solder).
- Add typically 0.002 inches (0.05mm) for solder plating.
- Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
- Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
- Controlling dimension: Inch.
- Revision 5 dated 7-97.

TO-263AB SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE


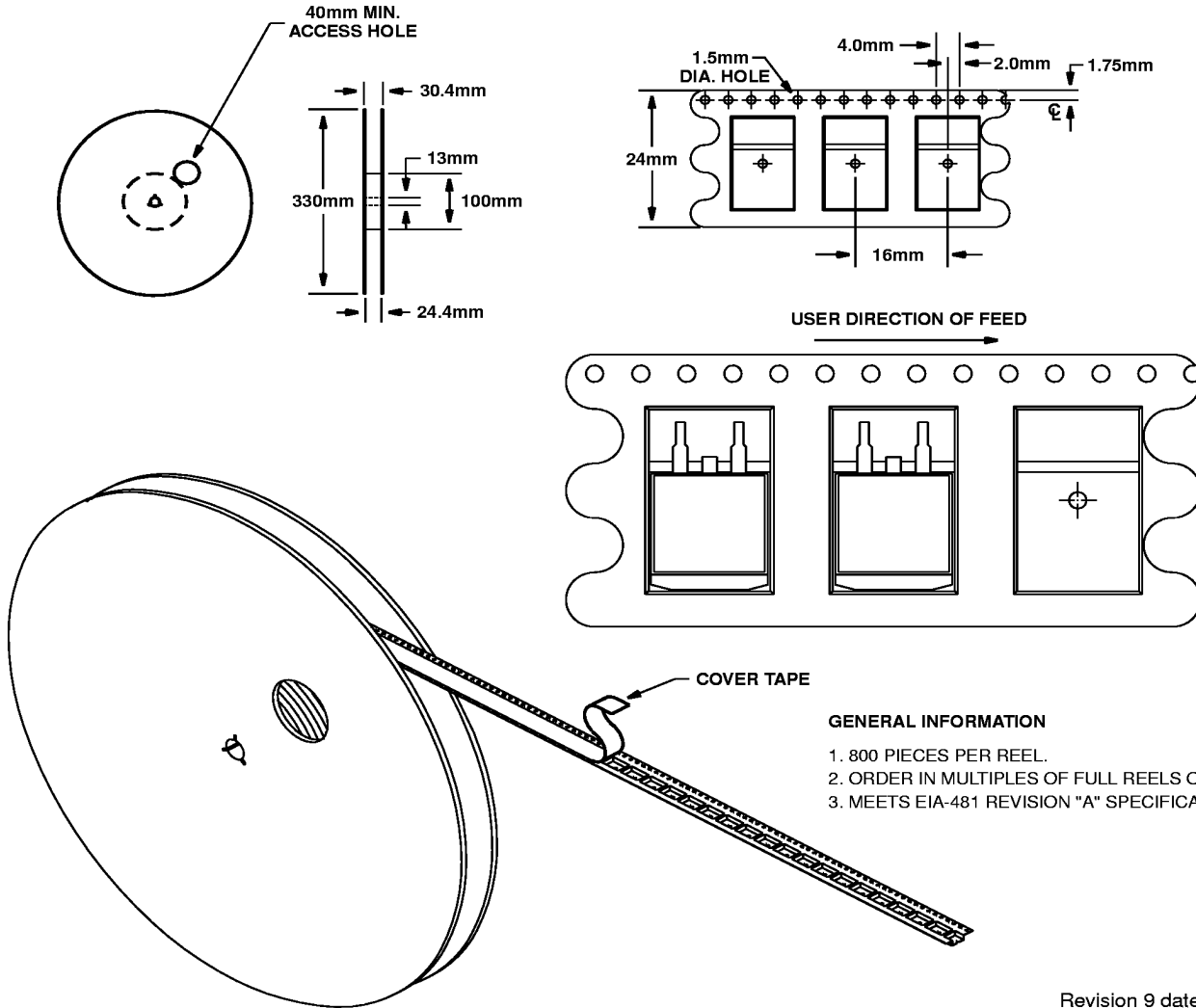
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b ₁	0.045	0.055	1.15	1.39	4, 5
b ₂	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e ₁	0.200 BSC		5.08 BSC		7
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L ₁	0.090	0.110	2.29	2.79	4, 6
L ₂	0.050	0.070	1.27	1.77	3
L ₃	0.315	-	8.01	-	2

NOTES:

- These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
- L₃ and b₂ dimensions established a minimum mounting surface for terminal 4.
- Solder finish uncontrolled in this area.
- Dimension (without solder).
- Add typically 0.002 inches (0.05mm) for solder plating.
- L₁ is the terminal length for soldering.
- Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
- Controlling dimension: Inch.
- Revision 9 dated 1-98.

TO-263AB

24mm TAPE AND REEL



Revision 9 dated 1-98