PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

# ID240E01

## 4MB Flash Memory Card

(Model No.: ID240E01)

Spec No.: EL105110

Issue Date: May 27, 1998

●When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2). even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

●Please direct all queries regarding the products covered herein to a sales representative of the company.

## Contents

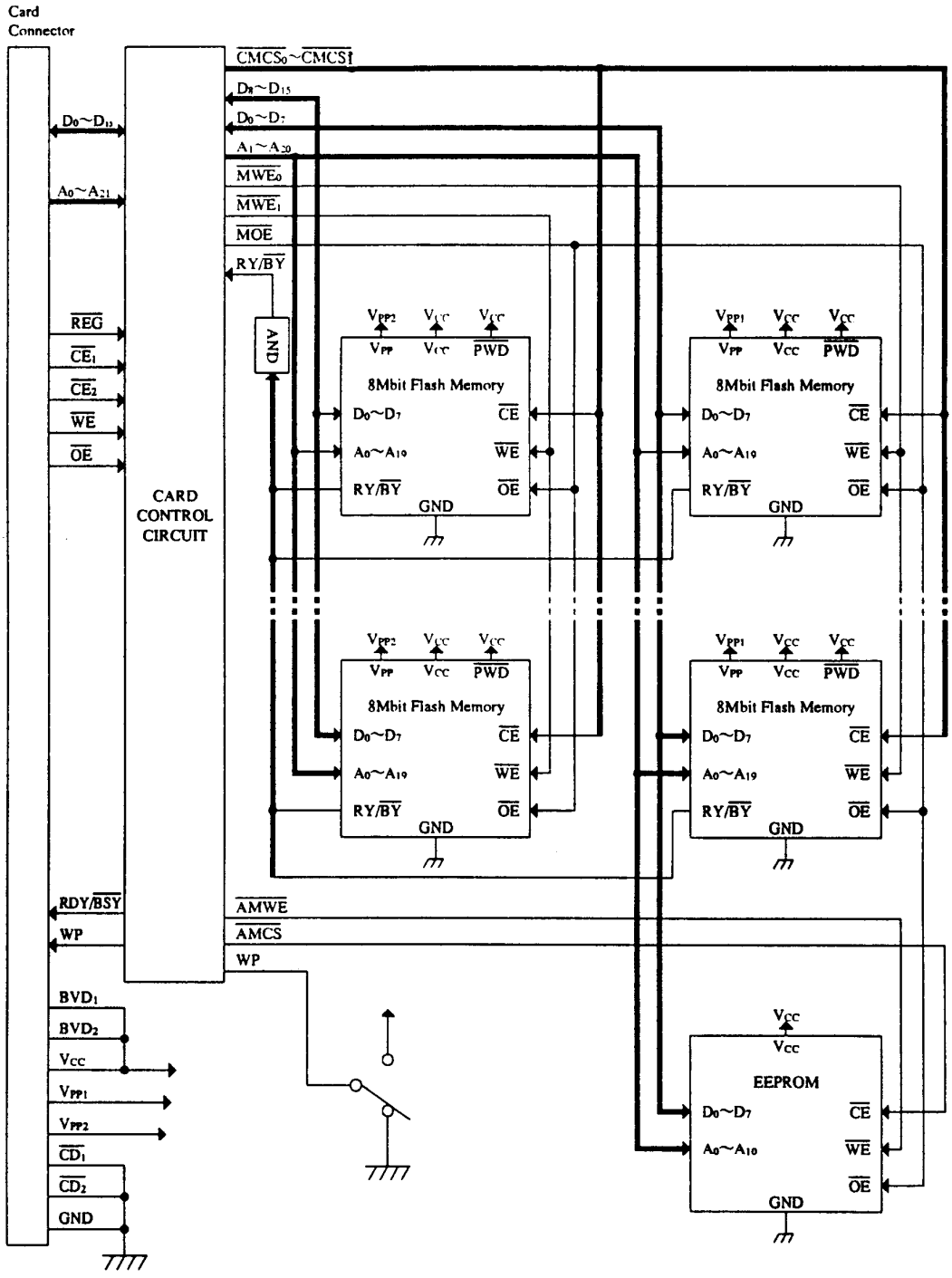
## 1. General Descriptions

The SHARP ID240E01 is a 4MB Flash Memory PC Card conforms to PCMCIA Release 2.0 and is offered to customers giving aim to confirm an external shape or electrical performances of the card. Before mass production, we will create a new product name dedicated for a customer and also present a specification which implies customer's request including panel design.

## 2. Features

| | | |
|---|---|---|
| 2.1 | Type | 4MB Flash Memory Card<br>(Conforms to PCMCIA Rel.2.0) |
| 2.2 | Memory Capacity | |
| | Common Memory | 4M words × 8 bits or 2M words × 16 bits |
| | Attribute Memory | EEPROM Model 2k words × 8 bits read/write |
| | Note) We have another type of attribute memory as follows,<br>No EEPROM Model. (5 words × 8 bits read only in card's control circuit.)<br>Sample card name: ID240E02. Customers can choose one model from two. | |
| 2.3 | Supply Voltage | |
| | Read Cycle | $V_{CC}=5\pm0.5V$, $V_{PP1}$, $V_{PP2}=0\sim1.5V$ |
| | Read/Program/Erase Cycle | $V_{CC}=5\pm0.5V$, $V_{PP1}$, $V_{PP2}=12.0V\pm0.6V$ |
| 2.4 | Erase Unit | Block<br>(64k bytes/byte access, 128k bytes/word access) |
| 2.5 | Program/Erase Cycles | 100,000 cycles |
| 2.6 | Interface | Parallel I/O Interface |
| 2.7 | Function Table | See Function Table in page. 6 |
| 2.8 | External Dimensions | 54 × 85.6 × 3.3 mm |
| 2.9 | Pin Connections | See Pin Connections in page. 4 |
| 2.10 | Type of Connector | Conforms to PCMCIA Re1.2.0 Card Use Connector<br>(Card connector: JC20-J68S-NB3 JAE or FCN-568J068-G/0 Fujitsu or ICM-C68S-TS13-5035A JST) |
| 2.11 | Average Weight | 30g |
| 2.12 | Operating Temp Range | 0 to 60℃ |
| 2.13 | Storage Temp Range | −20 to 65℃ |
| 2.14 | External Appearance | External appearance shall be free of any dirt, cratches and abnormalities that could adversely affect sales. |
| 2.15 | Manufacturer's Code | The manufacturer's code shall be printed on the memory card directly or on the seal which is then attached to the memory card. |
| 2.16 | Brand Name | The user's brand name will be used. |
| 2.17 | Not designed or rated radiation hardened. | |

## 3. Block Diagram



## 4. Pin Connections

| PIN | SIGNAL | PIN | SIGNAL | PIN | SIGNAL | PIN | SIGNAL |
|---|---|---|---|---|---|---|---|
| 1 | GND | 18 | $V_{PP1}$ | 35 | GND | 52 | $V_{PP2}$ |
| 2 | $D_3$ | 19 | $A_{16}$ | 36 | $\overline{CD_1}$ | 53 | $A_{22}$ (NC) |
| 3 | $D_4$ | 20 | $A_{15}$ | 37 | $D_{11}$ | 54 | $A_{23}$ (NC) |
| 4 | $D_5$ | 21 | $A_{12}$ | 38 | $D_{12}$ | 55 | $A_{24}$ (NC) |
| 5 | $D_6$ | 22 | $A_7$ | 39 | $D_{13}$ | 56 | $A_{25}$ (NC) |
| 6 | $D_7$ | 23 | $A_6$ | 40 | $D_{14}$ | 57 | NC |
| 7 | $\overline{CE_1}$ | 24 | $A_5$ | 41 | $D_{15}$ | 58 | NC |
| 8 | $A_{10}$ | 25 | $A_4$ | 42 | $\overline{CE_2}$ | 59 | NC |
| 9 | $\overline{OE}$ | 26 | $A_3$ | 43 | NC | 60 | NC |
| 10 | $A_{11}$ | 27 | $A_2$ | 44 | NC | 61 | $\overline{REG}$ |
| 11 | $A_9$ | 28 | $A_1$ | 45 | NC | 62 | $BVD_2$ |
| 12 | $A_8$ | 29 | $A_0$ | 46 | $A_{17}$ | 63 | $BVD_1$ |
| 13 | $A_{13}$ | 30 | $D_0$ | 47 | $A_{18}$ | 64 | $D_8$ |
| 14 | $A_{14}$ | 31 | $D_1$ | 48 | $A_{19}$ | 65 | $D_9$ |
| 15 | $\overline{WE}/\overline{PGM}$ | 32 | $D_2$ | 49 | $A_{20}$ | 66 | $D_{10}$ |
| 16 | RDY/$\overline{BSY}$ | 33 | WP | 50 | $A_{21}$ | 67 | $\overline{CD_2}$ |
| 17 | $V_{CC}$ | 34 | GND | 51 | $V_{CC}$ | 68 | GND |

Pin Descriptions :

| | |
|---|---|
| $D_0 \sim D_7$ | Data Bus (Input/output) |
| $D_8 \sim D_{15}$ | Data Bus (Input/output) |
| $A_0 \sim A_{22}$ | Address Bus (Input) |
| $\overline{CE_1}$, $\overline{CE_2}$ | Card Enable (Input) |
| $\overline{OE}$ | Output Enable (Input) |
| $\overline{WE}/\overline{PGM}$ | Write Enable/Program (Input) |
| $\overline{CD_1}$, $\overline{CD_2}$ | Card Detect (Output) (Card Inserted Detection Signal) |
| WP | Write Protect (Output) (in write protect mode, the WP output signal is "HIGH") |
| $V_{PP1}$ | Program/Erase Power Supply (Even Byte) |
| $V_{PP2}$ | Program/Erase Power Supply (Odd Byte) |
| $\overline{REG}$ | Register Select (Input) |
| $BVD_1$, $BVD_2$ | Battery Voltage Detect (Always "HIGH") |
| RDY/$\overline{BSY}$ | Ready/Busy (Output) |

# 5. Function

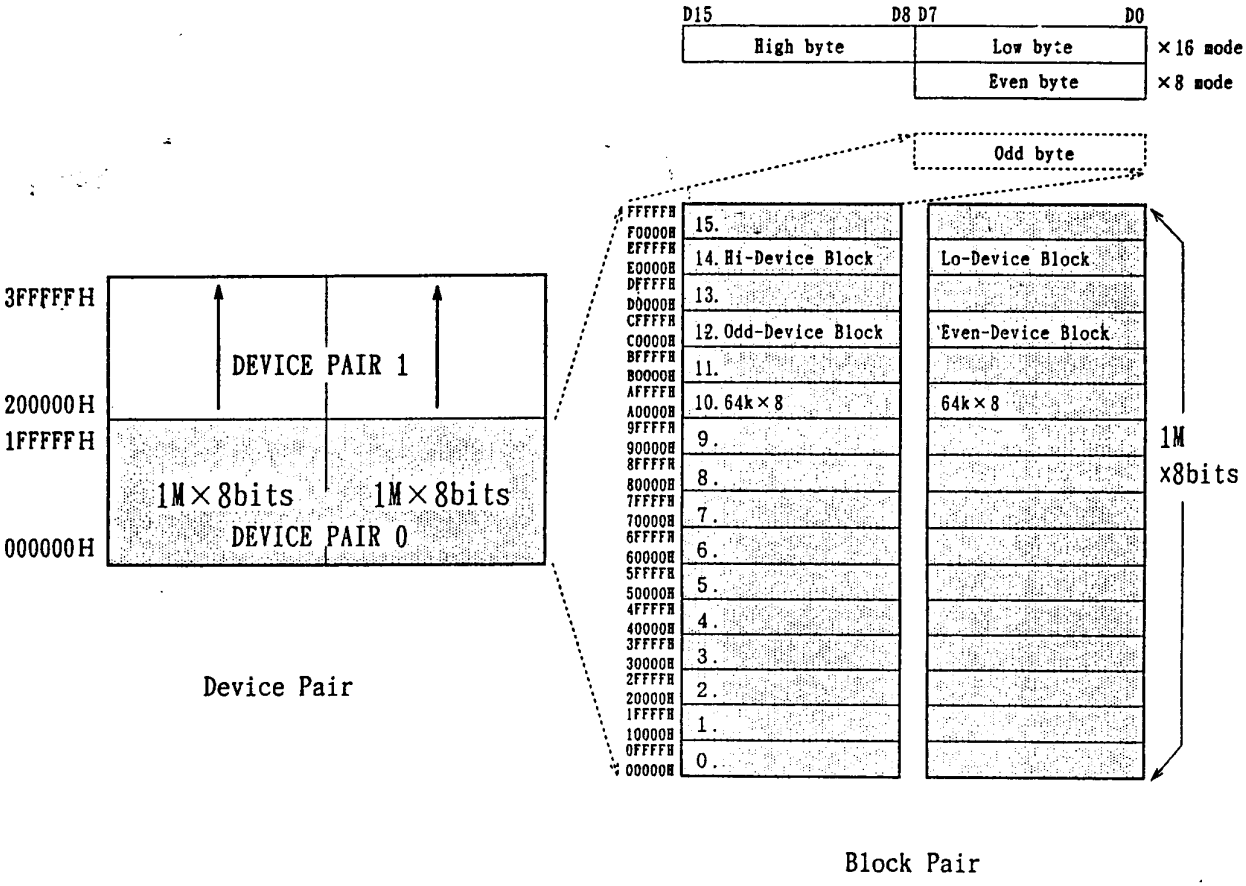
## 5.1 Memory Block

5.1.1 Memory Configuration 8Mbits Flash Memory× 4 Devices.

5.1.2 Memory Erase Unit Block Erase

Block: Byte Mode 64k bytes

Word Mode 128k bytes



## 5.2 Function Table

| $\overline{CE_1}$ | $\overline{CE_2}$ | $A_0$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{REG}$ | $V_{PP1}$ | $V_{PP2}$ | $V_{CC}$ | Operation | $D_0$-$D_7$ | $D_8$-$D_{15}$ | Status |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | H | × | × | × | H | $V_{PPL}$ | $V_{PPL}$ | $V_{CC}$ | | Hi-Z | Hi-Z | Standby |
| L | H | L | H | L | H | $V_{PPL}$ | $V_{PPL}$ | $V_{CC}$ | Read (×8) | Do (Even) | Hi-Z | Byte |
| L | H | H | H | L | H | $V_{PPL}$ | $V_{PPL}$ | $V_{CC}$ | Read (×8) | Do (Odd) | Hi-Z | Byte |
| L | L | × | H | L | H | $V_{PPL}$ | $V_{PPL}$ | $V_{CC}$ | Read (×16) | Do (Even) | Do (Odd) | Word |
| H | L | × | H | L | H | $V_{PPL}$ | $V_{PPL}$ | $V_{CC}$ | Read (×8) | Hi-Z | Do (Odd) | Byte |
| L | × | × | × | H | H | $V_{PPL}$ | $V_{PPL}$ | $V_{CC}$ | Outpu Disable | Hi-Z | Hi-Z | Byte |
| H | L | × | × | H | H | $V_{PPL}$ | $V_{PPL}$ | $V_{CC}$ | Outpu Disable | Hi-Z | Hi-Z | Byte |
| L | H | L | L | H | H | $V_{PPH}$ | $V_{PPX}$ | $V_{CC}$ | Program (×8) | Di (Even) | Don't care | Byte |
| L | H | H | L | H | H | $V_{PPX}$ | $V_{PPH}$ | $V_{CC}$ | Program (×8) | Di (Odd) | Don't care | Byte |
| L | L | × | L | H | H | $V_{PPH}$ | $V_{PPH}$ | $V_{CC}$ | Program (×16) | Di (Even) | Di (Odd) | Word |
| H | L | × | L | H | H | $V_{PPX}$ | $V_{PPH}$ | $V_{CC}$ | Program (×8) | Don't care | Di (Odd) | Byte |
| L | H | L | H | L | H | $V_{PPH}$ | $V_{PPX}$ | $V_{CC}$ | Verify (×8) | Do (Even) | Hi-Z | Byte |
| L | H | H | H | L | H | $V_{PPX}$ | $V_{PPH}$ | $V_{CC}$ | Verify (×8) | Do (Odd) | Hi-Z | Byte |
| L | L | × | H | L | H | $V_{PPH}$ | $V_{PPH}$ | $V_{CC}$ | Verify (×16) | Do (Even) | Do (Odd) | Word |
| H | L | × | H | L | H | $V_{PPX}$ | $V_{PPH}$ | $V_{CC}$ | Verify (×8) | Hi-Z | Do (Odd) | Byte |
| L | H | H | L | L | H | $V_{PPH}$ | $V_{PPX}$ | $V_{CC}$ | *1 Prohibited | — | — | — |
| L | H | L | L | L | H | $V_{PPX}$ | $V_{PPH}$ | $V_{CC}$ | *1 Prohibited | — | — | — |
| L | L | × | L | L | H | $V_{PPH}$ | $V_{PPH}$ | $V_{CC}$ | *1 Prohibited | — | — | — |
| H | L | × | L | L | H | $V_{PPX}$ | $V_{PPH}$ | $V_{CC}$ | *1 Prohibited | — | — | — |

*1. Do not use this mode as it will result in write errors.

H : High L : Low × : Don't Care

Di : Input Data Do : Output Data Hi-Z : High Impedance

$V_{CC}$ : 4.5 ~ 5.5V $V_{PPL}$ : 0.0 ~ 1.5V $V_{PPH}$ : 11.4 ~ 12.6V

$V_{PPX}$ : $V_{PPL}$ or $V_{PPH}$

Caution: When the write Protect switch is in protect-mode, the WP signal is "HIGH" and write operation are not allowed.

## 5.3 Software Command (8/16 Bits Operation ( ):16 Bits Operation)

| Command | Bus Cycles | First Bus Cycle | | | Second Bus Cycle | | | |
|---|---|---|---|---|---|---|---|---|
| | | Operation | Address | Data | Operation | Address | Data Input | Data Output |
| Read Array/Reset | 1 | Write | RA | FFH/ (FFFFH) | — | — | — | — |
| Read Intelligent Identifier | 3 | Write | DA | 90H/ (9090H) | Read | IA | — | IID |
| Read Status Register | 2 | Write | DA | 70H/ (7070H) | Read | DA | — | SRD |
| Clear Status Register | 1 | Write | DA | 50H/ (5050H) | — | — | — | — |
| Erase Setup/Erase Confirm | 2 | Write | BA | 20H/ (2020H) | Write | BA | D0H/ (D0D0H) | — |
| Erase Suspend/Erase Resume | 2 | Write | BA | B0H/ (B0B0H) | Write | BA | D0H/ (D0D0H) | — |
| Byte Write Setup/Write | 2 | Write | WA | 40H/ (4040H) | Write | WA | WD | — |
| Alternate Byte Write Setup/Write | 2 | Write | WA | 10H/ (1010H) | Write | WA | WD | — |

Note) 1. This Table shows the basic from of Erase, Verify and Program Verify.
Refer Programming Flowchart, Erase Algorithm in detail.

2. Bus operations are defined in function table in page.

3. IA : Device Identifier Address IID : Device Identifier Data

| | DA | IA | | | IID | |
|---|---|---|---|---|---|---|
| | | 8Bits (Even Device) | 8Bits (Odd Device) | 16Bits | Byte (8Bits) | Word (16Bits) |
| Manufacturer Code | 000000H～1FFFFFH | 000000H | 000001H | 000000H | 89H | 8989H |
| Device Code | 000000H～1FFFFFH | 000002H | 000003H | 000001H | A2H | A2A2H |

RA : Read Address WA : Write Address WD : Write Data

DA : Device Address (Any Address in device is acceptable.)

BA : Erase Block Address (Erase Size is 64k Bytes.)

SRD : Status Register Data

4. Either 40H (4040H) or 10H (1010H) are recognized by the WSM as the Byte Write Setup Command.

a) Read Array/Reset Command: (FFH/FFFFH)

By writing this command, device. Devices pair become read mode. The device remains enable for reads until the Command User Interface contents are altered.

b) Intelligent Identifier Command: (90H/9090H):

After writing this command into the Command User Interface, a read cycle retrieves the manufacturer Code and device Code. To terminate the Operation, it is necessary to write another valid command into the register.

c) Read Status Register Command: (70H/7070H):

By Writing this command, the Status Register may be read at any time to determine when a byte or block erase operation is complete, and whether that operation completed successfully.

Refer to Status Register definition in page. 9. After writing this command, all subsequent read operations output data from the Status Register, until another valid command is written to the Command User Interface.

d) Clear Status Register Command: (50H/5050H)

Status bits which show error, the Erase Status (SR. 5), Byte Write Status (SR. 4) bits and the $V_{PP}$ Status bit (SR. 3) can be reset by the Clear Status Machine Register Command.

e) Erase Setup/Erase Command: (20H/2020H) (D0H/D0D0H): Erase is executed one block (64kB for 1 device, 128kB for 2 devices) at a time.

This command is functional when $V_{PP} = V_{PPH}$ and an Erase Setup Command is first written to the Command User Interface, followed by the Erase Confirm Command. After that, the device automatically outputs Status Register data when read.

The CPU can detect the completion of the erase event by analyzing the output of the RDY/$\overline{BSY}$ pin, or the WSM Status bit of the Status Register. When erase is completed, the Erase Status bit should be checked. If erase error is detected, the Status Register should be cleared.

f) Erase Supend/Erase Resume Command: (B0H/B0B0H) / (D0H/D0D0H)

The Erase Suspend command allows block erase interruption in order to read data from another block of memory. The device continues to output Status Register data when read, after the Erase Suspend Command is written. Polling the WSM Status and Erase Suspend Status bits will determine when the erase operation has been suspended. RDY/$\overline{BSY}$ pin will also transition to $V_{OH}$. At this point, a Read Array Command can be written to the Command User Interface to read data from blocks other than that which is suspended. $V_{PP}$ must remain at $V_{PPH}$ while device is in Erase Suspend.

Erase Resume Command, at which time the WSM will continue with the erase process. The Erase Suspend Status and WSM Status bits of the Status Register will be automatically cleared and RDY/$\overline{BSY}$ pin will return to $V_{OL}$. After the Erase Resume is written, the device automatically output Status Register data when read.

g) Byte Write Setup/Write Command: (40H/4040H) or (10H/1010H)

This command is functional when $V_{PP} = V_{PPH}$ and an Byte Write Setup Command is first written to the Command User Interface, followed by a second write specifying the address and data to be written. The WSM then take over, controlling the byte write and write verify algorithms internally. After the two command byte sequence is written to it, the device automatically outputs Status Register data when read. The CPU can detect the completion of the byte write event by analyzing the output of the RDY/$\overline{BSY}$ pin, or the WSM Status bits of the Status Register.

## 5.4 Status Register

The memory devices in this card have Status Register which shows state of the device.

Byte Access×8 Bits

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| SR.7 | SR.6 | SR.5 | SR.4 | SR.3 | SR.2 | SR.1 | SR.0 |
| WSMS | ESS | ES | BWS | VPPS | RFU | RFU | RFU |

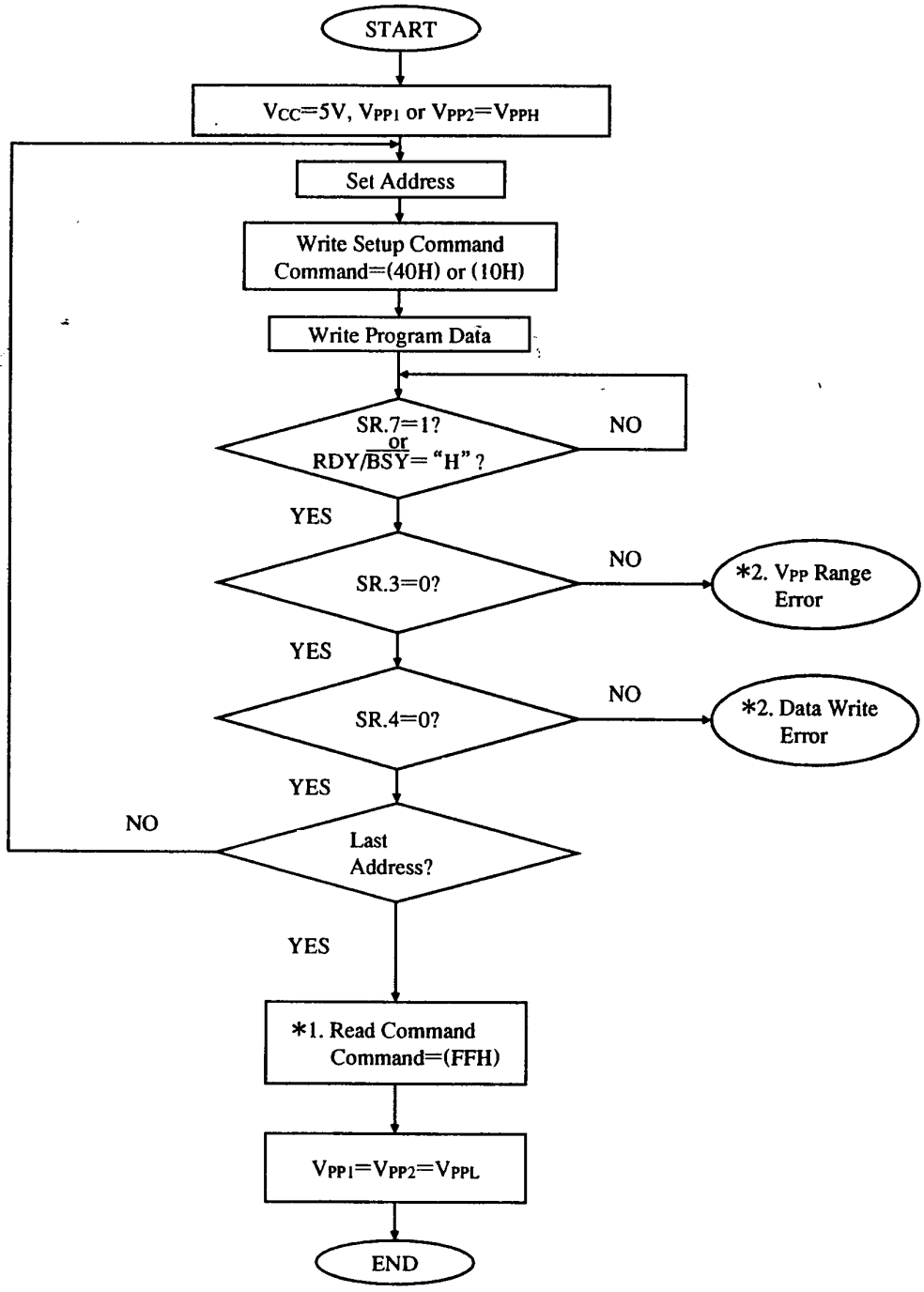
| Register | Contents |
|---|---|
| SR.7=Write State Machine Status<br>1=Ready<br>0=Busy | When set "1" s, read, erase, data write is acceptable. |
| SR.6=Erase Suspend Status<br>1=Erase Suspend<br>0=Erase In Progress/Completed | Check whether Erase Suspend Command is executed or not. |
| SR.5=Erase Status<br>1=Error In Block Erase<br>0=Successful Block Erase | Set "1" s when fail to Erase.<br>Reset by the Clear Status Register Command. |
| SR.4=Byte Write Status<br>1=Error In Byte Write<br>0=Successful Byte Write | Set "1" s when fail to Byte Write.<br>Reset by the Clear Status Register Command. |
| SR.3=$V_{PP}$ Status<br>1=$V_{PP}$ Low Detect ; Operation Abort<br>0=$V_{PP}$ OK | Set "1" s when $V_{PP}$, which is needed in Byte Write or Erase operation, is below $V_{PPH}$. Reset by the Clear Status Register Command. |
| SR.2~SR.0=Reserved for Future Use | |

Word Access×16 bits

| bit15 | | | | | | | bit8 | bit7 | | | | | | | bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SR.15 | SR.14 | SR.13 | SR.12 | SR.11 | SR.10 | SR.9 | SR.8 | SR.7 | SR.6 | SR.5 | SR.4 | SR.3 | SR.2 | SR.1 | SR.0 |
| Odd Byte device | | | | | | | | Even Byte device | | | | | | | |

## 5.5 Programming Flowchart

(Byte Mode)

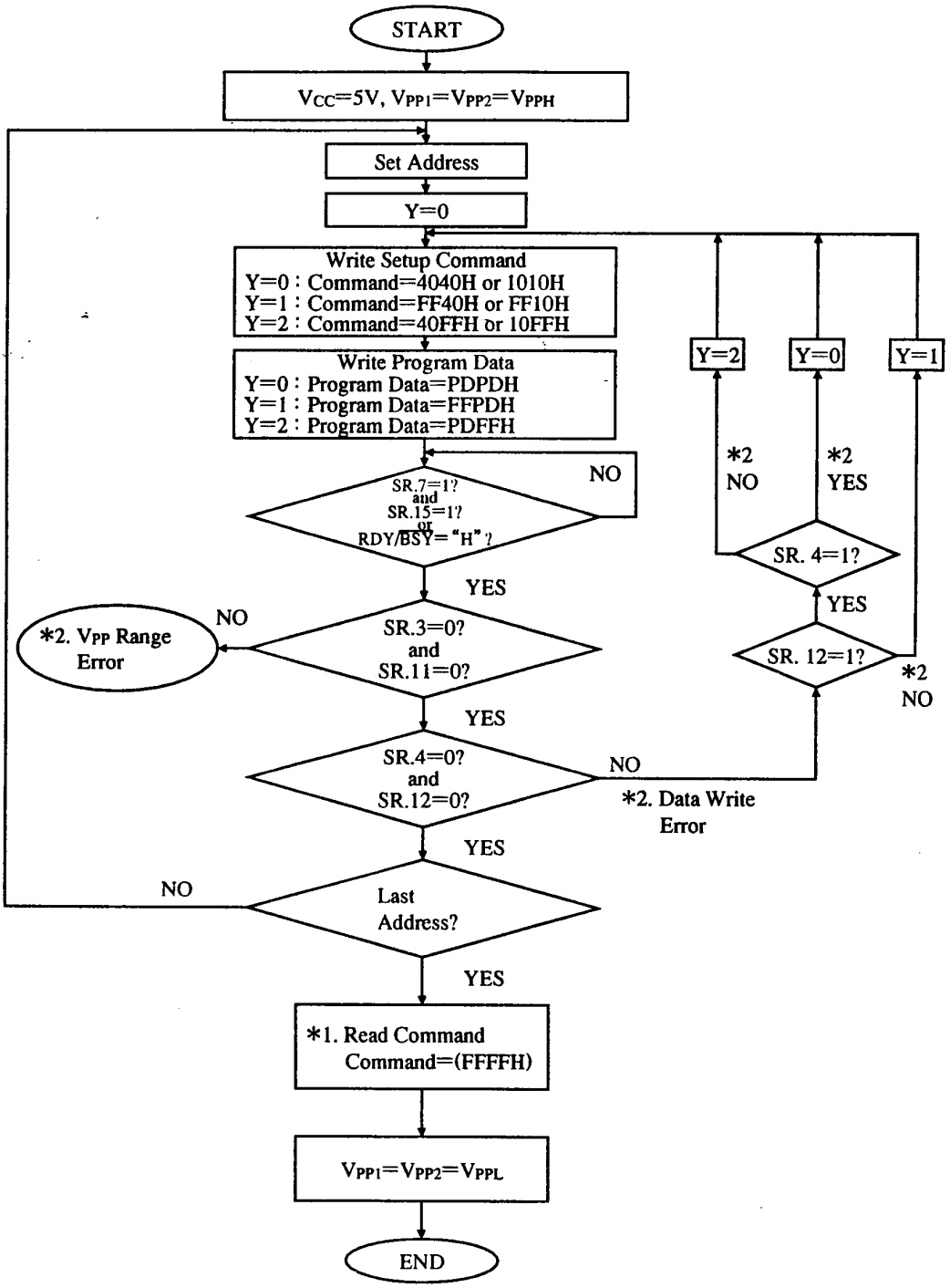



Note) *1. Write FFH after the last block write operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

Programming Flowchart

(Word Mode)

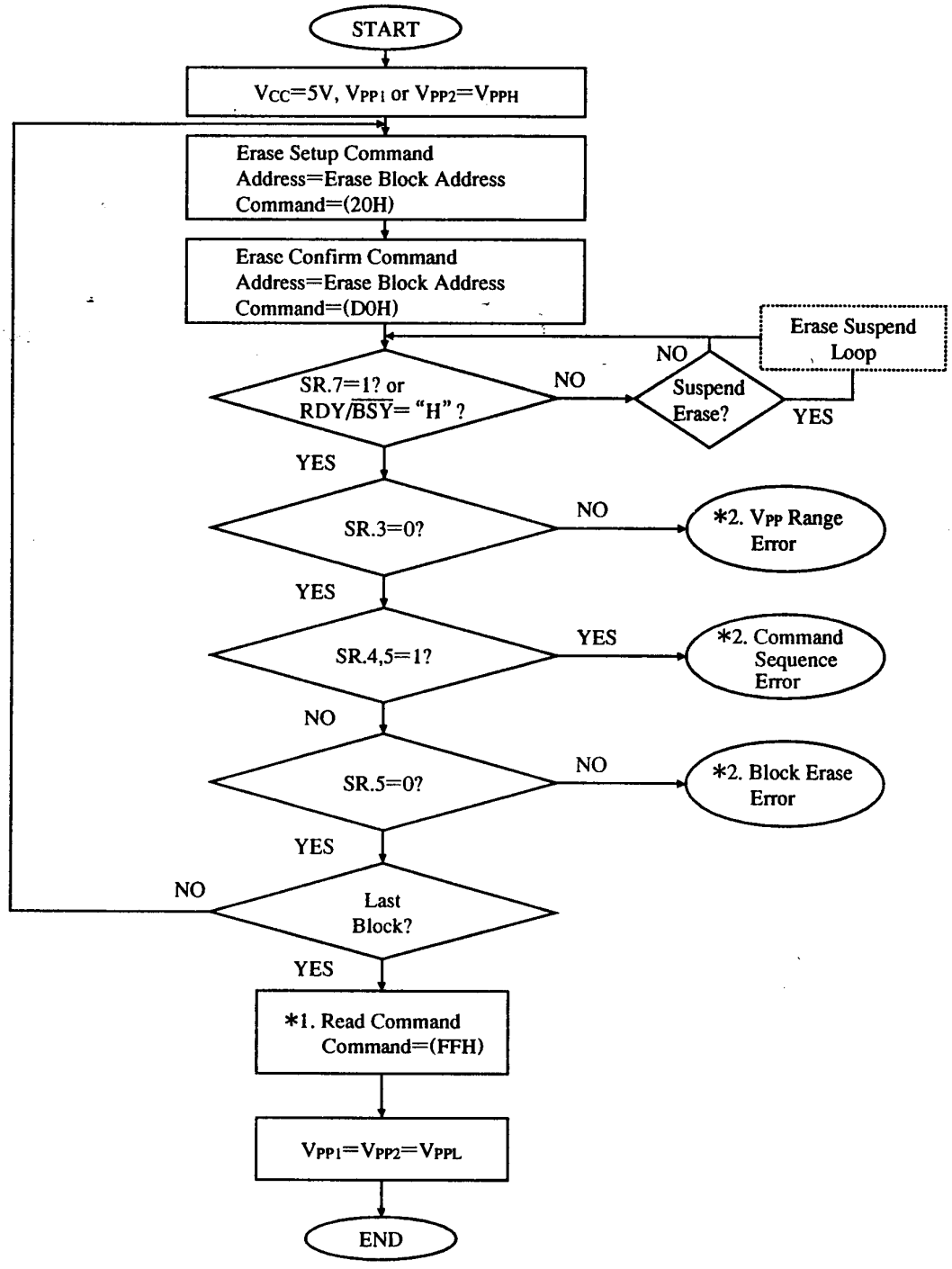



Note) *1. Write FFFFH after the last block write operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

## 5.6 Erase Algorithm

(Byte Mode)

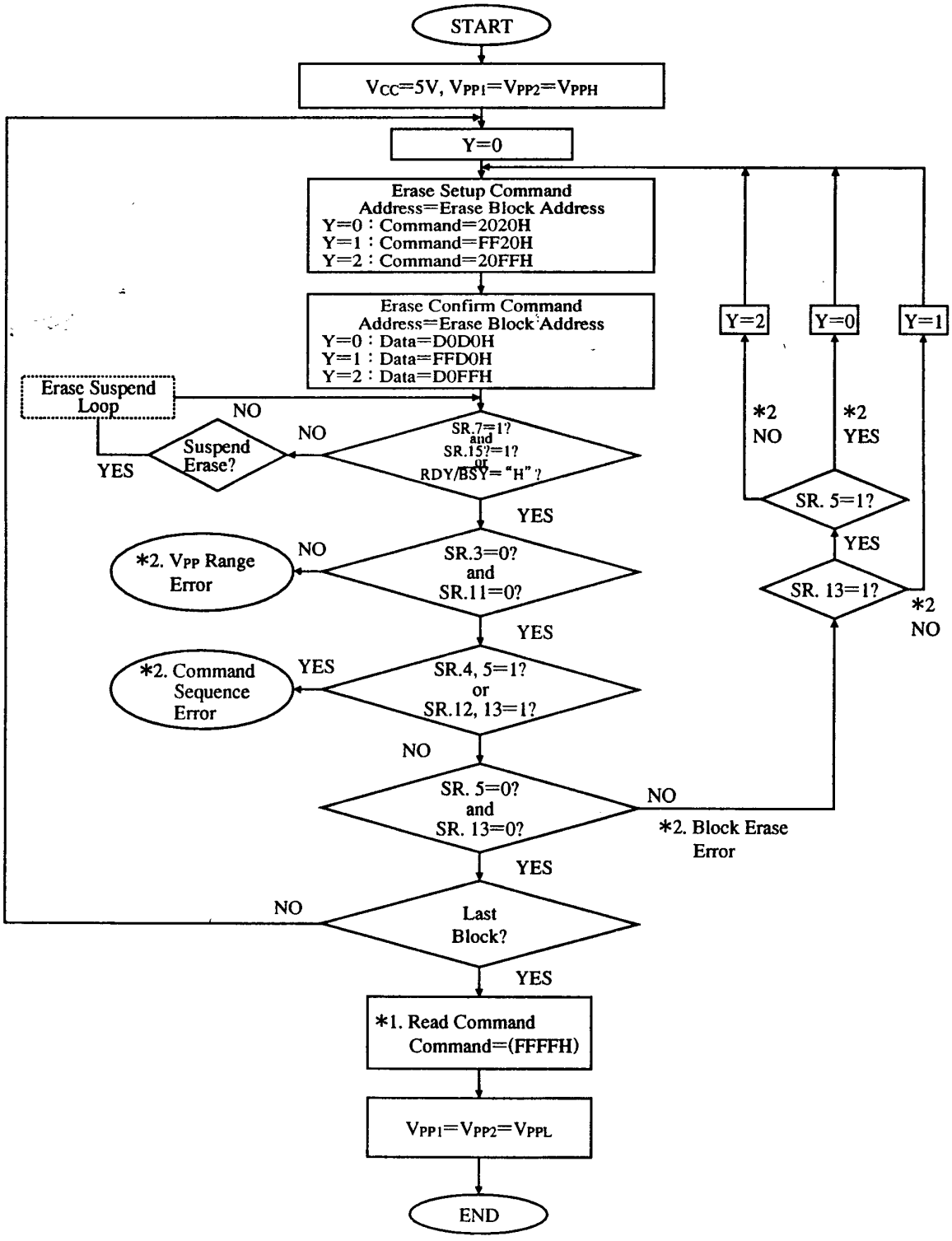



Note) * 1. Write FFH after the last block erase operation to reset the device to Read Array Mode.

* 2. If error is detected, clear the Status Register before attempting retry or other error recovery.

Erase Algorithm

(Word Mode)




Note) *1. Write FFFFH after the last block erase operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

## 6. Absolute Maximum Ratings

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to 7.0 | V |
| Input Voltage | $V_{IN}$ | −0.3 to $V_{CC}$+0.3 (Max : 7.0) | V |
| Output Voltage | $V_{OUT}$ | −0.3 to $V_{CC}$+0.3 (Max : 7.0) | V |
| Operating Temperature | $T_{OPR}$ | 0 to+60 | ℃ |
| Storage Temperature | $T_{STG}$ | −20 to+65 | ℃ |

## 7. Recommended Operating Conditions

| PARAMETER | SYMBOL | Min. | Max. | UNIT |
|---|---|---|---|---|
| Operating Temperature | $T_{OPR}$ | 0 | +60 | ℃ |
| Supply Voltage | $V_{CC}$ | 4.5 | 5.5 | V |
| Input Voltage High | $V_{IH}$ | 3.5 | $V_{CC}$+0.3 | V |
| Input Voltage Low | $V_{IL}$ | −0.3 | 1.5 | V |

## 8. Capacitance

| PARAMETER | SYMBOL | Min. | TYP | Max. | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | — | 17 | — | pF | $V_{CC}$=5V±10% |
| Input/Output Capacitance | $C_{IO}$ | — | 17 | — | pF | f=1MHz, Ta=25℃ |

# 9. Read Operation

## 9.1 DC Characteristics

($V_{CC}$=4.5~5.5V, Ta=0~60℃)

| PARAMETER | | SYMBOL | Min. | TYP | Max. | UNIT | CONDITION |
|---|---|---|---|---|---|---|---|
| Operating Voltage | High Temperature / Low Temperature | $V_{CC}$ | 4.5 | — | 5.5 | V | |
| Current Consumption *1 | Static Operatin Current | $I_{SB}$ | — | — | 2.0 | mA | X16, Address : PingPong |
| | Dynamic Operating Current | $I_{CC}$ | — | — | 80 | | |
| Input Voltage | Input Voltage Level High | $V_{IH}$ | 3.5 | — | $V_{CC}$+0.3 | V | $V_{CC}$=4.5~5.5V |
| | Input Voltage Level Low | $V_{IL}$ | −0.3 | — | 1.5 | | |
| Input Current | $A_0$~$A_{20}$, $D_0$~$D_{15}$ | $I_{LI}$ | −10 | | 70 | μA | $V_I$=$V_{CC}$, 0V |
| | $\overline{CE_1}$, $\overline{CE_2}$, $\overline{OE}$, $\overline{WE}$, $\overline{REG}$ | | −70 | — | 10 | | |
| Output Voltage | High | $V_{OH}$ | $V_{CC}$~0.5 | — | — | V | $I_{OH}$=−2mA (*2)<br>$I_{OH}$=−4 μA (*3) |
| | Low | $V_{OL}$ | — | — | 0.4 | | $I_{OL}$=4mA |

PingPong : Scan the target address, with accessing the target and another address alternately.

*1 (1) Static Operating Current : With the memory card's voltage at 5.5V and the $\overline{CE_1}$, $\overline{CE_2}$ $\overline{OE}$, $\overline{WE}$ and $\overline{REG}$ signals "HIGH" ($V_{IH}$=$V_{CC}$−0.2V), $A_0$ signal "LOW" ($V_{IL}$≦0.2V) the current consumption is measured with the output open.

(2) Dynamic Operating Current : With the memory card's $V_{CC}$ at 5.5V and $V_{PP1}$=$V_{PP2}$ at 12.6V, current consumption during access is measured with the output open.
(Access time : 200ns) The current depends on addressing.

*2 $D_0$~$D_{15}$

*3 $BVD_1$, $BVD_2$, RDY/$\overline{BSY}$, WP

## 9.2 AC Characteristics ($V_{CC}$=4.5~5.5V, $V_{PP}$=0.0~1.5V, Ta=0~60℃)

Testing Conditions:

1) Input Pulse Level : 0.8~3.5V
2) Input Rise/Fall Time : 10ns
3) Input/Output Timing Reference Level : 1.5V
4) Output Load : 1TTL+$C_L$ (100pF) (including scope and jig capacitance)

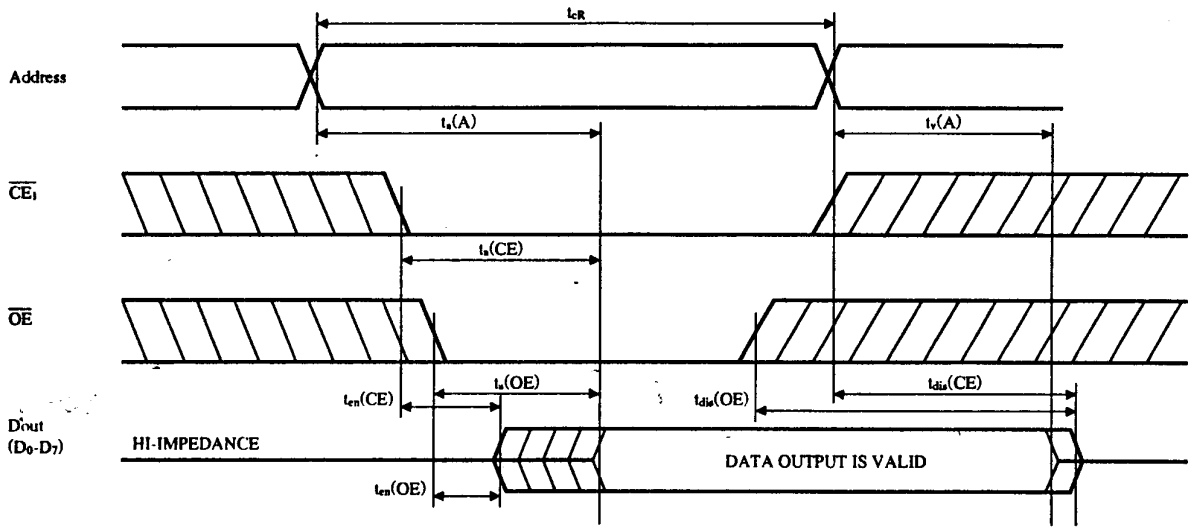
### 9.2.1 Read Cycle

($V_{CC}$=4.5~5.5V, $V_{PP}$=0.0~1.5V, Ta=0~60℃)

| PARAMETER | SYMBOL | SYMBOL (PCMCIA) | Min. | Max. | UNIT |
|---|---|---|---|---|---|
| Read Cycle Time | $t_{AVAV}$ | $t_{cR}$ | 200 | — | ns |
| Address Access Time | $t_{AVQV}$ | $t_a$ (A) | — | 200 | |
| Card Enable Access Time | $t_{ELQV}$ | $t_a$ (CE) | — | 200 | |
| Output Enable Access Time | $t_{GLQV}$ | $t_a$ (OE) | — | 100 | |
| Output Disable Time from $\overline{CE}$* | $t_{EHQV}$ | $t_{dis}$ (CE) | — | 90 | |
| Output Disable Time from$\overline{OE}$* | $t_{GHQZ}$ | $t_{dis}$ (OE) | — | 90 | |
| Output Enable Time from $\overline{CE}$ | $t_{ELQX}$ | $t_{en}$ (CE) | 5 | — | |
| Output Enable Time form $\overline{OE}$ | $t_{GLQX}$ | $t_{en}$ (OE) | 5 | — | |
| Data Valid from Add Change | | $t_v$ (A) | 0 | — | |

* Time until output becomes floating. (The output voltage is not defined.)

○Read CYCLE (1) ($\overline{CE_2}$=$V_{IH}$ Fixed), 8bits Output

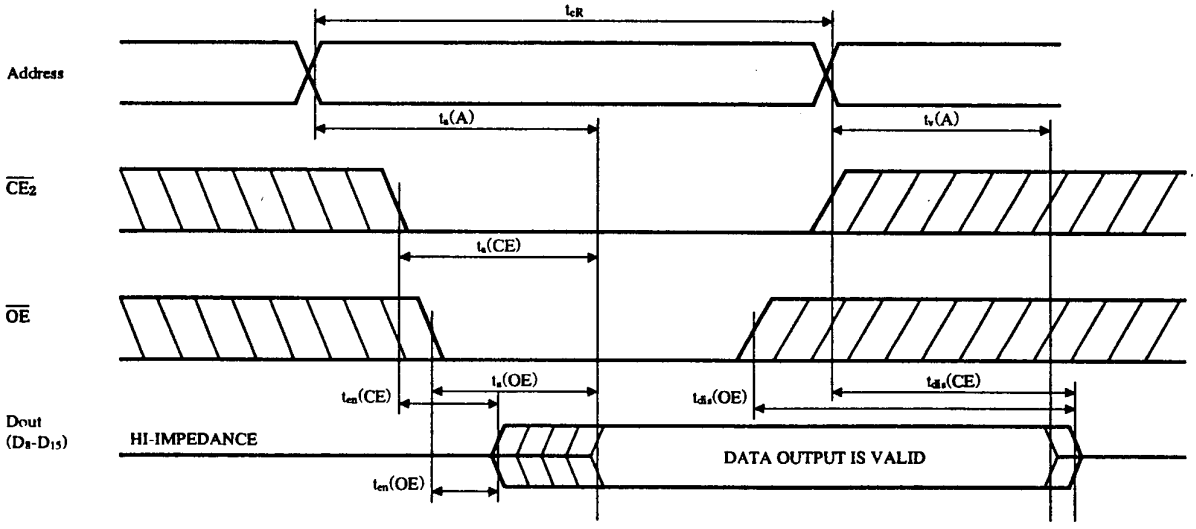



Note) 1. $\overline{WE}$="HIGH", during a read cycle.

2. Either "HIGH" or "LOW" in diagonal areas.

3. The output data becomes valid when last interval, $t_a$ (A), $t_a$ (CE) or $t_a$ (CE) have concluded.

○Read Cycle (2) ($\overline{CE_1}$=$V_{IH}$ Fixed), 8Bits Output

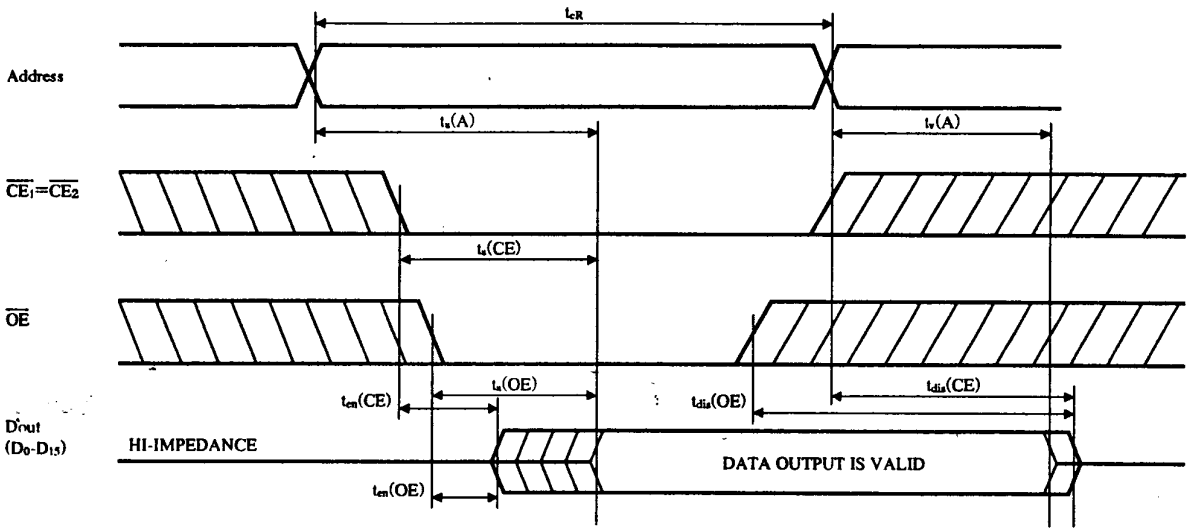



Note) 1. $\overline{WE}$="HIGH", during a read cycle.

2. Either "HIGH" or "LOW" in diagonal areas.

3. The output data becomes valid when last interval, $t_a$ (A), $t_a$ (CE) or $t_a$ (CE) have concluded.

○Read Cycle (3), 16Bits Output




Note) 1. $\overline{WE}$="HIGH", during a read cycle.

2. Either "HIGH" or "LOW" in diagonal areas.

3. Change $\overline{CE_1}$ and $\overline{CE_2}$ at the same time.

4. The output data becomes valid when last interval, $t_a$ (A), $t_a$ (CE) or $t_a$ (CE) have concluded.

## 10. Programming Operation

### 10.1 DC Characteristics

($V_{CC}$=4.5~5.5V, $V_{PP}$=11.4~12.6V, Ta=0~60℃)

| PARAMETER | | SYMBOL | Min. | Max. | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $V_{PP1}$, $V_{PP2}$ operating Voltage | Read | $V_{PPL}$ | 0 | 1.5 | V | |
| | Program | $V_{PPH}$ | 11.4 | 12.6 | | |
| $V_{PP1}$, $V_{PP2}$ operating Current (×16 Mode) | Read | $I_{SB2}$ | — | 1.6 | mA | Input open |
| | Program | $I_{PP}$ | — | 20 | | RMS |
| $V_{CC}$ operating Current | Standby | $I_{SB1}$ | — | 2 | | Input open |
| | Program | $I_{CC}$ | — | 75 | | RMS |
| Input Voltage | | $V_{IL}$ | −0.3 | 1.5 | V | |
| | | $V_{IH}$ | 3.5 | $V_{CC}$+0.3 | | |
| Output Voltage During Verify | | $V_{OL}$ | — | 0.4 | | $I_{OL}$=4mA |
| | | $V_{OH}$ | $V_{CC}$−0.5 | — | | $I_{OH}$=−2mA |

Note) 1. Power on $V_{CC}$ before power on $V_{CC}$, power off $V_{CC}$ after power off $V_{PP}$.

2. Keep $V_{PP}$ including its overshoot, below 13V.

3. Card insertion or removal while applying $V_{PP}$=12V may cause a loss of integrity.

4. Do not turn on or turn off during $\overline{CE}$="LOW".

5. If $V_{IH}$ goes above $V_{CC}$+0.3V, normal operation is not assured.

## 10.2 AC Characteristics ($V_{CC}$=4.5~5.5V, $V_{PP}$=11.4~12.6V, Ta=0~60℃)

Testing Conditions:

1) Input Pulse Level : 0.8~3.5V
2) Input Rise/Fall Time : 10ns
3) Input/Output Timing Reference Level : 1.5V
4) Output Load : 1TTL+$C_L$ (100pF) (including scope and jig capacitance)

### 10.2.1 Program Cycle

$\overline{WE}$ Controlled

($V_{CC}$=4.5~5.5V, $V_{PP}$=11.4~12.6V, Ta=0~60℃)

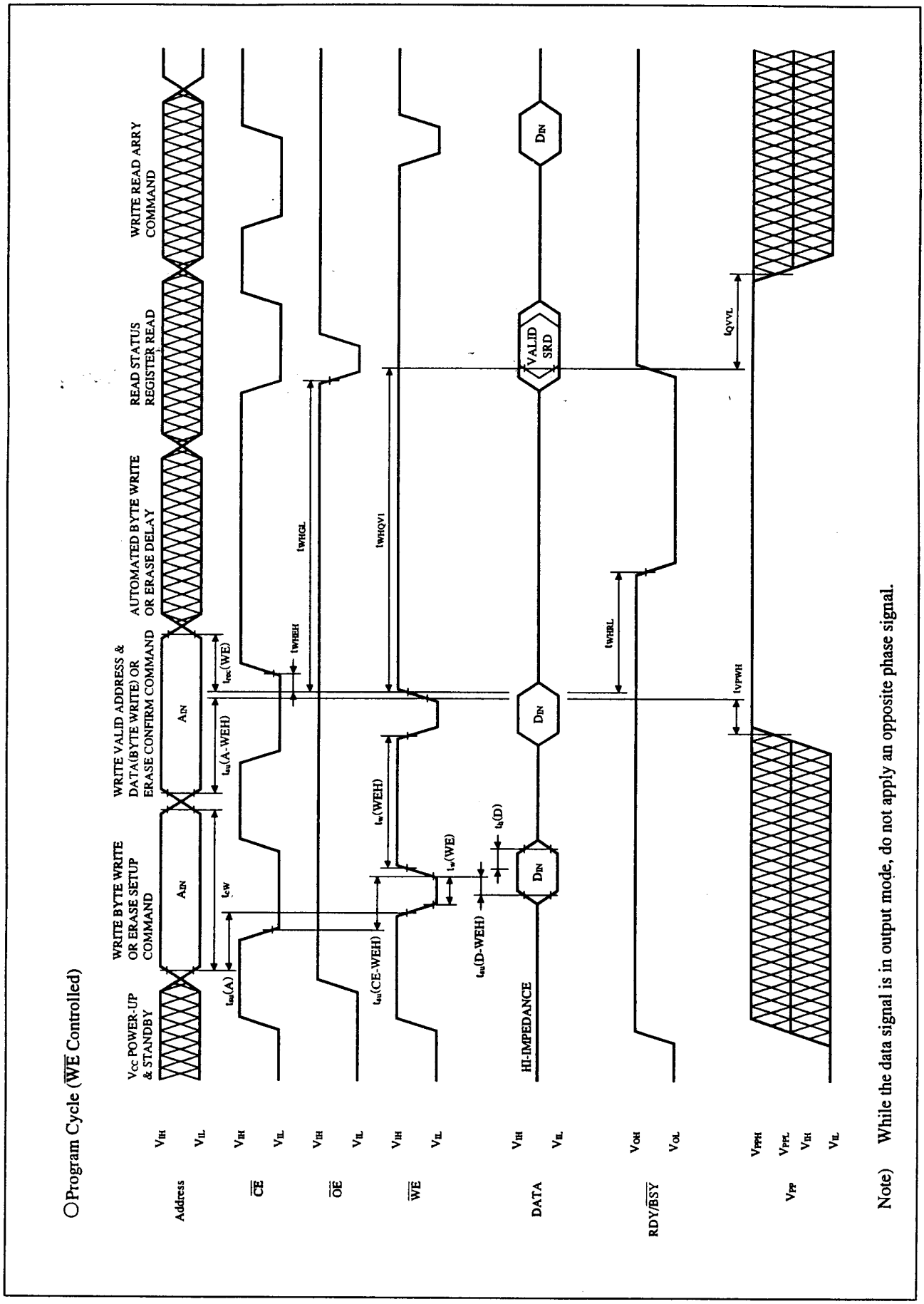
| PARAMETER | SYMBOL | SYMBOL (PCMCIA) | Min. | Max. | UNIT |
|---|---|---|---|---|---|
| Write Cycle Time | $t_{AVAV}$ | $t_{cW}$ | 200 | — | ns |
| Address Setup Time | $t_{AVWL}$ | $t_{su}$ (A) | 20 | — | |
| Write Recovery Time | $t_{WHAX}$ | $t_{rec}$ (WE) | 30 | — | |
| Data Setup Time for $\overline{WE}$ | $t_{DVWH}$ | $t_{su}$ (D-WEH) | 60 | — | |
| Data Hold Time | $t_{WHDX}$ | $t_h$ (D) | 30 | — | |
| Write Recovery Before Read | $t_{WHGL}$ | | 10 | — | |
| Card Enable Setup time for $\overline{WE}$ | $t_{ELWH}$ | $t_{su}$ (CE-WEH) | 140 | — | |
| Address Setup for $\overline{WE}$ | $t_{AVWH}$ | $t_{su}$ (A-WEH) | 140 | — | |
| Card Enable Hold Time | $t_{WHEH}$ | | 15 | — | |
| Write Pulse Width | $t_{WLWH}$ | $t_W$ (WE) | 120 | — | |
| Write Pulse Width High | $t_{WHWL}$ | $t_W$ (WEH) | 30 | — | |
| $\overline{WE}$ High to RDY/$\overline{BSY}$ Going Low | $t_{WHRL}$ | | — | 150 | |
| Duration of write operation | $t_{WHQV1}$ | | 4.8 | — | μs |
| $V_{PP}$ Setup to $\overline{WE}$ Going High | $t_{VPWH}$ | | 100 | — | ns |
| $V_{PP}$ Hold from Valid SRD, RDY/$\overline{BSY}$ High | $t_{QVVL}$ | | 0 | — | |

$\overline{CE}$ Controlled ($V_{CC}$=4.5~5.5V, $V_{PP}$=11.4~12.6V, Ta=0~60℃)

| PARAMETER | SYMBOL | SYMBOL (PCMCIA) | Min. | Max. | UNIT |
|---|---|---|---|---|---|
| Write Cycle Time | $t_{AVAV}$ | $t_{cW}$ | 200 | — | ns |
| Address Setup Time | $t_{AVEL}$ | $t_{su}$ (A) | 20 | — | |
| Write Recovery Time | $t_{EHAX}$ | $t_{rec}$ (CE) | 30 | — | |
| Data Setup Time for $\overline{CE}$ | $t_{DVEH}$ | $t_{su}$ (D-CEH) | 60 | — | |
| Data Hold Time | $t_{EHDX}$ | $t_h$ (D) | 30 | — | |
| Write Recovery Before Read | $t_{EHGL}$ | | 10 | — | |
| Write Enable Setup time for $\overline{CE}$ | $t_{WLEH}$ | $t_{su}$ (WE-CEH) | 140 | — | |
| Address Setup for $\overline{CE}$ | $t_{AVEH}$ | $t_{su}$ (A-CEH) | 140 | — | |
| Write Enable Hold Time | $t_{EHWH}$ | | 0 | — | |
| Write Pulse Width | $t_{ELEH}$ | $t_W$ (CE) | 120 | — | |
| Write Pulse Width High | $t_{EHEL}$ | $t_W$ (CEH) | 30 | — | |
| $\overline{WE}$ High to RDY/$\overline{BSY}$ Going Low | $t_{EHRL}$ | | — | 150 | |
| Duration of write operation | $t_{EHQV1}$ | | 4.8 | — | μs |
| $V_{PP}$ Setup to $\overline{WE}$ Going High | $t_{VPEH}$ | | 100 | — | ns |
| $V_{PP}$ Hold from Valid SRD, RDY/$\overline{BSY}$ High | $t_{QVVL}$ | | 0 | — | |

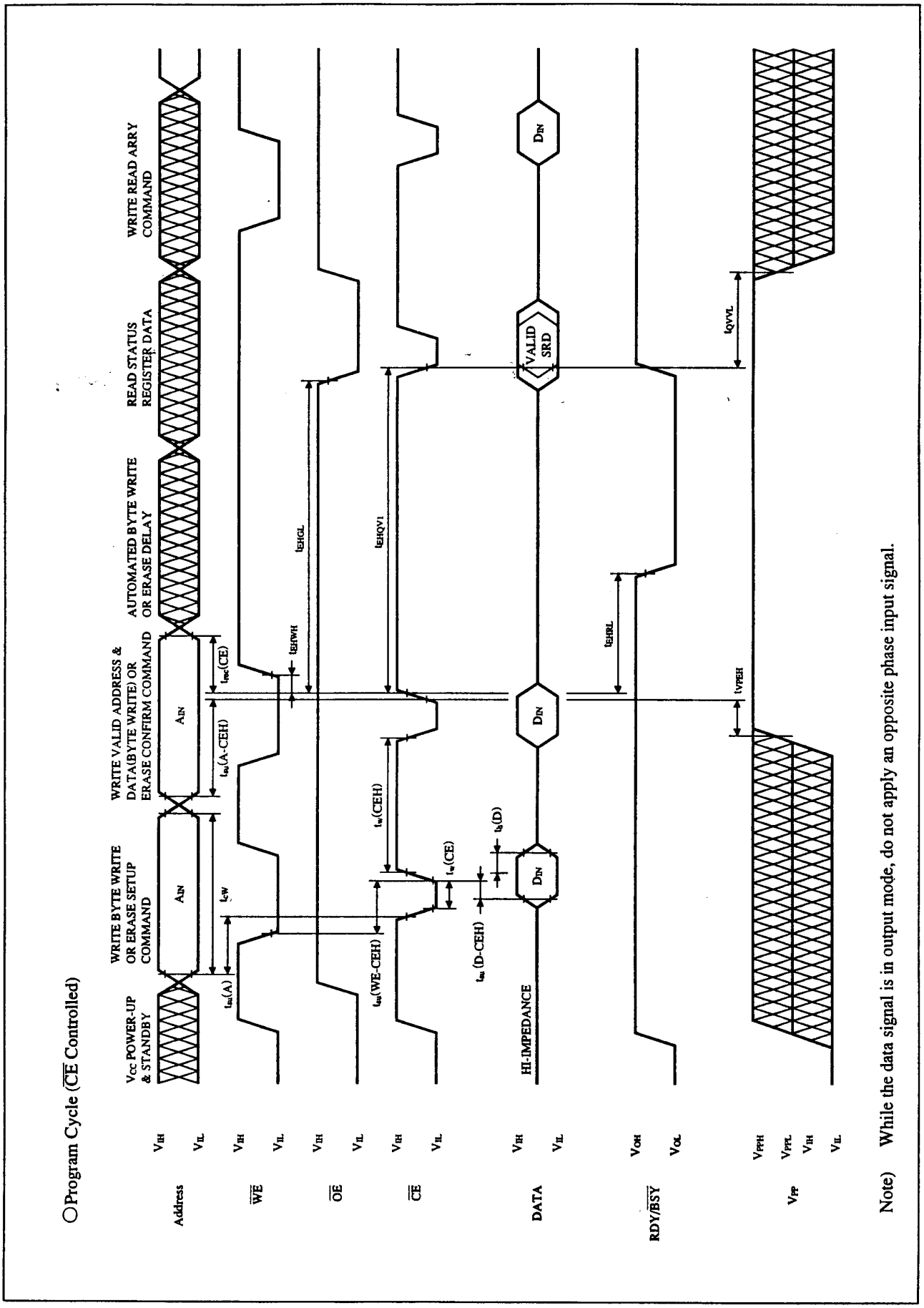
1. Set $\overline{CE_1}$, $\overline{CE_2}$, $\overline{OE}$ and $\overline{WE}$ "HIGH", when $V_{PP}$ changes from $V_{PPL}$ to $V_{PPH}$ or vice versa.

○Program Cycle ($\overline{WE}$ Controlled)




Note) While the data signal is in output mode, do not apply an opposite phase signal.

○Program Cycle ($\overline{CE}$ Controlled)




Note) While the data signal is in output mode, do not apply an opposite phase input signal.

# 11. Erase Operation

## 11.1 DC Charactristics

($V_{CC}$=4.5~5.5V, $V_{PP}$=11.4~12.6V, Ta=0~60℃)

| PARAMETER | | SYMBOL | Min. | Max. | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $V_{PP1}$, $V_{PP2}$ Operating Voltage | Read | $V_{PPL}$ | 0 | 1.5 | V | |
| | Program | $V_{PPHE}$ | 11.4 | 12.6 | | |
| $V_{PP1}$, $V_{PP2}$ Operating Current (×16 Mode) | Standby | $I_{SB2}$ | — | 1.6 | mA | I/O open |
| | Erase | $I_{PP}$ | — | 20 | | RMS |
| | Erase Suspend | $I_{PPS}$ | — | 1.6 | | $\overline{CE_1}$, $\overline{CE_2}$=$V_{IH}$, RMS |
| $V_{CC}$ Operating Current (×16 Mode) | Standby | $I_{SB1}$ | — | 2.0 | | I/O open |
| | Erase | $I_{CCE}$ | — | 75 | V | RMS |
| | Erase Suspend | $I_{CCES}$ | −0.3 | 22 | | $\overline{CE_1}$, $\overline{CE_2}$=$V_{IH}$, RMS |
| Input Voltage | | $V_{IL}$ | 3.5 | 1.5 | | |
| | | $V_{IH}$ | — | $V_{CC}$+0.3 | | |
| Output Voltage During Verify | | $V_{OL}$ | $V_{CC}$−0.5 | 0.4 | | $I_{OL}$=4mA |
| | | $V_{OH}$ | | — | | $I_{OH}$=−2mA |

Note) Power on $V_{CC}$ before power on $V_{PP}$, power off $V_{CC}$ after power off $V_{PP}$. Keep $V_{PP}$ including its overshoot, below 13V. Card insertion or removal while applying $V_{PP}$=12V may cause a loss of integrity. Do not turn on or turn off during $\overline{CE}$= "LOW".
If $V_{IH}$ goes above $V_{CC}$+0.3V, normal operation is not assured.

## 11.2 AC Characteristics ($V_{CC}$=4.5~5.5V, $V_{PP}$=11.4~12.6V, Ta=0~60℃)

Testing Conditions:

1) Input Pulse Level : 0.8~3.5V
2) Input Rise/Fall Time : 10ns
3) Input/Output Timing Reference Level : 1.5V
4) Output Load : 1TTL+$C_L$ (100pF) (including scope and jig capacitance)

### 11.2.1 Erase Cycle

$\overline{WE}$ Controlled ($V_{CC}$=4.5~5.5V, $V_{PP}$=11.4~12.6V, Ta=0~60℃)

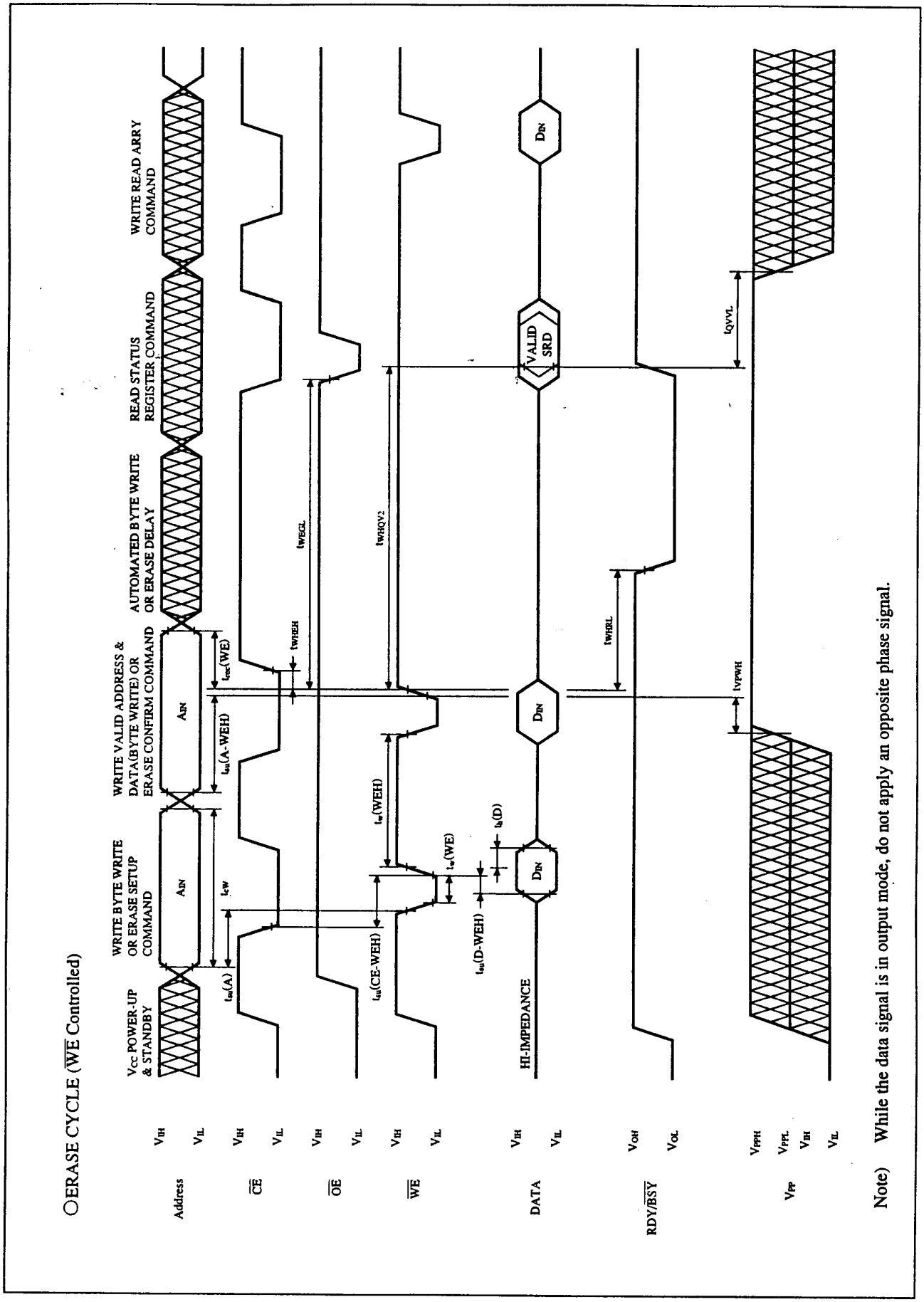
| PARAMETER | SYMBOL | SYMBOL (PCMCIA) | Min. | Max. | UNIT |
|---|---|---|---|---|---|
| Write Cycle Time | $t_{AVAV}$ | $t_{cW}$ | 200 | — | ns |
| Address Setup Time | $t_{AVWL}$ | $t_{su}$ (A) | 20 | — | |
| Write Recovery Time | $t_{WHAX}$ | $t_{rec}$ (WE) | 30 | — | |
| Data Setup Time for $\overline{WE}$ | $t_{DVWH}$ | $t_{su}$ (D-WEH) | 60 | — | |
| Data Hold Time | $t_{WHDX}$ | $t_h$ (D) | 30 | — | |
| Write Recovery Before Read | $t_{WHGL}$ | | 10 | — | |
| Card Enable Setup time for $\overline{WE}$ | $t_{ELWH}$ | $t_{su}$ (CE-WEH) | 140 | — | |
| Address Setup for $\overline{WE}$ | $t_{AVWH}$ | $t_{su}$ (A-WEH) | 140 | — | |
| Card Enable Hold Time | $t_{WHEH}$ | | 15 | — | |
| Write Pulse Width | $t_{WLWH}$ | $t_W$ (WE) | 120 | — | |
| Write Pulse Width High | $t_{WHWL}$ | $t_W$ (WEH) | 30 | — | |
| $\overline{WE}$ High to RDY/$\overline{BSY}$ Going Low | $t_{WHRL}$ | | — | 150 | |
| Duration of Erase operation | $t_{WHQV2}$ | | 0.3 | — | s |
| $V_{PP}$ Setup to $\overline{WE}$ Going High | $t_{VPWH}$ | | 100 | — | ns |
| $V_{PP}$ Hold from Valid SRD, RDY/$\overline{BSY}$ High | $t_{QVVL}$ | | 0 | — | |

$\overline{CE}$ Contorolled ($V_{CC}$=4.5~5.5V, $V_{PP}$=11.4~12.6V, Ta=0~60°C)

| PARAMETER | SYMBOL | SYMBOL (JEIDA) | Min. | Max. | UNIT |
|---|---|---|---|---|---|
| Write Cycle Time | $t_{AVAV}$ | $t_{cW}$ | 200 | — | ns |
| Address Setup Time | $t_{AVEL}$ | $t_{su}$ (A) | 20 | — | |
| Write Recovery Time | $t_{EHAX}$ | $t_{rec}$ (CE) | 30 | — | |
| Data Setup Time for $\overline{CE}$ | $t_{DVEH}$ | $t_{su}$ (D-CEH) | 60 | — | |
| Data Hold Time | $t_{EHDX}$ | $t_h$ (D) | 30 | — | |
| Write Recovery Before Read | $t_{EHGL}$ | | 10 | — | |
| Write Enable Setup time for $\overline{CE}$ | $t_{WLEH}$ | $t_{su}$ (WE-CEH) | 140 | — | |
| Address Setup for $\overline{CE}$ | $t_{AVEH}$ | $t_{su}$ (A-CEH) | 140 | — | |
| Write Enable Hold Time | $t_{EHWH}$ | | 0 | — | |
| Write Pulse Width | $t_{ELEH}$ | $t_W$ (CE) | 120 | — | |
| Write Pulse Width High | $t_{EHEL}$ | $t_W$ (CEH) | 30 | — | |
| $\overline{WE}$ High to RDY/$\overline{BSY}$ Going Low | $t_{EHRL}$ | | — | 150 | |
| Duration of Erase operation | $t_{EHQV2}$ | | 0.3 | — | s |
| $V_{PP}$ Setup to $\overline{WE}$ Going High | $t_{VPEH}$ | | 100 | — | ns |
| $V_{PP}$ Hold from Valid SRD, RDY/$\overline{BSY}$ High | $t_{QVVL}$ | | 0 | — | |

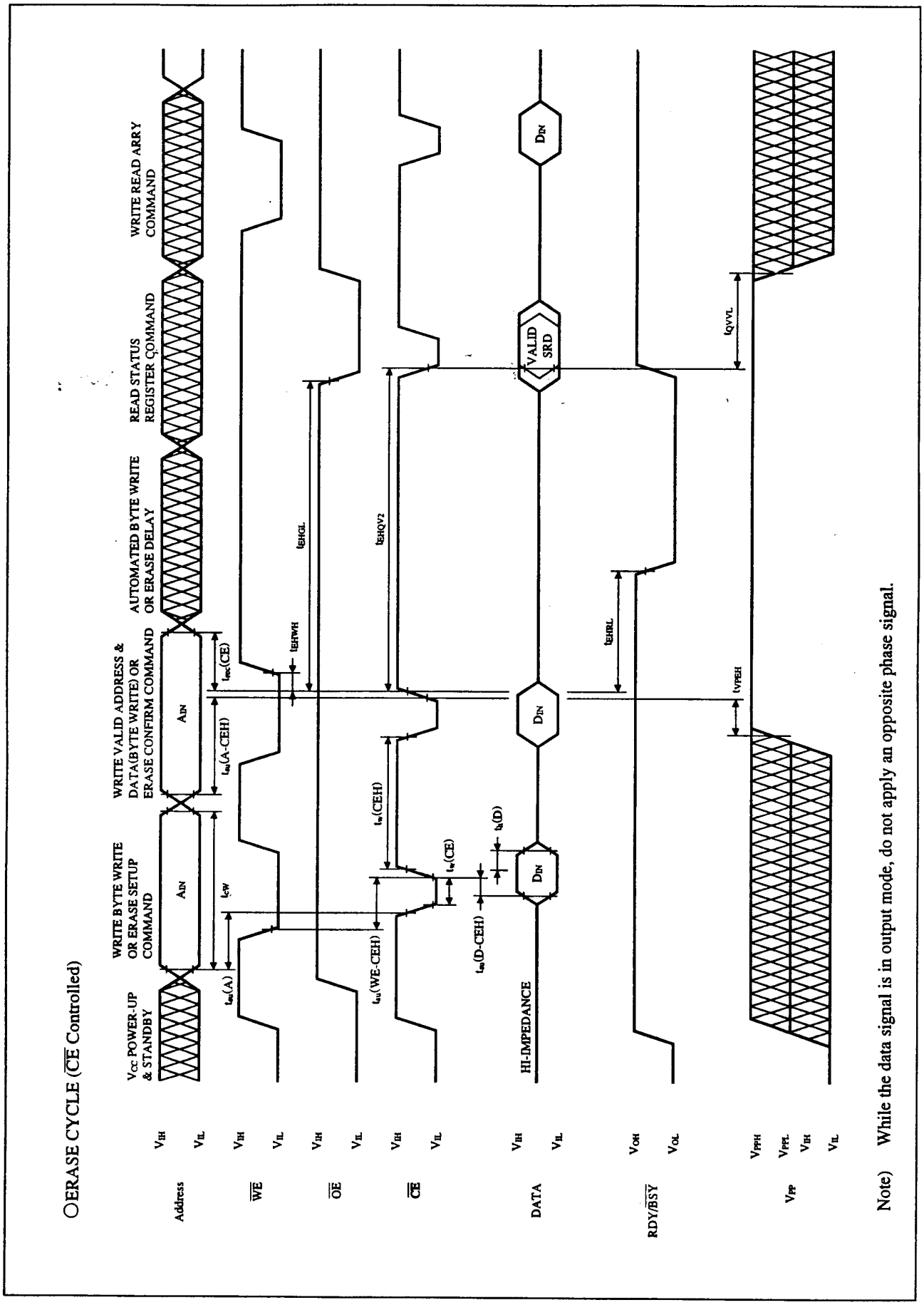
1. Set $\overline{CE_1}$, $\overline{CE_2}$, $\overline{OE}$ and $\overline{WE}$ "HIGH", when $V_{PP}$ changes from $V_{PPL}$ to $V_{PPH}$ or vice versa.

○ERASE CYCLE ($\overline{WE}$ Controlled)




Note) While the data signal is in output mode, do not apply an opposite phase signal.

○ERASE CYCLE ($\overline{CE}$ Controlled)



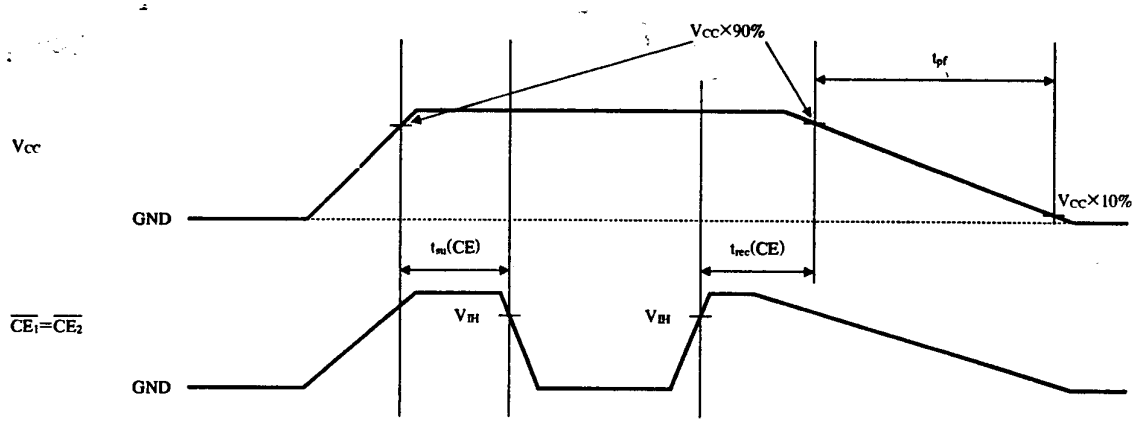

Note) While the data signal is in output mode, do not apply an opposite phase signal.

## 12. Block Erase and Data Write Characteristics

($V_{CC}$=4.5~5.5V, $V_{PP}$=11.4~12.6V, Ta=0~60℃)

| PARAMETER | | Min. | Typ. | Max. | UNIT |
|---|---|---|---|---|---|
| Block Pair Erase Time | | — | 1.0 | 10 | s |
| Block Pair Write Time | | — | 0.4 | 2.1 | |

## 13. Voltage Timing (Ta=25℃)




3.5V < $V_{IH}$ < $V_{CC}$+0.3

| PARAMETER | SYMBOL | Min. | Max. | UNIT |
|---|---|---|---|---|
| $\overline{CE}$ Setup Time | $t_{su}$ (CE) | 4.0 | — | ms |
| $\overline{CE}$ Recovery Time | $t_{rec}$ (CE) | 1.0 | — | μs |
| $V_{CC}$ Falling Time | $t_{pf}$ | 3.0 | 300 | ms |

Note) 1. When $V_{CC}$ (4.5~5.5V) is applied to the memory card and you are inserting or removing the card, $\overline{CE_1}$, $\overline{CE_2}$ should both be high-impedance. At such a time, other signal line should also be hi-impedance. After inserting the memory card, do not access it during the $\overline{CE}$ setup time (minimum of 4ms).
(During this time, neither $\overline{CE_1}$ nor $\overline{CE_2}$= "LOW".)

2. When $V_{CC}$ is turn on, if the condition (for example, $V_{CC}$ rising time. etc) is not sufficient to as specified, it is possible that device's Status Register is not cleared or device not becomes to Read Array Mode. To prevent these, it is recommended that using software command, reset the Status Register or set the device to Read Array Mode.

ex.

Reset the Status Register 50H (5050H)
Set to Read Array Mode FFH (FFFFH)

## 14. Attribute Memory

The attribute memory holds the attribute information of the card such as the type of card, bit configuration, speed and so on.

EEPROM Model

Card has 2k bytes of EEPROM attribute memory. To read the attribute memory, set $\overline{REG}$="LOW" and perform a read with the same access timming as common memory read.

For this operation, access time is 300ns maximum. To allow 2k bytes of attribute memory, even addresses from 0 to 4096 are reserved. Since only the even-numbered bytes are used, reading odd-numbered bytes will result in invalid data.

Note) We have another type of attribute memory as follows,

No EEPROM Model. (Model no.ID240E02:5 bytes device informations in even address 0 to 8 , read only in card's control circuit,with the same access timming as common memory read.)

### 14.1 Attribute Memory Read/Write Function Chart

| $\overline{CE_1}$ | $\overline{CE_2}$ | $A_0$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{REG}$ | MODE | $D_0$~$D_7$ | $D_8$~$D_{15}$ | STAATUS |
|---|---|---|---|---|---|---|---|---|---|
| H | H | X | X | X | X | | High-Z | High-Z | Standby |
| L | H | L | H | L | L | Read (×8) | $D_0$ (even byte) | High-Z | Byte Access |
| L | H | H | H | L | L | | High-Z | High-Z | Standby |
| L | L | X | H | L | L | Read (×8) | $D_0$ (even byte) | High-Z | Byte Access |
| H | L | X | H | L | L | | High-Z | High-Z | Standby |
| L | H | L | L | H | L | Write (×8) | $D_1$ (even byte) | ××× | Byte Access |
| L | H | H | L | H | L | | ××× | ××× | Standby |
| L | L | X | L | H | L | Write (×8) | $D_1$ (even byte) | ××× | Byte Access |
| H | L | X | L | H | L | | ××× | ××× | Standby |
| L | X | X | H | L | L | Attribute Memory Address 0~8 | $D_0$ | High-Z | Byte Access |

H : High L : Low X : High/Low not applicable

Di : Input Data Do : Output Data Hi-Z : High Impedance ××× : Don't Care

Notes : 1) When the write protect switch is in protect-mode, the WP output signal is "HIGH" and write operations (including attribute memory) are not allowed.

2) $A_0$-$A_{11}$ are attribute memory address. Addresses after $A_{12}$ are not decoded, so care should be taken.

### 14.2 AC Characteristics ($V_{CC}$=4.5V~5.5V, Ta=0~60℃)

Testing Conditions

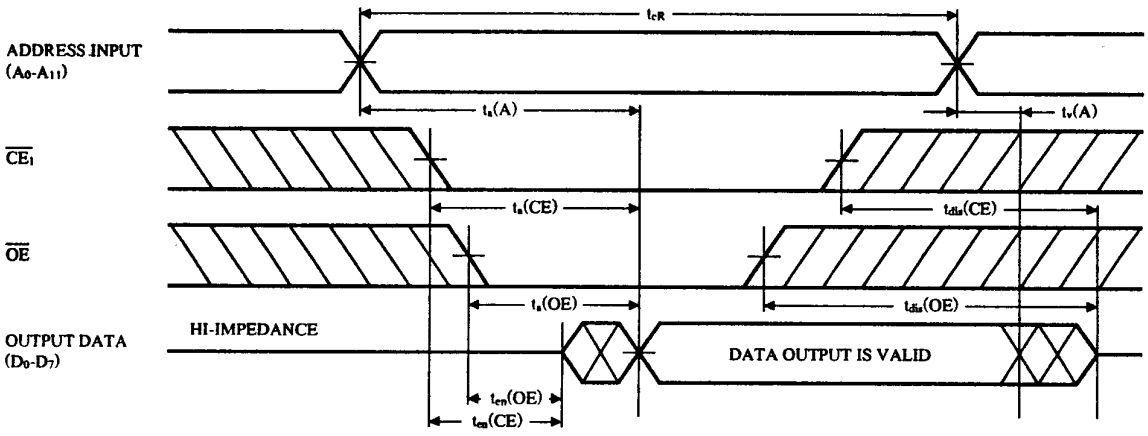
1) Input Pulse Level : 0.8~3.5V
2) Input Rise/Fall Time : 10ns
3) Input/Output Timing Reference Level : 1.5V
4) Output Load Capacitance : 1TTL+$C_L$ (100pF)
   (including scope and jig capacitance)

## 14.3 Attribute Memory Read Cycle

($V_{CC}$=4.5~5.5V, Ta=0~60℃)

| PARAMETER | SYMBOL | SYMBOL (PCMCIA) | Min. | Max. | UNIT |
|---|---|---|---|---|---|
| Read Cycle Time | $t_{CR}$ | $t_{cR}$ | 300 | — | ns |
| Address Access Time | $t_{ACC}$ | $t_a$ (A) | — | 300 | |
| Card Enable Access Time | $t_{CE}$ | $t_a$ (CE) | — | 300 | |
| Output Enable Access Time | $t_{OE}$ | $t_a$ (OE) | — | 150 | |
| Output Disable Time from $\overline{CE}$ | | $t_{dis}$ (CE) | — | 100 | |
| Output Disable Time from $\overline{OE}$ | $t_{DF}$ | $t_{dis}$ (OE) | — | 100 | |
| Output Enable Time from $\overline{CE}$ | | $t_{en}$ (CE) | 5 | — | |
| Output Enable Time from $\overline{OE}$ | | $t_{en}$ (OE) | 5 | — | |
| Data Valid from Add Change | $t_{OH}$ | $t_v$ (A) | 0 | — | |

○Attribute Memory Read Cycle




Note: 1. To read attribute memory, $\overline{REG}$="LOW", $\overline{WE}$="HIGH" and either $\overline{CE_2}$="LOW" or else $\overline{CE_2}$="HIGH" and $A_0$="LOW".

2. The output data becomes valid when last interval, $t_a$ (A), $t_a$ (CE)or $t_a$ (OE)have concluded.

## 14.4 Attribute Memory Write Cycle

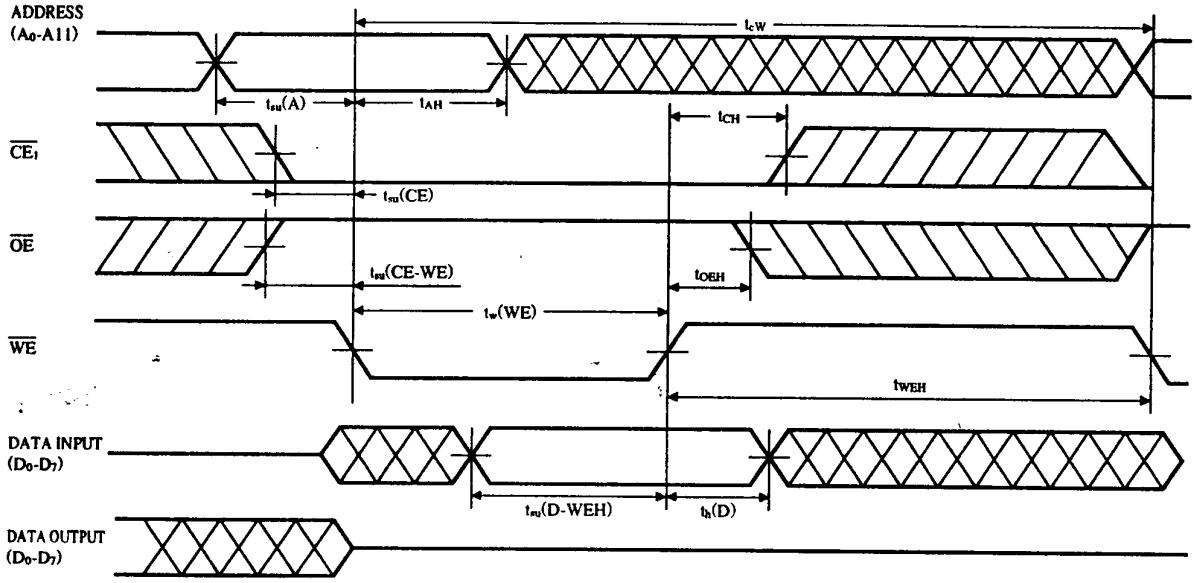
$\overline{WE}$ Controlled ($V_{CC}$=4.5V~5.5V, Ta=0~60℃)

| PARAMETER | SYMBOL | SYMBOL (PCMCIA) | Min. | Max. | UNIT |
|---|---|---|---|---|---|
| Write Cycle Time | $t_{WC}$ | $t_{cW}$ | 10 | — | ms |
| Write Pulse Width | $t_{WP}$ | $t_w$ (WE) | 180 | — | ns |
| Address Setup Time | $t_{AS}$ | $t_{su}$ (A) | 10 | — | |
| Data Setup Time for $\overline{WE}$ | $t_{DS}$ | $t_{su}$ (D-WEH) | 100 | — | |
| Card Enable Setup Time | $t_{CES}$ | $t_{su}$ (CE) | 0 | — | |
| Output Enable Setup Time | $t_{OES}$ | $t_{su}$ (OE-WE) | 45 | — | |
| Address Hold Time | $t_{AH}$ | | 260 | — | |
| Write Hold Time | $t_{CH}$ | | 0 | — | |
| Output Enable Hold Time | $t_{OEH}$ | | 70 | — | |
| $\overline{WE}$ HIGH Hold Time | $t_{WEH}$ | | 9.9 | — | ms |
| Data Hold Time | $t_{DH}$ | $t_h$ (D) | 80 | — | ns |

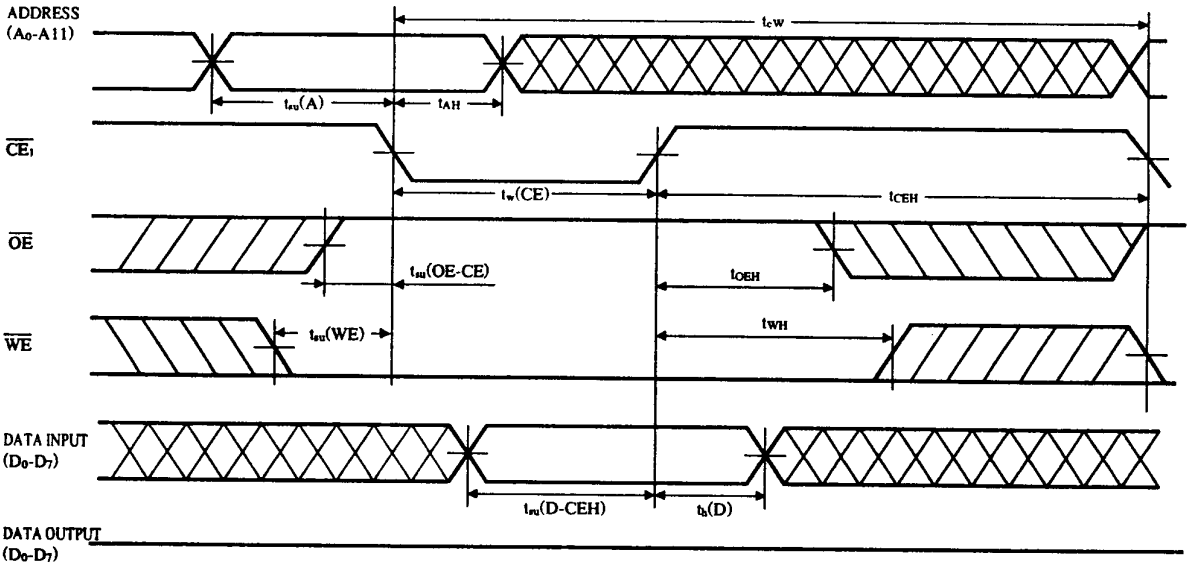
$\overline{CE}$ Controlled ($V_{CC}$=4.5V~5.5V, Ta=0~60℃)

| PARAMETER | SYMBOL | SYMBOL (PCMCIA) | Min. | Max. | UNIT |
|---|---|---|---|---|---|
| Write Cycle Time | $t_{WC}$ | $t_{cW}$ | 10 | — | ms |
| Write Pulse Width | $t_{WP}$ | $t_w$ (CE) | 210 | — | ns |
| Address Setup Time | $t_{AS}$ | $t_{su}$ (A) | 10 | — | |
| Data Setup Time for $\overline{CE}$ | $t_{DS}$ | $t_{su}$ (D-CEH) | 100 | — | |
| Write Enable Setup Time | $t_{WES}$ | $t_{su}$ (WE) | 0 | — | |
| Output Enable Setup Time | $t_{OES}$ | $t_{su}$ (OE-CE) | 45 | — | |
| Address Hold Time | $t_{AH}$ | | 260 | — | |
| Write Hold Time | $t_{WH}$ | | 0 | — | |
| Output Enable Hold Time | $t_{OEH}$ | | 70 | — | |
| $\overline{CE}$ HIGH Hold Time | $t_{CEH}$ | | 9.9 | — | ms |
| Data Hold Time | $t_{DH}$ | $t_h$ (D) | 80 | — | ns |

○Attribute Memory Write Cycle ($\overline{WE}$ Controlled)




○Attribute Memory Write Cycle ($\overline{CE}$ Controlled)




Note: 1. To write attribute memory, $\overline{REG}$ = "LOW" and either $\overline{CE_2}$ = "LOW" or else $\overline{CE_2}$ = "HIGH" and $A_0$ = "LOW"

## 15. Specification Changes

Specifications may be changed upon discussion and agreement between both parties.

## 16. Othes Precautions

- Permanent damage occures if the memory card is stressed beyond Absolute Maximum Ratings. Operation beyond the Recommended Operating Conditions is not recommended and extended exposure beyond the Recommended Operating Conditions may affect device reliability.
- Writing to the memory card can be prevented by switching on the write protect switch on the end of the memory card.
- Avoid allowing the memory card connectors to come in contact with metals and avoid touching the connectors, as the internal circuits can be damaged by static electricity.
- Avoid storing in direct sunlight, high temperatures (do not place near heaters or radiators), high humidity and dusty areas.
- Avoid subjecting the memory card to strong physical abuse. Dropping, bending, smashing or throwing the card can result in loss of function.
- When the memory card is not being used, return it to its protective case.
- Do not allow the memory card to come in contact with fire.

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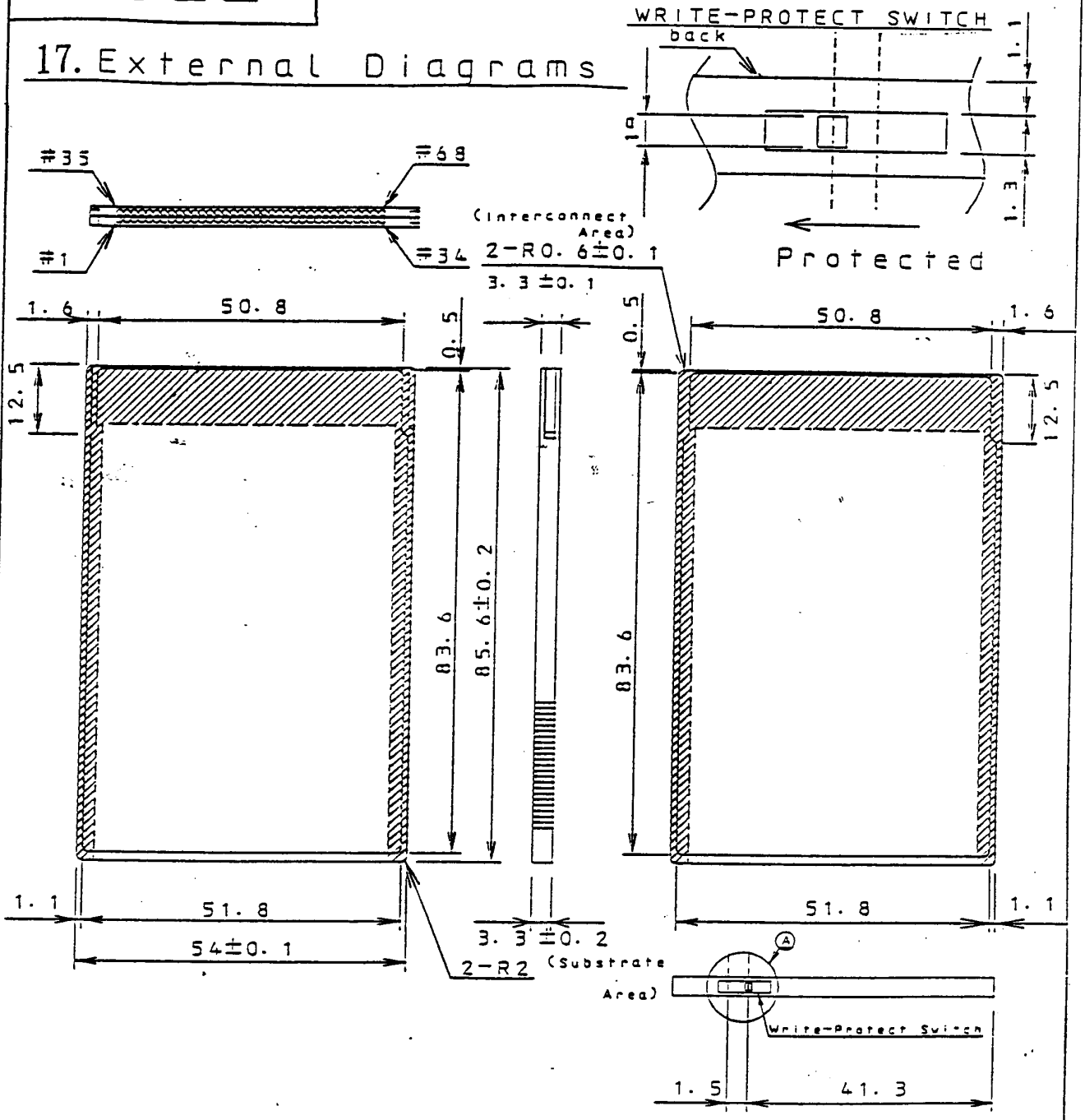
# 17. External Diagrams




| | | | | | | |
|---|---|---|---|---|---|---|
| APPLICABLE MODEL | | SCALE 1/1 | UNIT mm | CH. DATE | REVISE | CHANGE |
| THICKNESS | | MATERIAL | FINISH | NAME | MEMORY CARD EXTERNAL DIAGRAM | |
| DATE | 1994.11.15 | | | | PCMCIA Rel. 2.0 TYPE1 | |
| DESIGN / DRAW / TRACE / CHECK / APPROVE | Memory Card Business Project Team | | | | | |
| | TENRI IC GROUP SHARP CORPORATION | | | DRAWING NO. | IMC001-A102 | |

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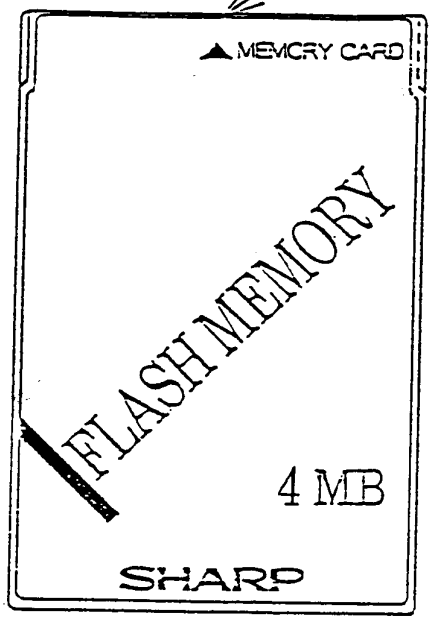
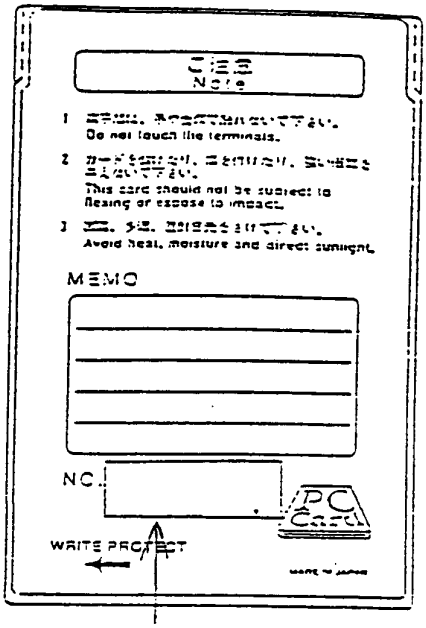
# 19. EXTERNAL APPEARANCES

CONNECTOR SIDE



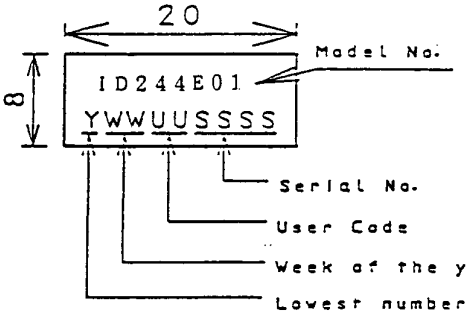

FRONT PANEL




LABELING POSITION

BACK PANEL

LABEL SIZE AND DENOTATIONS




| | | | | | | |
|---|---|---|---|---|---|---|
| APPLICABLE MODEL | ID244E01 | SCALE | UNIT mm | A2 / A | | |
| | | | | CH. DATE | REVISE | CHARGE |
| THICKNESS | DEFFERENCE | MATERIAL | FINISH | NAME | | |
| DATE 1995. 10. 10 | | | | | | |
| K. Hashizume / S. Sasaki | S. Shintani | MEMORY CARD BUSINESS PROJECT TEAM | | | | |
| | | INTEGRATED CIRCUITS GROUP | | | | |
| | | SHARP CORPORATION | | DRAWING NO. | | |

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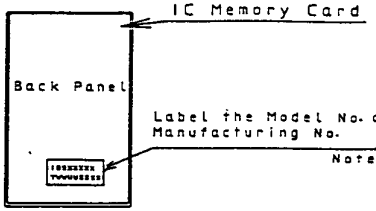
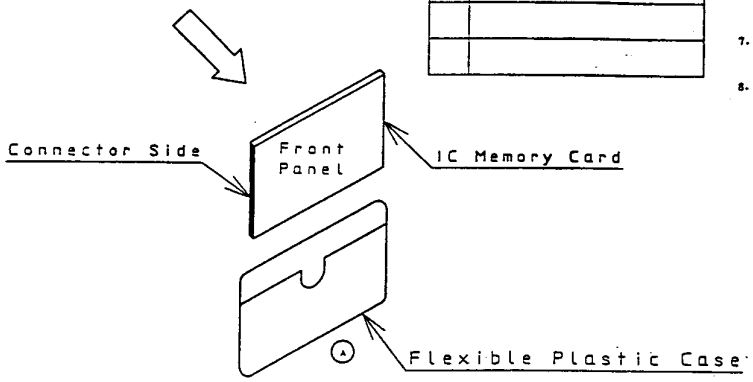
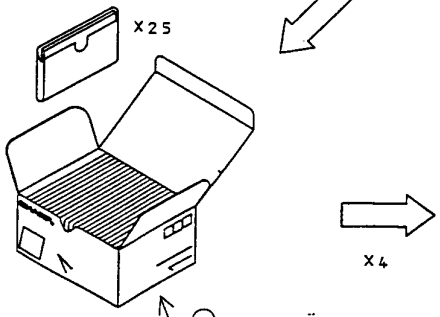
# 18. PACKING SPECIFICATION

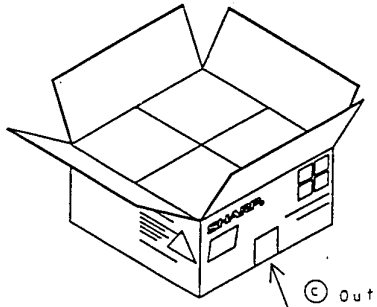
Connector Side



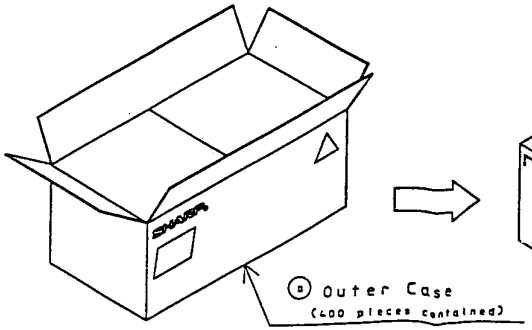



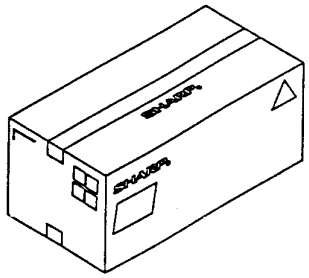




X4




X4



Parts List

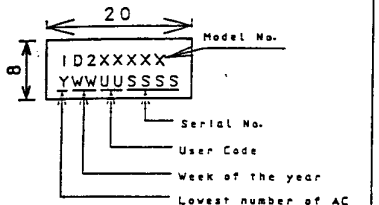
| | Parts Name |
|---|---|
| A | Flexible Plastic Case |
| B | Inner Carton (25 pieces contained) |
| C | Outer Carton (100 pieces contained) |
| D | Outer Case (400 pieces contained) |
| | |
| | |
| | |
| | |
| | |

## Packing Specification

1. Label the Model No. and Manufuring No. on the back panel of the card.
2. Each memory card is contained in the flexible plastic case. (The front side of the card comes to the place where the card is released, and the connector side is placed against to this point, so that the connector is not touched by finger, as shown in the figure.)
3. The inner carton contains 25 pieces of the card with the case. (Note 1.)
4. The product name, Lot no. (product no.), quantity and the date are either written directly on the inner carton or printed on the label which is then attached on inner carton.
5. The outer carton contains 4 inner cartons. (Note 2.)
6. The product name, Lot no. (product no.), quantity and the date are either written directly on the outer carton or printed on the label which is then attached on the outer carton.
7. The outer carton is then put in the outer case, which contains 4 outer cartons. (Note 3.)
8. The product name, Lot no. (product no.), quantity and the date are either written directly on the case or printed on the label which is then attached on the case.

Note 1. The least packing unit is 25 pieces, which is the number contained in the inner carton.

2. The space inside the outer carton is filled card board.
3. The other size of outer case may be used if there is not enough quantity to fill the normal outer case which can contain 4 outer cartons.
4. Size of label and denotations are following. [unit:mm]




| | | | | | | |
|---|---|---|---|---|---|---|
| APPLICABLE MODEL | ID2XXXXX | SCALE | UNIT mm | A | | |
| | | | | A | | |
| THICKNESS | DEFFERENCE | MATERIAL | FINISH | CH. DATE | REVISE | CHARGE |
| | | | | NAME | ID2XXXXX Packing Specification | |
| DATE | 1995. 10. 10 | | | | | |
| | | MEMORY CARD BUSINESS PROJECT TEAM INTEGRATED CIRCUITS GROUP SHARP CORPORATION | | DRAWING NO. | IMC025-J300 | |

4 MB, PCMCIA, Flash Card, ID240E01

**SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.**

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