Data Sheet No. PD60241
PRELIMINARY DATASHEET

International
IOR Rectifier

IRS2106(4)D(S)PbF

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs
- Integrated bootstrap diode

Packages


8-Lead SOIC


8-Lead PDIP


14-Lead SOIC


14-Lead PDIP

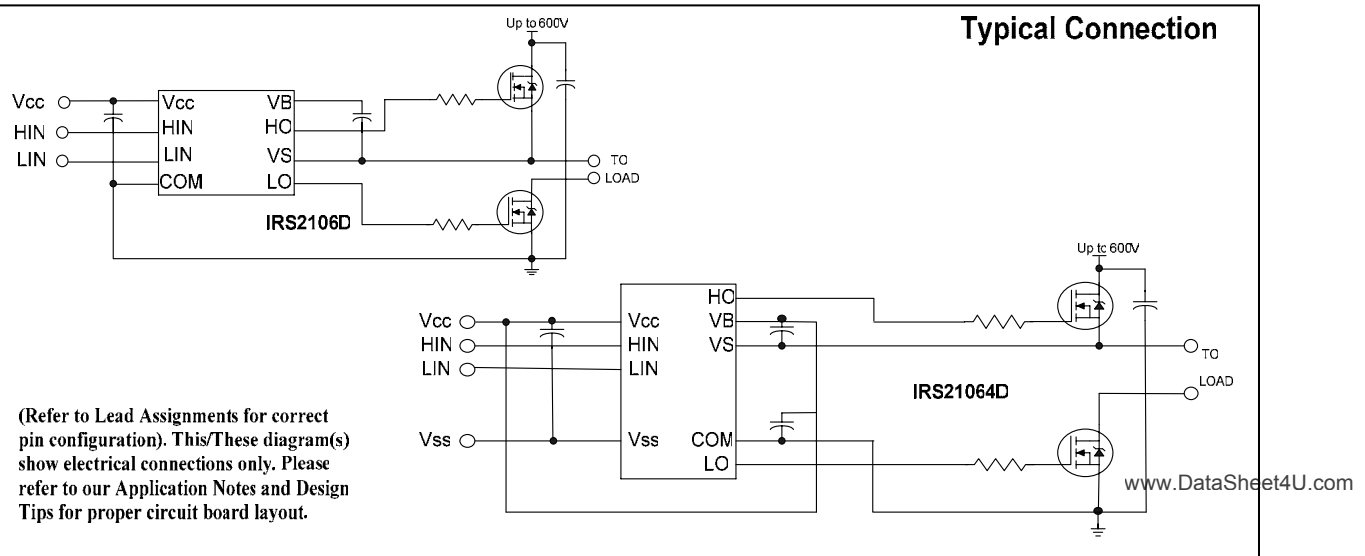
Description

The IRS2106(4)D(S) are high voltage, high speed power MOSFET an 1GBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with Standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or 1GBT in the high side configuration which operates up to 600 volts.

IRS2106D/IRS2108D/IRS2109D/Feature Comparison

Part	Input Logic	Cross-Conduction Prevention logic	Dead-Time	Ground Pins	Ton/Toff
2106	HIN/LIN	no	none	COM	515/500
21064				VSS/COM	
2108	HIN/$\overline{\text{LIN}}$	yes	Internal 540ns	COM	220/220
21084			Programmable 0.54- 5us	VSS/COM	
2109	IN/$\overline{\text{SD}}$	yes	Internal 540ns	COM	750/220
21094			Programmable 0.54- 5us	VSS/COM	

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	620	V
V_S	High side floating supply offset voltage		V_B - 20	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	20	
V_{SS}	Logic ground (IRS21064D only)		V_{CC} - 20	V_{CC} + 0.3	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage		V_{SS} -0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ TA ≤ +25°C	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.6	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S & V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S +10	V_S +20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	V_{SS}	V_{SS} + 5	
V_{SS}	Logic ground (IRS21064D only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to – V_{BS}. (Please refer to the Design Tip DT97 -3 for more details).
Note 2: HIN, LIN are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C

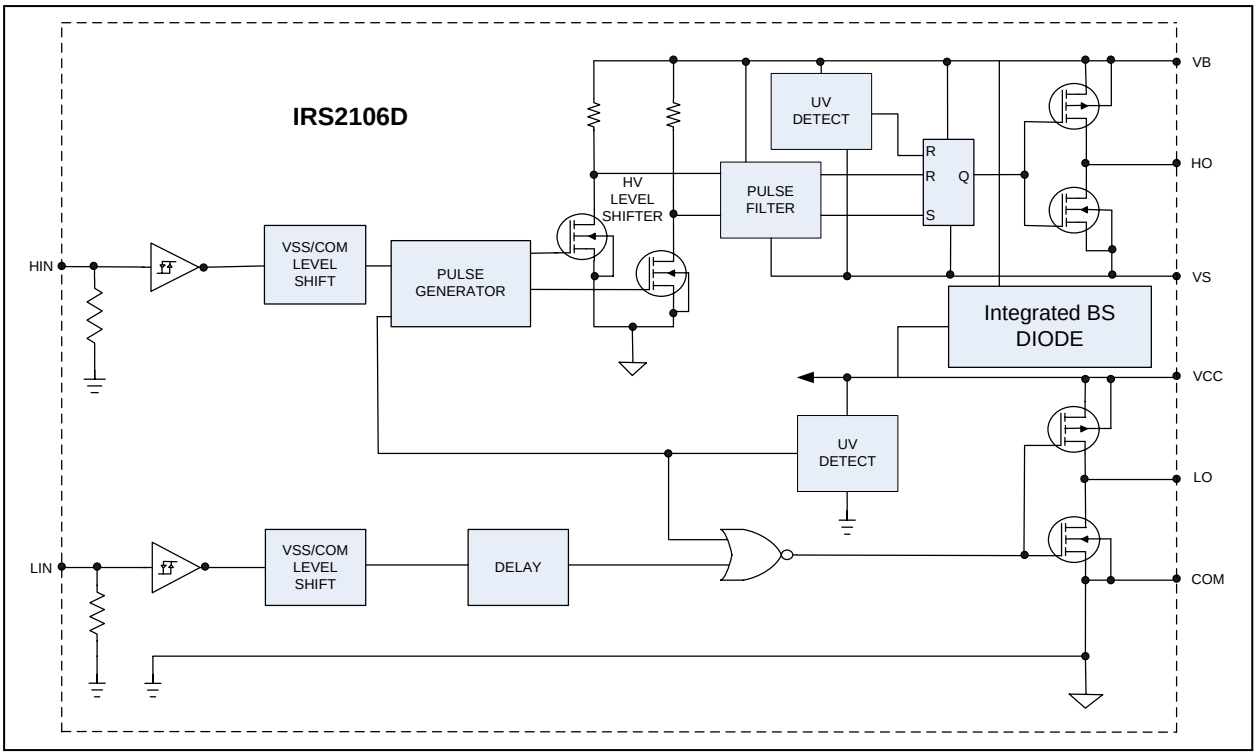
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	515	715	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	500	700		V_S = 0V or 600V
MT	Delay matching, HS & LS turn-on/off	—	—	30		
t_r	Turn-on rise time	—	150	220		V_S = 0V
t_f	Turn-off fall time	—	50	80		V_S = 0V
t_{fil}	Minimum pulse input filter time	—	300	—		

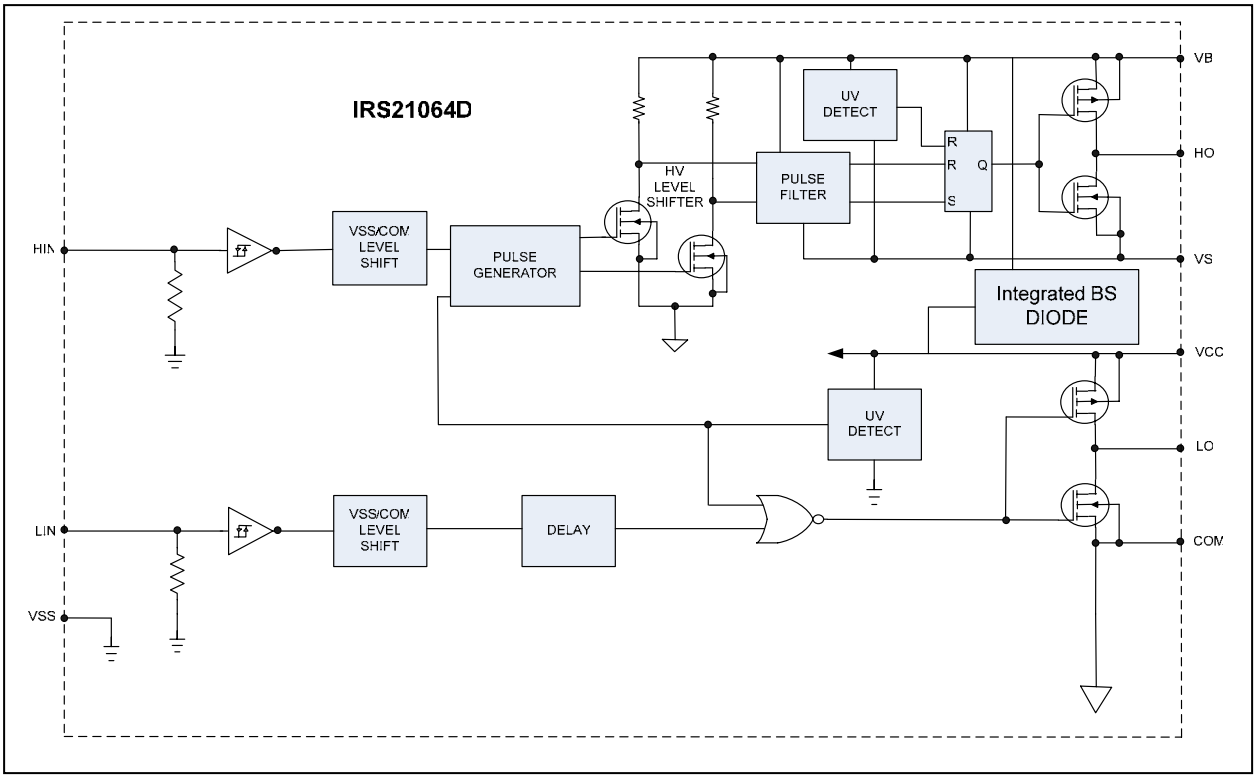
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM and T_A = 25°C unless otherwise specified. The $V_{IL,}$ V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads. The $V_{O,}$ I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{InTH+}	Positive input threshold voltage	—	—	2.2	V	V_{CC} = 10V to 20V
V_{InTH-}	Negative input threshold voltage	0.8	—	—		V_{CC} = 10V to 20V
V_{OH}	High level output voltage	—	0.8	1.4		I_O = 20 mA
V_{OL}	Low level output voltage	—	0.3	0.6		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	45	70		V_{IN} = 0V or 4V
I_{QCC}	Quiescent V_{CC} supply current	500	1100	1700		V_{IN} = 0V or 4V
I_{IN+}	Logic "1" input bias current	—	5	20		V_{IN} = 4V
I_{IN-}	Logic "0" input bias current	—	—	2		V_{IN} = 0V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going Threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going Threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage Hysteresis	—	0.7	—		
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	V_O = 0V, PW ≤ 10 us
I_{O-}	Output low short circuit pulsed current	250	350	—		V_O = 15V, PW ≤ 10 us
Rbs	Bootstrap resistance	—	200	—	Ohm	V_{CC} = 15

Functional Block Diagrams

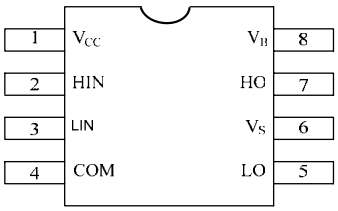




Lead Definitions

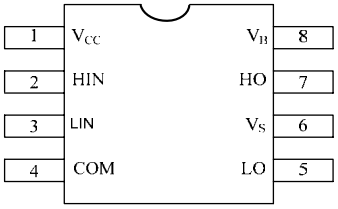
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic Ground (IRS21064D only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



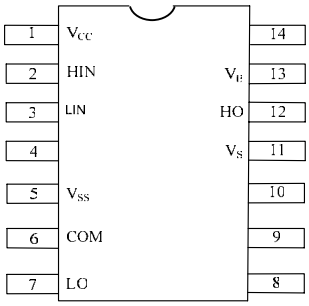
8 Lead PDIP

IRS2106D



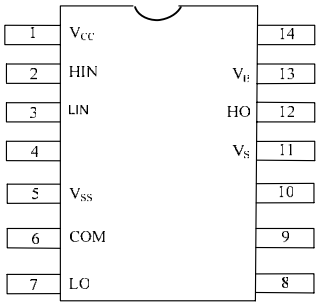
8 Lead SOIC

IRS2106DS



14 Lead PDIP

IRS21064D



14 Lead SOIC

IRS21064DS

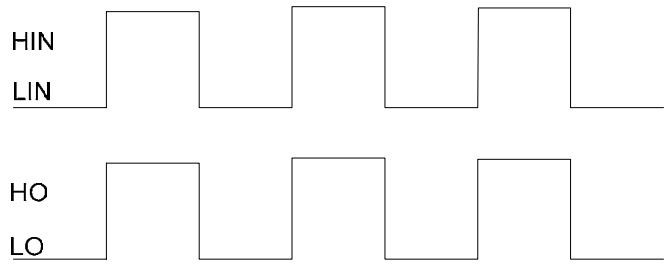


Figure 1. Input/Output Timing Diagram

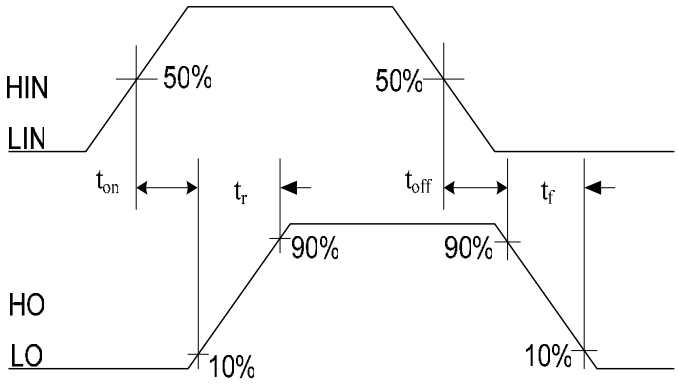


Figure 2. Switching Time Waveform Definitions

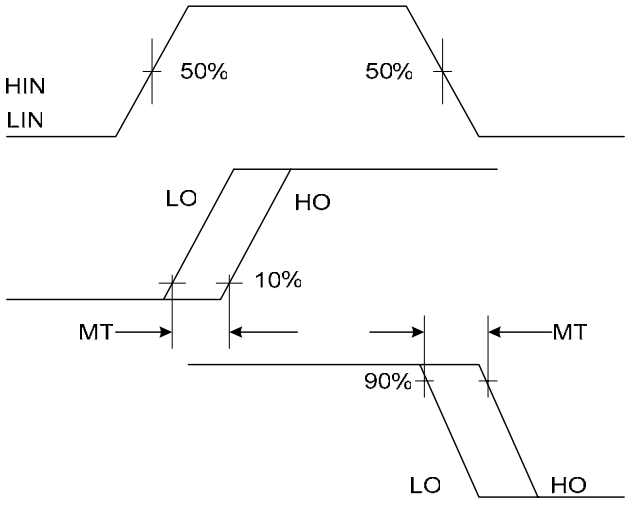
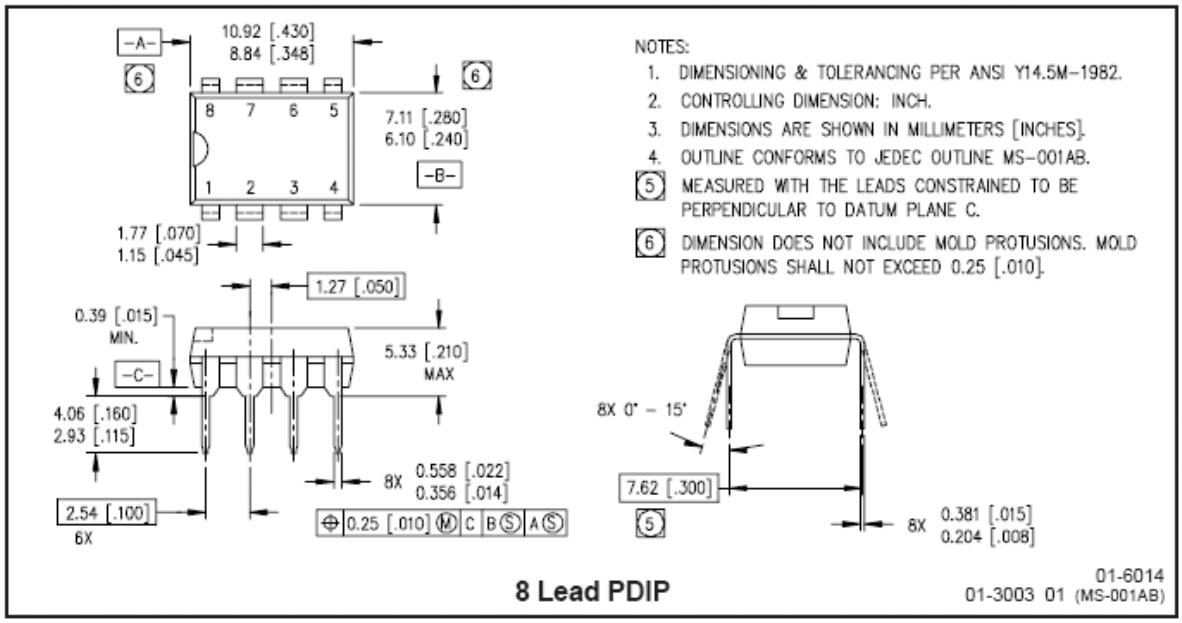


Figure 3. Delay Matching Waveform Definitions

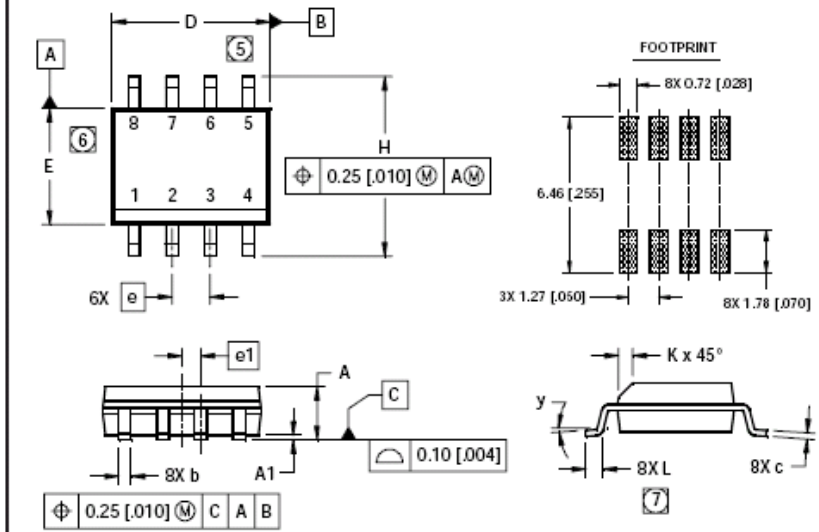
Case Outlines



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

8 Lead PDIP

01-6014
01-3003 01 (MS-001AB)

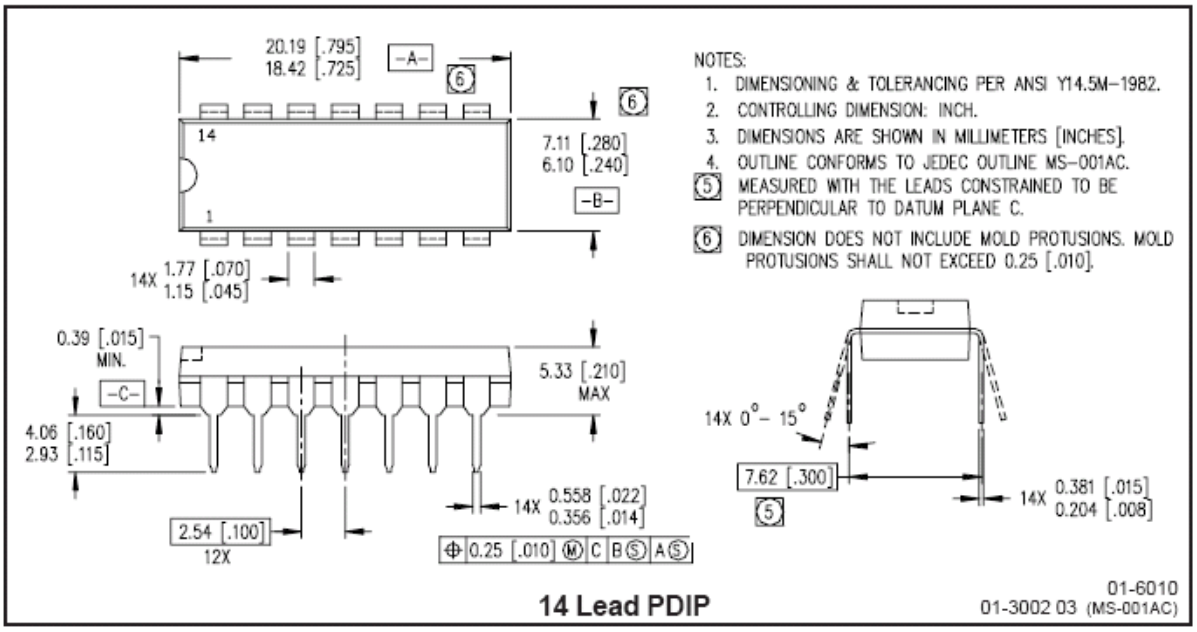


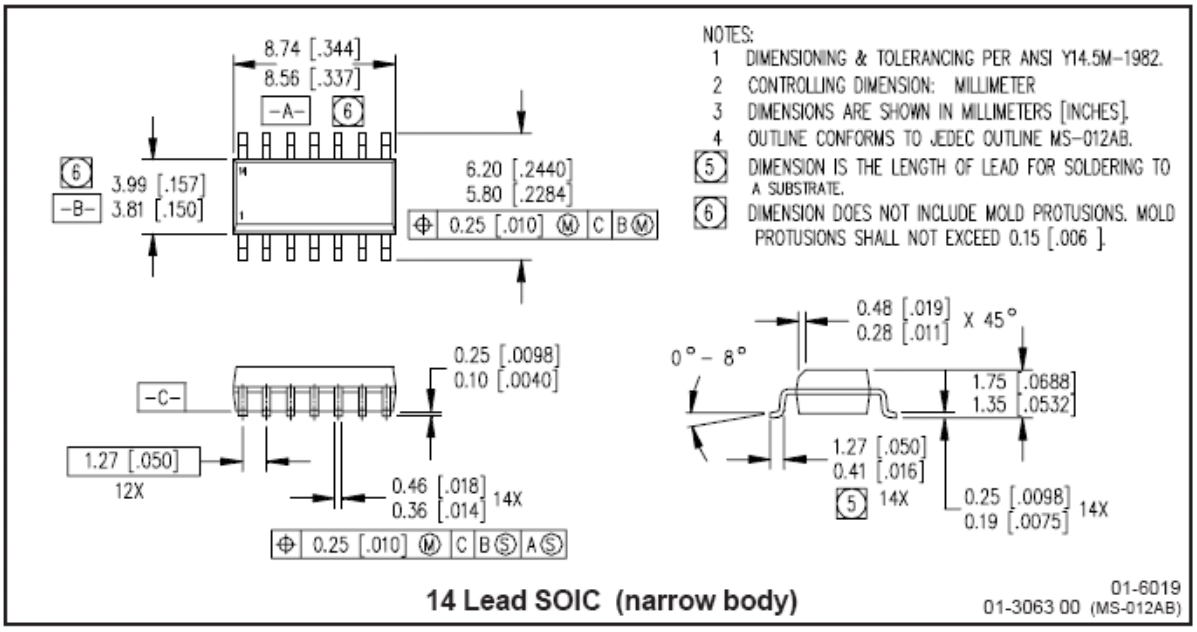
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

01-6027
01-0021 11 (MS-012AA)


20.19 [.795]
18.42 [.725]
-A-
6
14
1
7.11 [.280]
6.10 [.240]
-B-
14X 1.77 [.070]
1.15 [.045]
0.39 [.015]
MIN.
-C-
5.33 [.210]
MAX
4.06 [.160]
2.93 [.115]
14X 0.558 [.022]
0.356 [.014]
2.54 [.100]
12X
0.25 [.010] M C B S A S
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5 MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].
14X 0° - 15°
7.62 [.300]
5
14X 0.381 [.015]
0.204 [.008]
14 Lead PDIP
01-6010
01-3002 03 (MS-001AC)


8.74 [.344]
8.56 [.337]
-A-
6
6
-B-
3.99 [.157]
3.81 [.150]
6.20 [.2440]
5.80 [.2284]
0.25 [.010] M C B M
-C-
0.25 [.0098]
0.10 [.0040]
1.27 [.050]
12X
0.46 [.018]
0.36 [.014] 14X
0.25 [.010] M C B S A S
NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AB.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].
0.48 [.019]
0.28 [.011] X 45°
0° - 8°
1.75 [.0688]
1.35 [.0532]
1.27 [.050]
0.41 [.016]
5 14X
0.25 [.0098]
0.19 [.0075] 14X
14 Lead SOIC (narrow body)
01-6019
01-3063 00 (MS-012AB)