ITZ35F12

Powerline N-Channel IGBT

Advance Information

Supersedes November 1998, version DS5069-1.0

DS5069-2.1 January 1999

The ITZ35F12 is a very robust non punch through n-channel, enhancement mode insulated gate bipolar transistor (IGBT) designed for low power dissipation in a wide range of high voltage applications such as power supplies and motor drives. The high impedance gate simplifies gate drive considerations, allowing operation directly from low power control circuitry.

The device is optimised for high frequency operation with fast rise and fall times. The product is suitable for modern systems employing switching frequencies up to and beyond the audible spectrum.

Low saturation voltages minimise power dissipation, thereby reducing the cost of the overall system in which they are used.

The ITZ is fully short circuit rated making it especially suited for motor control and other applications requiring short circuit withstand capability. Each device in the Powerline range is available with or without an integral anti-parallel ultrafast soft recovery diode, see separate datasheet for co-pack device.

Typical applications include high frequency inverters for motor control, pwm, welding and heating apparatus. The Powerline range of IGBTs is also applicable to switched mode (SMPS) and uninterruptible power supplies (UPS).

FEATURES

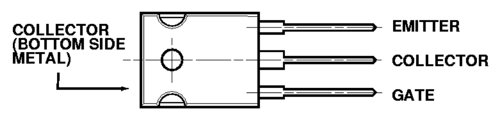
- Enhancement Mode n-Channel Device
- Non Punch Through Structure
- High Switching Speed
- Low On-state Saturation Voltage
- High Input Impedance Simplifies Gate Drive
- Fully Short Circuit Rated To 10μs
- Square RBSOA

APPLICATIONS

- High Frequency Inverters
- Motor Control
- Switched Mode Power Supplies
- High Frequency Welding
- UPS Systems
- PWM Drives

KEY PARAMETERS

V_{CES}	(max)	1200V
$V_{CE(sat)}$	(typ)	2.7V
I_{C25}	(max)	65A
I_{C85}	(max)	35A
I_{CM}	(max)	105A
t_{sc}	(max)	10μs



Outline type code: TO247

(See Package Outlines for further information)

Fig.1 Pin connections - top view (not to scale)

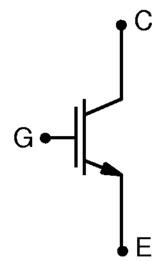


Fig.2 ITZ35F12 circuit

ORDERING INFORMATION

ITZ35F12P TO247

Note: When ordering, use the complete part number.

Caution: These devices are sensitive to electrostatic discharge. Users should observe proper ESD handling precautions.

ITZ35F12

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device.

T_{case} = 25˚C unless stated otherwise.

Symbol	Parameter	Test Conditions	Max.	Units
V_{CES}	Collector-emitter voltage	V_{GE} = 0V	1200	V
V_{GES}	Gate-emitter voltage	-	±20	V
I_{C25}	Continuous collector current	T_{case} = 25˚C	65	A
I_{C85}	Continuous collector current	T_{case} = 85˚C	35	A
I_{CM}	Pulsed collector current	1ms, T_{case} = 85˚C	105	A
P_{tot}	Power dissipation	T_{case} = 85˚C	155	W

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance	DC junction to case	-	0.42	°C/W
T_{OP}	Operating junction temperature range	-	–40	150	°C
T_{stg}	Storage temperature range	-	–40	150	°C
-	Mounting torque	M3 screw	-	1.1	Nm

DC ELECTRICAL CHARACTERISTICS

T_{case} = 25˚C unless stated otherwise.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CES}	Collector cut-off current	V_{GE} = 0V, V_{CE} = 1200V	-	-	1	mA
I_{GES}	Gate leakage current	V_{GE} = 20V, V_{CE} = 0V	-	-	±500	nA
$V_{GE(TH)}$	Gate threshold voltage	I_C = 2mA, V_{CE} = V_{GE}	4.5	6	7.5	V
$V_{CE(SAT)}$	Collector-emitter saturation voltage	V_{GE} = 15V, I_C = 35A	-	2.7	3.3	V
		V_{GE} = 15V, I_C = 35A, T_j = 125˚C	-	3.3	-	V

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AC ELECTRICAL CHARACTERISTICS

T_{case} = 25˚C unless stated otherwise.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{ies}	Input capacitance	V_{CE} = 25V, V_{GE} = 15V, f = 1MHz	-	8040	-	pF
C_{oes}	Output capacitance	V_{CE} = 25V, V_{GE} = 15V, f = 1MHz	-	340	-	pF
C_{res}	Reverse transfer capacitance	V_{CE} = 25V, V_{GE} = 15V, f = 1MHz	-	90	-	pF

INDUCTIVE SWITCHING CHARACTERISTICS - see figures 3 to 5

T_{case} = 25˚C unless stated otherwise.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{d(ON)}$	Turn-on delay time	I_C = 35A, V_{GE} = ±15V, V_{CE} = 50%V_{ces}, $R_{G(ON)}$ = 20Ω, $R_{G(OFF)}$ = 5Ω	-	75	-	ns
t_r	Rise time		-	45	-	ns
E_{ON}	Turn-on energy loss - per cycle		-	3.2	-	mJ
$t_{d(OFF)}$	Turn-off delay time		-	240	-	ns
t_f	Fall time		-	60	-	ns
E_{OFF}	Turn-off energy loss - per cycle		-	3.7	-	mJ
T_{case} = 125˚C unless stated otherwise.						
$t_{d(ON)}$	Turn-on delay time	I_C = 35A, V_{GE} = ±15V, V_{CE} = 50%V_{ces}, $R_{G(ON)}$ = 20Ω, $R_{G(OFF)}$ = 5Ω	-	75	-	ns
t_r	Rise time		-	50	-	ns
E_{ON}	Turn-on energy loss - per cycle		-	5.5	-	mJ
$t_{d(OFF)}$	Turn-off delay time		-	270	-	ns
t_f	Fall time		-	80	-	ns
E_{OFF}	Turn-off energy loss - per cycle		-	4.7	-	mJ

For additional switching information please refer to figures 8 to 13.

SHORT CIRCUIT RATING

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{sc}	Short circuit withstand time	T_c = 125˚C, V_{GE} = 15V, V_{CE} = 80% V_{CES}	-	-	10	µs

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BASIC TEST CIRCUIT AND SWITCHING DEFINITIONS

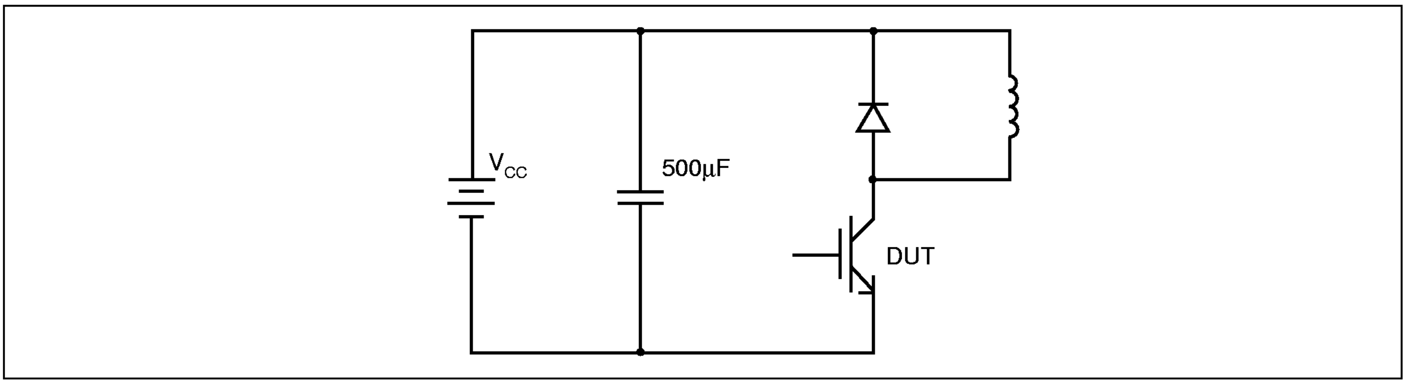

Fig.3 Basic d.c. chopper ciruit

$t_{d(on)} = t_2 - t_1$

$t_r = t_3 - t_2$

$E_{on} = \int_{t_1}^{t_3 + 1\mu s} V_{CE} \cdot I_C \, dt$

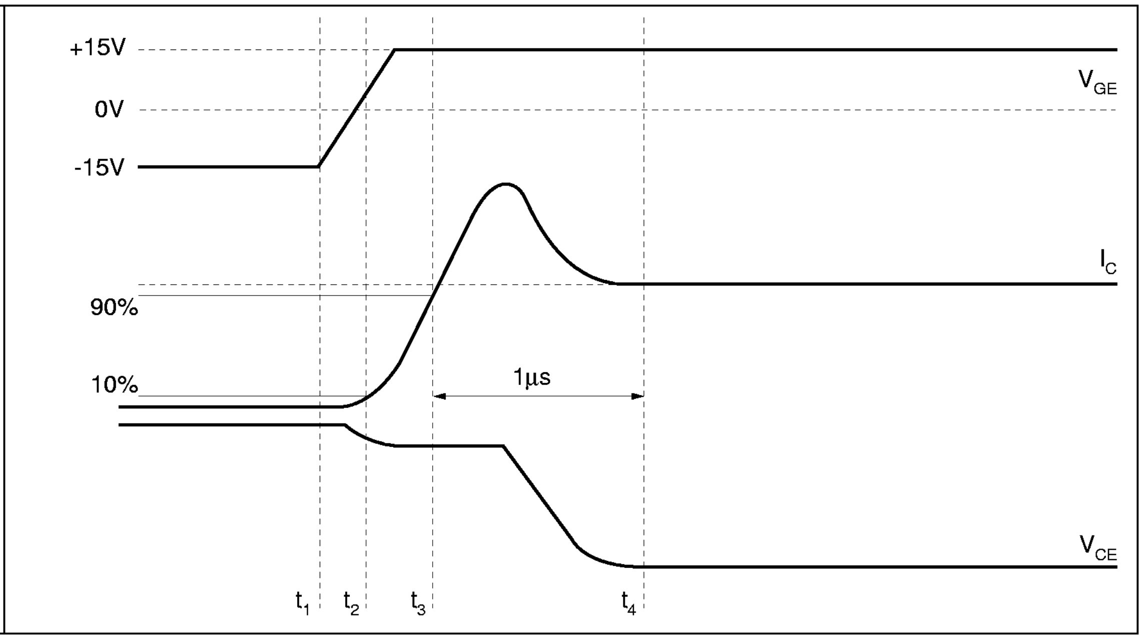

Fig.4 Turn-on characteristics

$t_{d(off)} = t_6 - t_5$

$t_f = t_7 - t_6$

$E_{off} = \int_{t_5}^{t_7 + 1\mu s} V_{CE} \cdot I_C \, dt$

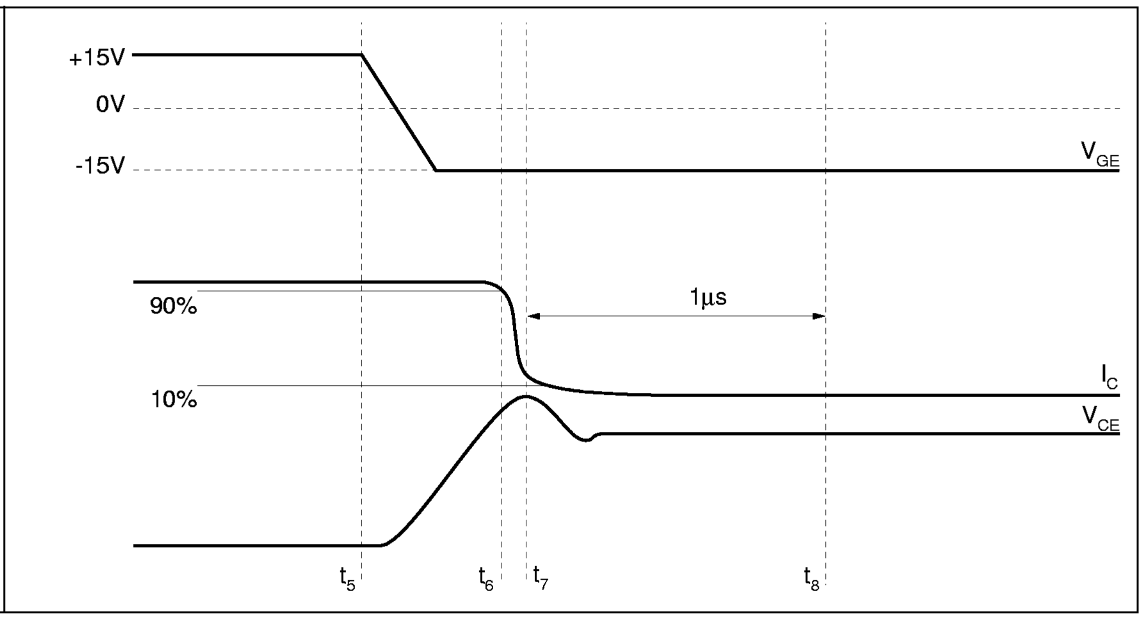

Fig.5 Turn-off characteristics

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CURVES

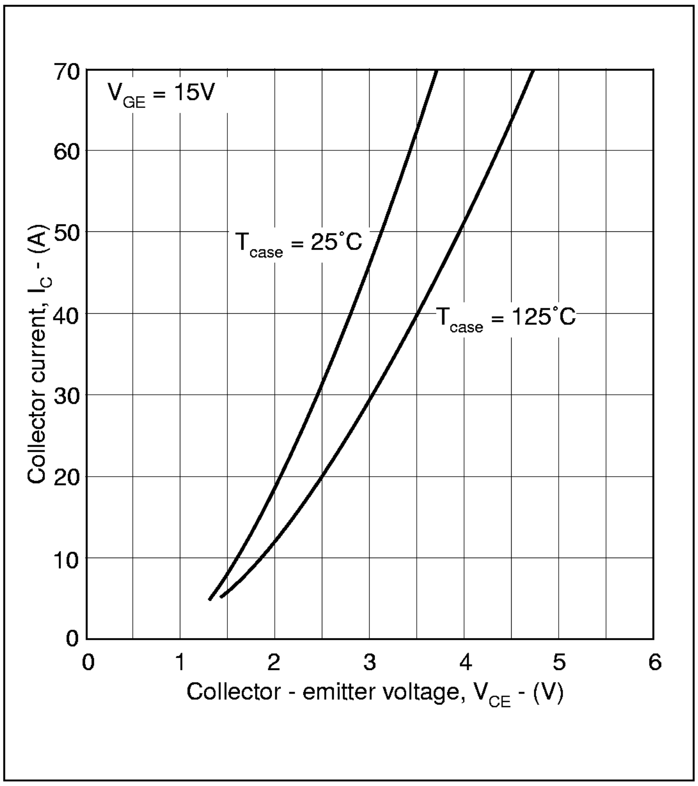

Fig.6 Typical output characteristics

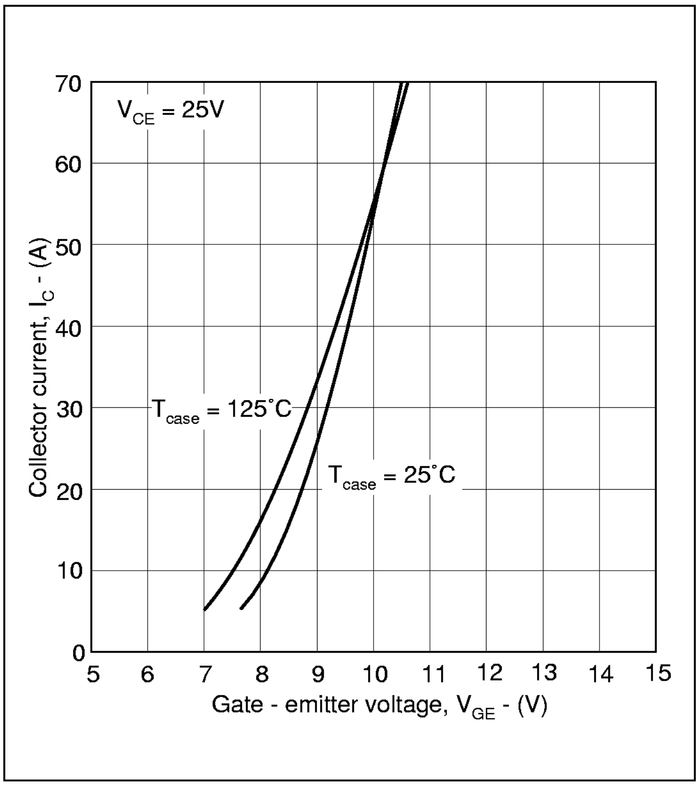

Fig.7 Typical transfer characteristics

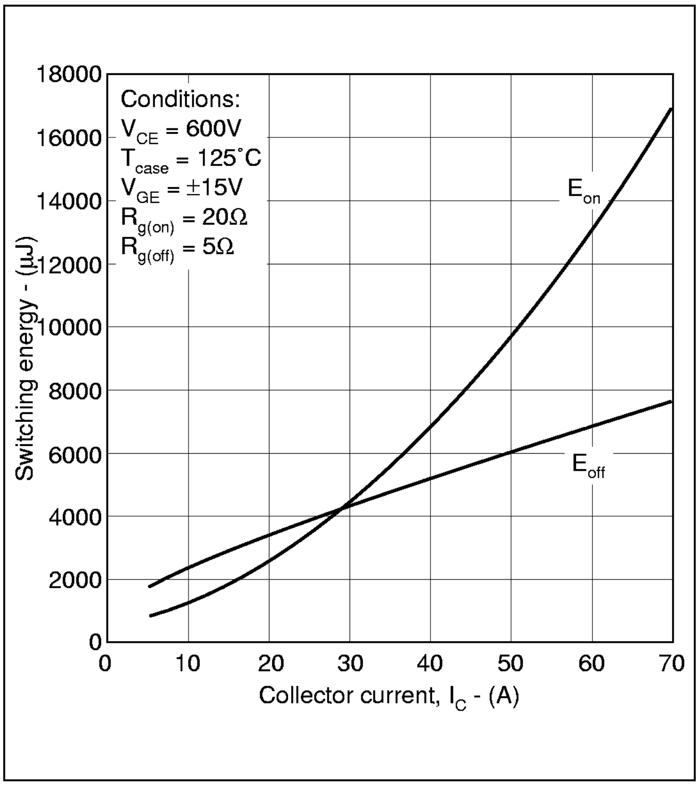

Fig.8 Typical switching losses vs collector current

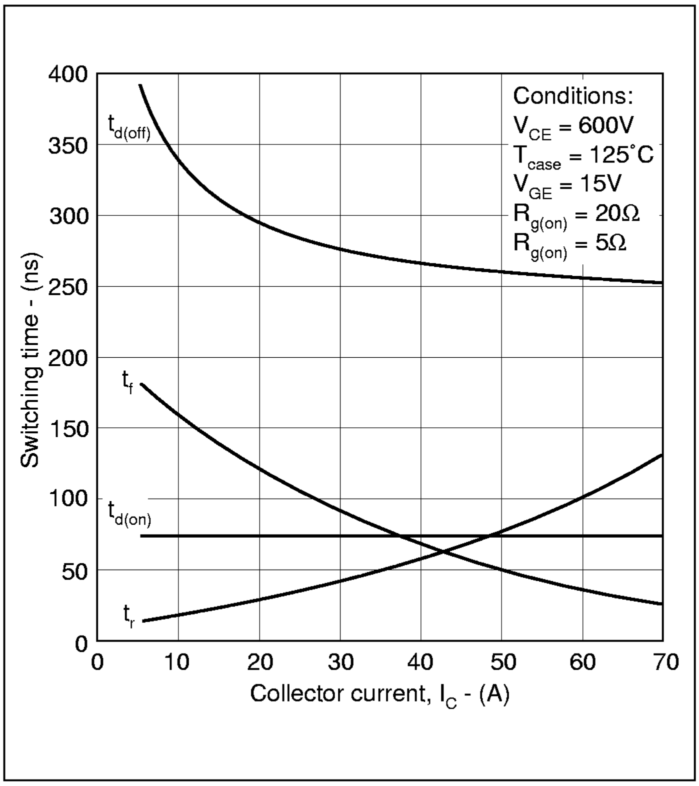

Fig.9 Typical switching times vs collector current

Caution: These devices are sensitive to electrostatic discharge. Users should observe proper ESD handling precautions.

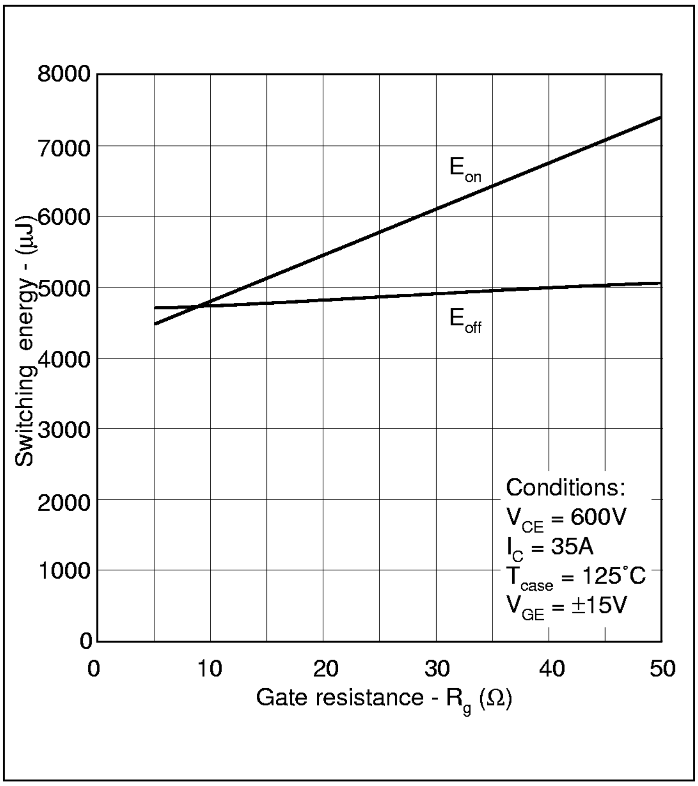

Fig.10 Typical switching losses vs gate resistance

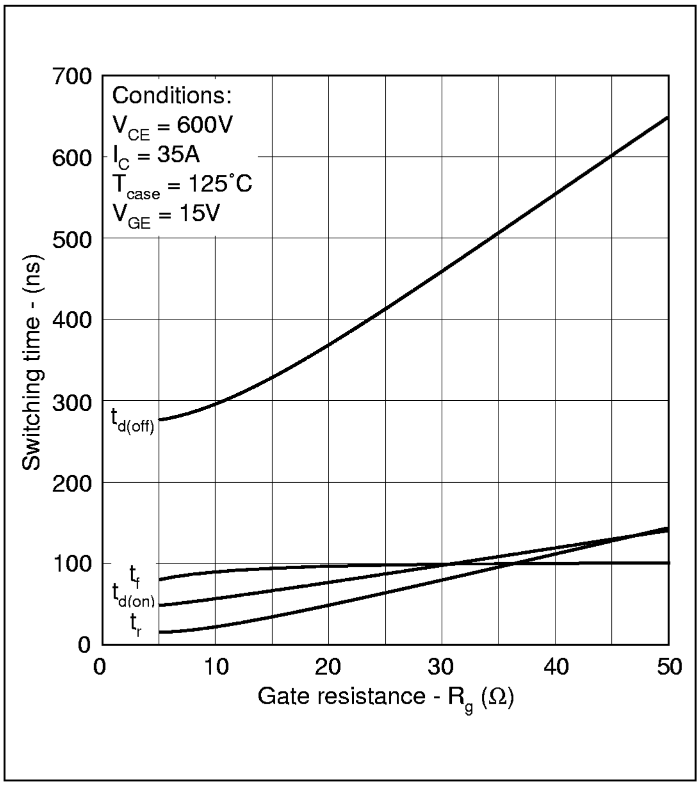

Fig.11 Typical switching times vs gate resistance

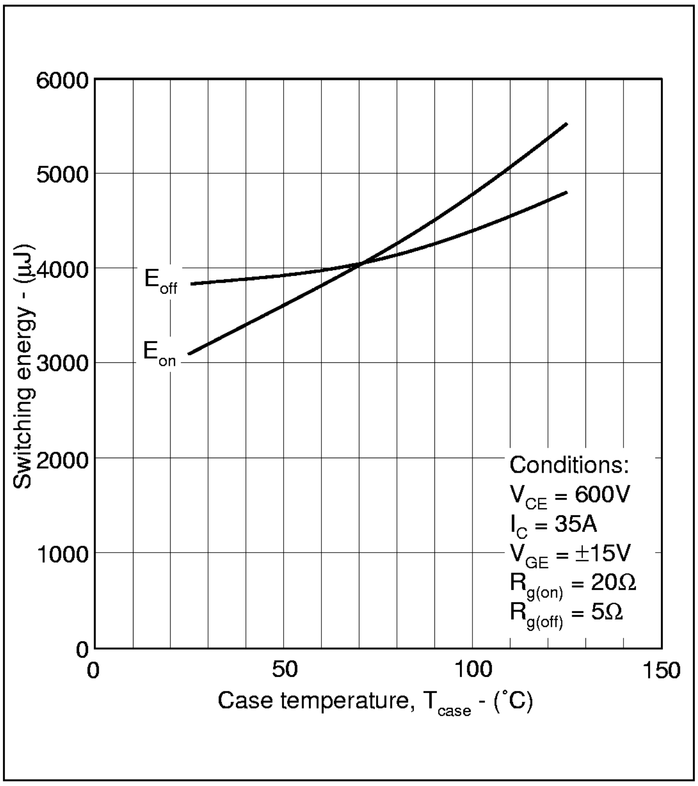

Fig.12 Typical switching losses vs case temperature

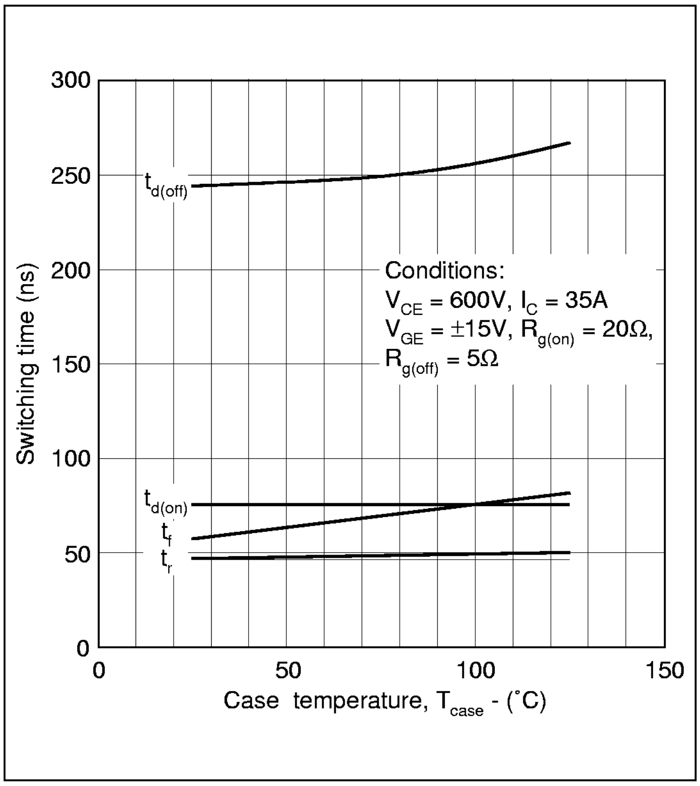

Fig.13 Typical switching time vs case temperature

Caution: These devices are sensitive to electrostatic discharge. Users should observe proper ESD handling precautions.

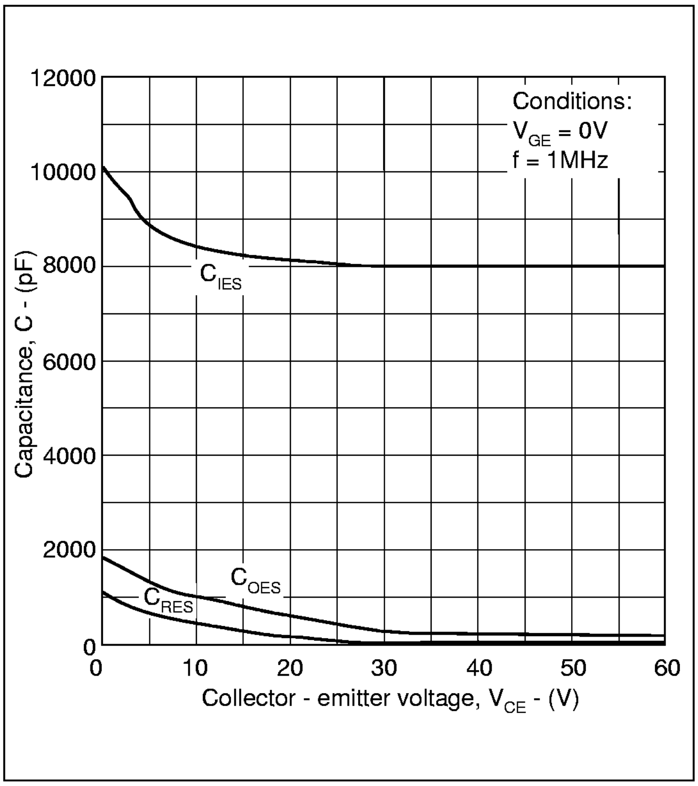

Fig.14 Typical capacitance

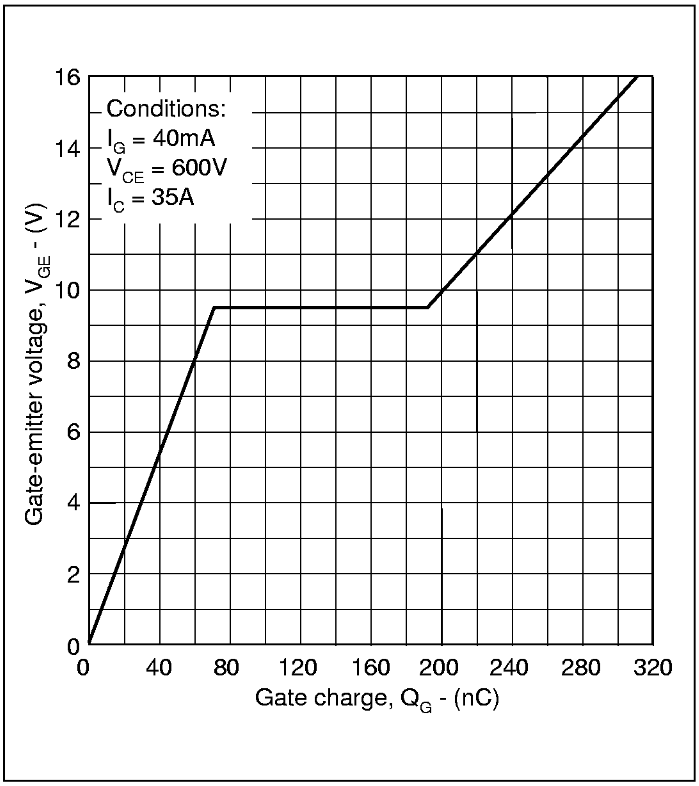

Fig.15 Typical gate charge

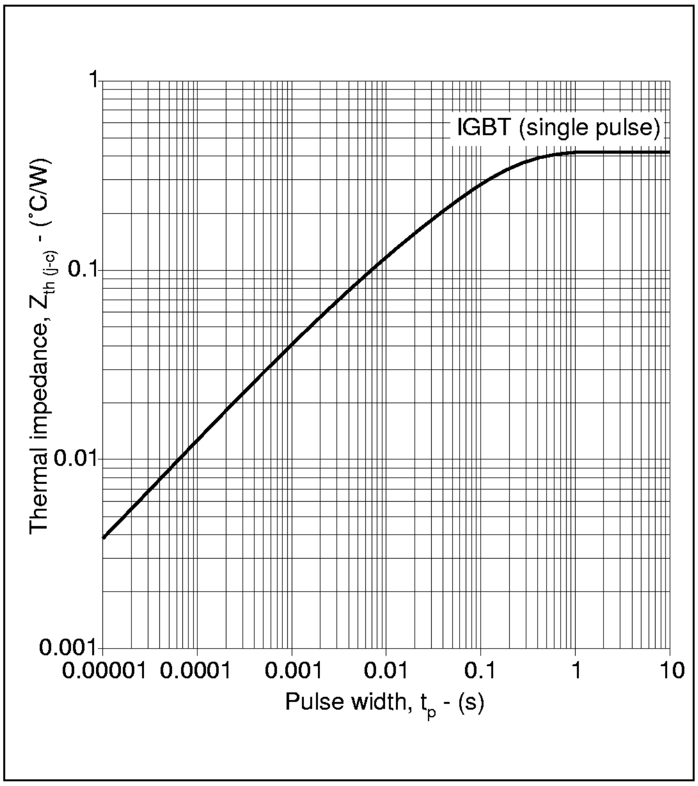

Fig.16 Transient thermal impedance - junction to case

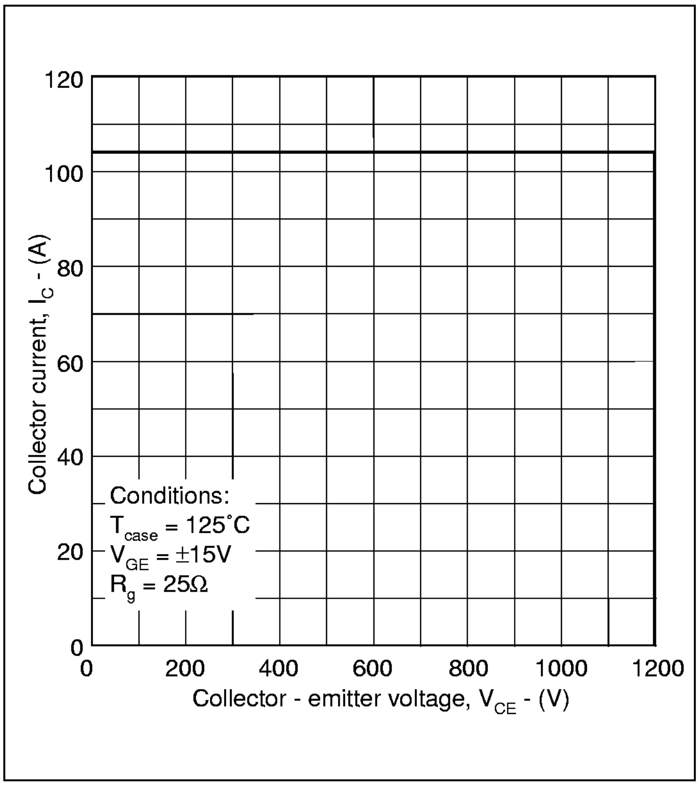

Fig.17 Reverse bias safe operating area

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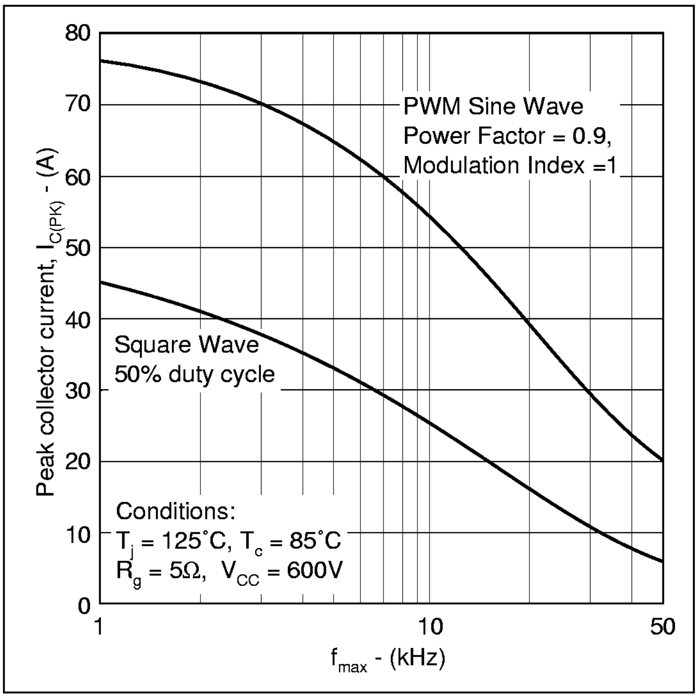


Fig.18 Three Phase PWM inverter operating frequency

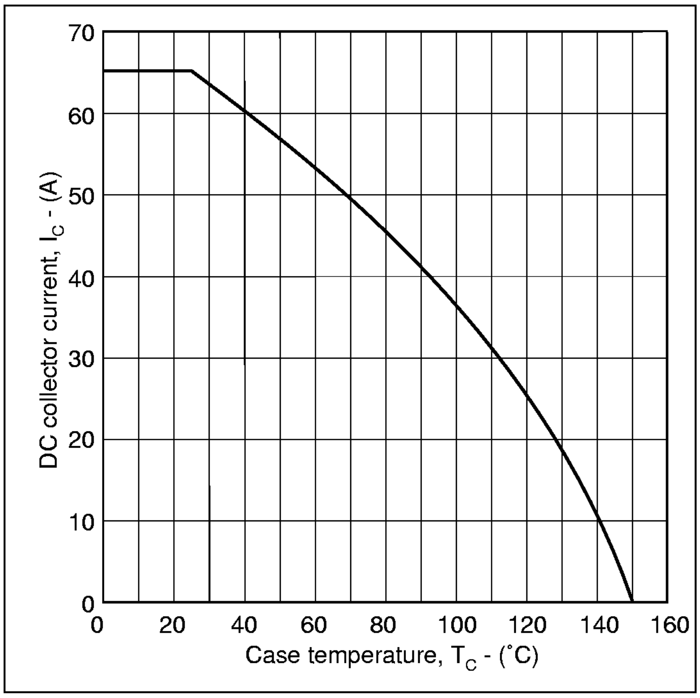
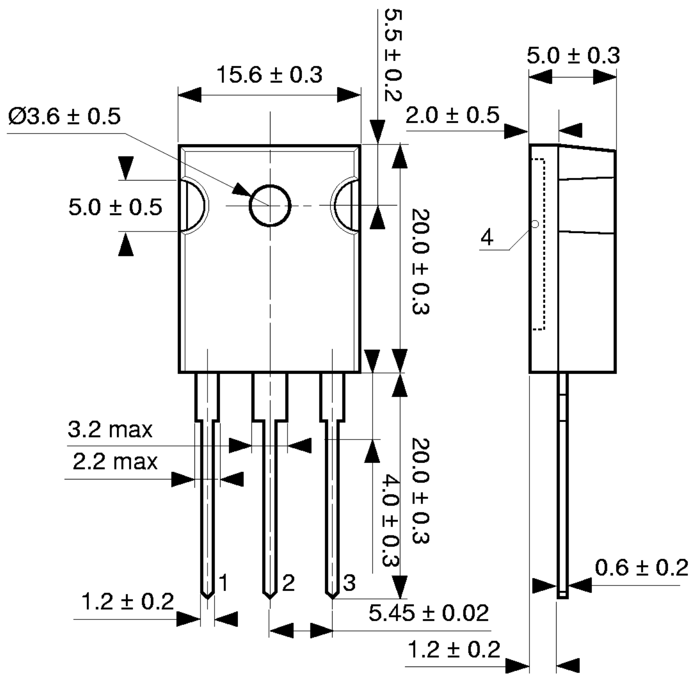


Fig.19 DC current rating vs case temperature

PACKAGE OUTLINE - TO247

For further package information, please contact your local Customer Service Centre. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Terminal 1 - Gate
Terminal 2 - Collector
Terminal 3 - Emitter
Terminal 4 - Collector

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These are supported by agents and distributors in major countries world-wide.

ADVANCE INFORMATION - The product design is complete and final characterisation for volume production is well in hand.

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