LSI LOGIC CORPORATION

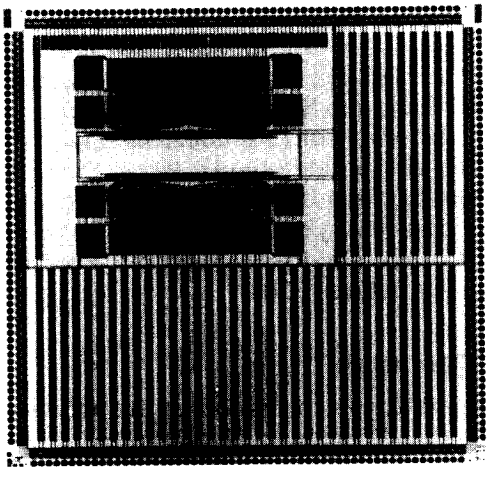
LSA2003 Two Micron HCMOS Structured Array™

General Description

The LSA2003 is a member of the 2-micron drawn, (1.4-micron effective) HCMOS family of Structured Arrays offered by LSI LOGIC Corporation. These very high performance, Application Specific Integrated Circuits (ASICs) combine special purpose silicon structures, optimized for performance with general purpose logic arrays on a single chip. Structured Arrays provide a high density of logic functionality while maintaining the flexibility of design and fast turn-around of metal mask programmable logic-arrays. The use of dual layer metal interconnect technology provides high speed, high packing density, ease of layout and the ability to configure megacell architectures at the interconnect level.

Contains The Following Structures:

- 6900 gate LL7000 Series type 2-micron drawn (1.4-micron effective) logic array
- 4608-bit configurable RAM
  - Fully static
  - Divisible into as many as four separate 1152-bit RAMs
  - Each RAM individually accessible and configurable
  - Any size RAM can be uniquely configured as a $\times 4$, $\times 9$, $\times 18$ or $\times 36$.
  - Latches on outputs and data/address inputs
  - Three-state outputs
  - Low power standby mode
  - Built-in scan testability
  - Programmable output buffers



LSA2003 Pad Statistics

Max Pads[1]		Max I/O Pads[1]		Max Package Pins[2]	
Plastic or Ceramic	Ceramic	Plastic or Ceramic	Ceramic	Plastic or Ceramic	Ceramic
174	228	158	216	170	228

Notes:

1. The difference between the maximum number of pads and I/Os is the number of dedicated V_{DD} or V_{SS} pads. It may be necessary to configure additional I/O pads for V_{DD}/V_{SS}, depending on the number and drive of the output buffers.

2. LSI LOGIC recommends that all LSA2003 designs be configured for use in plastic packages, thus permitting upward compatibility to ceramic packages, where required. Does not apply to military designs.

RAM AC Switching Characteristics—2304-bit RAM

RAM Size	Parameter	Worst-Case Commercial	Worst-Case Military
1152-bit	Read Cycle Time	39.2ns	50.0ns
	Write Cycle Time	19.7ns	25.1ns
2304-bit	Read Cycle Time	47.0ns	60.0ns
	Write Cycle Time	25.8ns	32.9ns

Commercial: 0°C to 70°C, $V_{DD} = 4.75V$ to $5.25V$
Military: -55°C to 125°C, $V_{DD} = 4.5V$ to $5.5V$

Note: The above specifications represent worst-case values for worst-case configuration (512×4). Most other configurations will be slightly faster.

Available Packages

Ceramic Pin Grid Array—64, 68, 84, 100, 120, 132, 144, 180, 224 pins
Plastic Pin Grid Array—68, 84, 100, 120, 132, 144, 180 pins
Ceramic Chip Carrier (Leaded and Leadless)—68, 84, 100, 132 pins
Plastic Chip Carrier (J-bend)—68, 84 pins

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Configurable RAM

Description

The LSA2003 contains two 2304-bit metal mask configurable asychronous static RAMs with scan testing and power down. Each RAM is word length and bit width configurable either as a single RAM or as two individual, independently configurable RAMs (RAM A and RAM B).

All RAM configurations contain latched address and data inputs as well as latched three-state outputs. These latches facilitate pipelined operation and easy interface with the other structures in the array.

Read Operation

Read Operation is controlled by the active-HIGH Output Clock (OCK) input. When the Output Clock is held HIGH and the RAM is selected (CS = HIGH), data will be read from the addressed location and presented at the data ouputs. When the Output Clock input is held LOW, the output latches are latched, containing data just read from the RAM; also, the outputs of the RAM (into the output latches) are pulled HIGH.

Write Operation

Write Operation is controlled by the active-HIGH Write Enable (WE) input. When the Write Enable is held HIGH and the RAM selected (CS = HIGH), data from the data inputs will be written into the addressed location. This same data can be made available at the data outputs by holding the Output Clock (OCK) input HIGH.

RAM Configuration Table

	RAM Configuration Words × Bits
Combined Single RAMs (4608-Bit)	1024 × 4 512 × 9 256 × 18 128 × 36 64 × 72 32 × 144
Single RAM (2304-Bit)	512 × 4 256 × 9 128 × 18 64 × 36
Each Half RAM (1152-Bit)	256 × 4 128 × 9 64 × 18 32 × 36

Any RAM or combination of RAMs can be used up to a total of 4608 bits.

There are a total of four separate 1152-bit RAM blocks. Each individually configurable. These can be used in any combination as a single RAM up to 4608-bits or used as up to four separate 1152-bit RAMs.

Latch Related Operation

The data input address input and data output signals all pass through built-in latches. Each group of latches are independently controlled by a separate latch enable (ICKDATA for the data input latches, ICKADR for the address input latches and OCK for the data output latches). OCK controls the read operation of the RAM as well as the output latches.

Latches may be used at any time during RAM operation or set to transparent if the latches are not to be used.

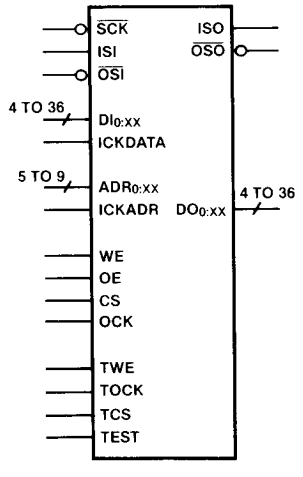
Scan Path Operation

The built-in latches can be placed in scan mode to preload data and test the RAM independently of the rest of the logic on the array. Scan path refers to a technique whereby the on-board latches can be used as serial shift registers. Data may be shifted into the address and data inputs through a single pin (ISI), written into the RAM, read out of the RAM, then shifted out through a different pin ($\overline{OSO}$).

The LSI LOGIC RAM scan path configuration contains a single scan path for the address and input latches and a separate scan path for the output latches. Each scan path has a unique input and output pin but all are controlled by a single scan clock ($\overline{SCK}$).

The scan operation commences by holding the TEST input HIGH. This disables all the RAM Control and Latch Control inputs and enables TCS, TWE and TOCK (Test Chip Select, Test Write Enable and Test Output Clock, respectively).

RAM Typical 2304-bit Configuration Option Block (One of Two)



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