● MOTOROLA

MC145152-1

Advance Information

PARALLEL INPUT PLL FREQUENCY SYNTHESIZER

The MC145152-1 is programmed by sixteen parallel inputs. The device features consist of a reference oscillator, selectable-reference divider, two output phase dectector, 10-bit programmable divide-by-N counter and 6-bit programmable ÷ A counter. When combined with a loop filter and VCO, the MC145152-1 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and MC145152-1.

The MC145152-1 offers improved performance over the MC145152. Modulus Control output drive has been increased and the ac characteristics have been improved. Input current requirements have also been changed.
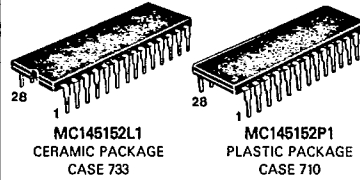
- General Purpose Applications:
  CATV   TV Tuning
  AM/FM Radios   Scanning Receivers
  Two-Way Radios Amateur Radio
- Low Power Consumption
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User-Selectable ÷ R Values — 8, 64, 128, 256, 512, 1024, 1160, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 63
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates
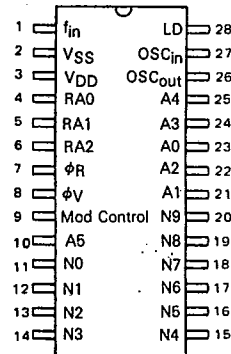

HIGH-PERFORMANCE
CMOS
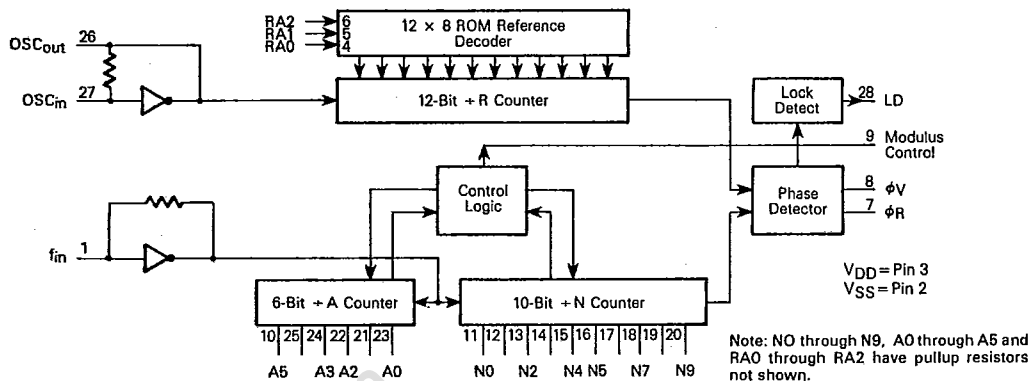### LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

PARALLEL INPUT PLL
FREQUENCY SYNTHESIZER

MC145152L1
CERAMIC PACKAGE
CASE 733

MC145152P1
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT

1	f_{in}	LD	28
2	V_{SS}	OSC_{in}	27
3	V_{DD}	OSC_{out}	26
4	RA0	A4	25
5	RA1	A3	24
6	RA2	A0	23
7	ϕR	A2	22
8	ϕV	A1	21
9	Mod Control	N9	20
10	A5	N8	19
11	N0	N7	18
12	N1	N6	17
13	N2	N5	16
14	N3	N4	15

BLOCK DIAGRAM

Note: N0 through N9, A0 through A5 and RA0 through RA2 have pullup resistors not shown.

V_{DD} = Pin 3
V_{SS} = Pin 2

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
  Plastic "P" Package: -12 mW/°C from 65°C to 85°C
  Ceramic "L" Package: No derating

> This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
> Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD}	-40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Voltage Range	V_{DD}	-	3	9	3	-	9	3	9	V
Output Voltage 0 Level V_{in}=0 V or V_{DD} $I_{out} \approx 0 \mu A$	V_{OL}	3	-	0.05	-	0.001	0.05	-	0.05	V
		5	-	0.05	-	0.001	0.05	-	0.05	
		9	-	0.05	-	0.001	0.05	-	0.05	
1 Level	V_{OH}	3	2.95	-	2.95	2.999	-	2.95	-	
		5	4.95	-	4.95	4.999	-	4.95	-	
		9	8.95	-	8.95	8.999	-	8.95	-	
Input Voltage 0 Level V_{out}=0.5 V or V_{DD}-0.5 V (All Outputs Except OSC_{out})	V_{IL}	3	-	0.9	-	1.35	0.9	-	0.9	V
		5	-	1.5	-	2.25	1.5	-	1.5	
		9	-	2.7	-	4.05	2.7	-	2.7	
1 Level	V_{IH}	3	2.1	-	2.1	1.65	-	2.1	-	
		5	3.5	-	3.5	2.75	-	3.5	-	
		9	6.3	-	6.3	4.95	-	6.3	-	
Output Current — Modulus Control Source V_{out}=2.7 V V_{out}=4.6 V V_{out}=8.5 V	I_{OH}	3	-0.60	-	-0.50	-1.5	-	-0.30	-	mA
		5	-0.90	-	-0.75	-2.0	-	-0.50	-	
		9	-1.50	-	-1.25	-3.2	-	-0.80	-	
Sink V_{out}=0.3 V V_{out}=0.4 V V_{out}=0.5 V	I_{OL}	3	1.30	-	1.10	5.0	-	0.66	-	
		5	1.90	-	1.70	6.0	-	1.08	-	
		9	3.80	-	3.30	10.0	-	2.10	-	
Output Current — Other Outputs Source V_{out}=2.7 V V_{out}=4.6 V V_{out}=8.5 V	I_{OH}	3	-0.44	-	-0.35	-1.0	-	-0.22	-	mA
		5	-0.64	-	-0.51	-1.2	-	-0.36	-	
		9	-1.30	-	-1.00	-2.0	-	-0.70	-	
Sink V_{out}=0.3 V V_{out}=0.4 V V_{out}=0.5 V	I_{OL}	3	0.44	-	0.35	1.0	-	0.22	-	
		5	0.64	-	0.51	1.2	-	0.36	-	
		9	1.30	-	1.00	2.0	-	0.70	-	
Input Current — f_{in}, OSC_{in}	I_{in}	9	-	±50	-	±10	±25	-	±22	µA
Input Current — Other Inputs (with Pullups)	I_{IH}	9	-	0.3	-	0.00001	0.1	-	1.0	µA
	I_{IL}	9	-	-400	-	-90	-200	-	-170	
Input Capacitance	C_{in}	-	-	10	-	6	10	-	10	pF
Quiescent Current V_{in}=0 V or V_{DD} I_{out}=0 µA	I_{DD}	3	-	800	-	200	800	-	1600	µA
		5	-	1200	-	300	1200	-	2400	
		9	-	1600	-	400	1600	-	3200	

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SWITCHING CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise Time, Modulus Control (Figures 1 and 5)	t_{TLH}	3	—	50	115	ns
		5	—	30	60	
		9	—	20	40	
Output Fall Time, Modulus Control (Figures 1 and 5)	t_{THL}	3	—	25	60	ns
		5	—	17	34	
		9	—	15	30	
Output Rise and Fall Time, LD, ϕ_V, ϕ_R (Figures 1 and 5)	t_{TLH}, t_{THL}	3	—	60	140	ns
		5	—	40	80	
		9	—	30	60	
Propagation Delay Time f_{in} to Modulus Control (Figures 2 and 5)	t_{PLH}, t_{PHL}	3	—	55	125	ns
		5	—	40	80	
		9	—	25	50	
Output Pulse Width ϕ_R, ϕ_V with f_R in Phase With f_V (Figures 3 and 5)	$t_{W(\phi)}$	3	25	100	175	ns
		5	20	60	100	
		9	10	40	70	
Input Rise and Fall Times OSC$_{in}$, f_{in} (Figure 4)	t_r, t_f	3	—	20	5	μs
		5	—	5	2	
		9	—	2	0.5	

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GRAPH 1 — OSC$_{in}$ AND f$_{in}$ MAXIMUM FREQUENCY VERSUS TOTAL DIVIDE VALUE

GRAPH 1A — V$_{DD}$ = 3 V

GRAPH 1B — V$_{DD}$ = 5 V

GRAPH 1C — V$_{DD}$ = 9 V
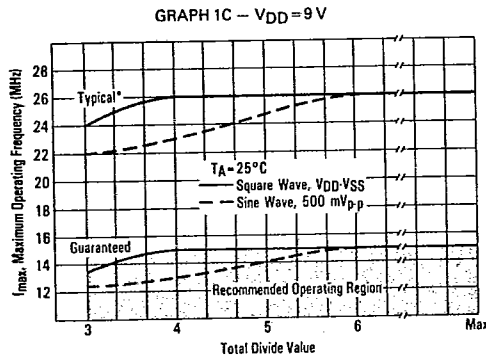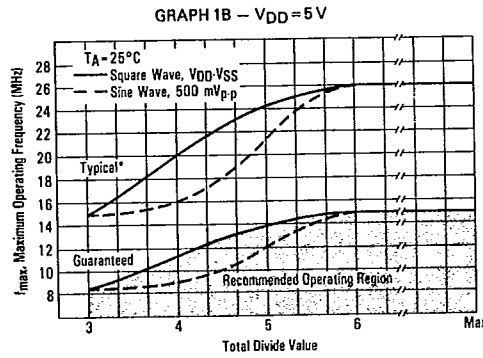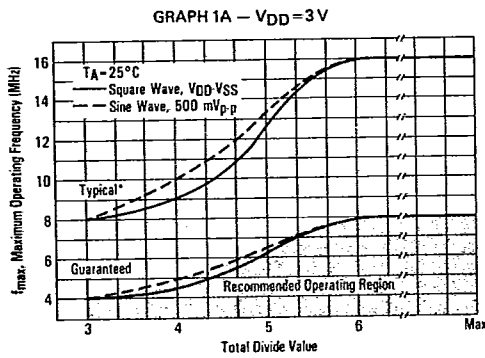
GRAPH 2 — OSC$_{in}$ AND f$_{in}$ MAXIMUM FREQUENCY VERSUS TEMPERATURE FOR
SINE AND SQUARE WAVE INPUTS

GRAPH 2A — TOTAL DIVIDE VALUE = 3, 4, OR 5

GRAPH 2B — TOTAL DIVIDE VALUE ≥ 6
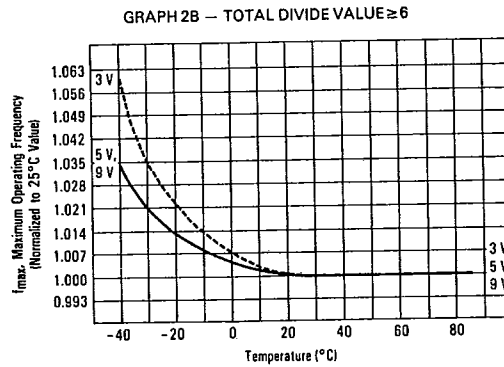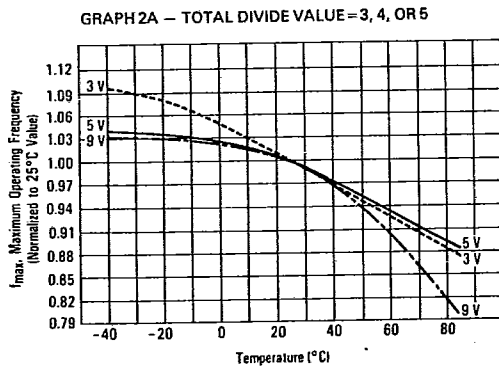
* Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

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PIN DESCRIPTIONS

f_{in} (Pin 1) — Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual modulus prescaler and is AC coupled into Pin 1. For larger amplitude signals (standard CMOS logic levels) DC coupling may be used.

V_{SS} (Pin 2) — Circuit Ground.

V_{DD} (Pin 3) — Positive power supply.

RA0, RA1, RA2 (Pins 4, 5, and 6) — These three inputs establish a code defining one of eight possible divide values for the total reference divider. The total reference divide values are as follows:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

ϕ_R, ϕ_V (Pins 7 and 8) — These phase detector outputs can be combined externally for a loop error signal.

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency of f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

MODULUS CONTROL (Pin 9) — Signal generated by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N − A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value $(N_T) = N \bullet P + A$ where P and P + 1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels; N the number programmed into the ÷ N counter and A the number programmed into the ÷ A counter.

N INPUTS (Pins 11 through 20) — The N inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is the least significant digit and N9 is the most significant. Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

A INPUTS (Pins 23, 21, 22, 24, 25, 10) — The A inputs define the number of clock cycles of f_{in} that require a logic zero on the modulus control output. See page 8 for explanation of dual modulus prescaling. The A inputs all have internal pullup resistors that ensure that inputs left open will remain at a logic one.

OSC_{out}, OSC_{in} (Pins 26 and 27) — These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

LD (Pin 28) — Lock detector signal. High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

PHASE LOCKED LOOP — LOW PASS FILTER DESIGN
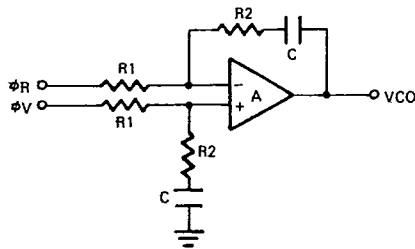
$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NCR1}}$$

$$\zeta = \frac{\omega_N R2C}{2}$$

Assuming gain A is very large, then:

$$F(s) = \frac{R2CS + 1}{R1CS}$$

NOTE. Sometimes R1 is split into two series resistors each R1 ÷ 2. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value for C_C should be such that the corner frequency of this network does not significantly affect ω_N.
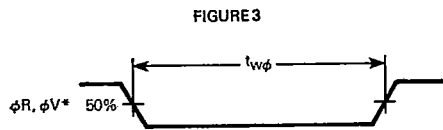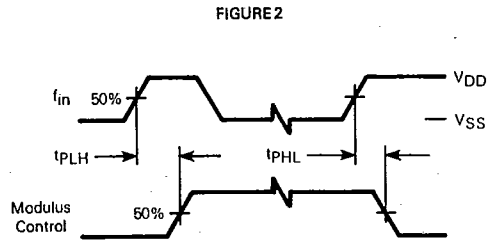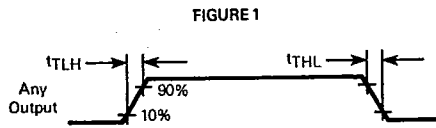
DEFINITIONS: N = Total Division Ratio in feedback loop

$K_\phi = V_{DD}/2\pi$

$K_{VCO} = \dfrac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design $\omega_N \cong (2\pi/10)\, f_r$ (at phase detector input)

$\zeta \cong 1$

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SWITCHING WAVEFORMS

FIGURE 1

t_{TLH} t_{THL}

Any
Output
90%
10%

FIGURE 2

f_{in} 50%
V_{DD}
V_{SS}

t_{PLH} t_{PHL}

Modulus
Control 50%

FIGURE 3

$\phi R, \phi V*$ 50% $t_{w\phi}$

* f_r in phase with f_v

FIGURE 4

t_r t_f

OSC_{in}, f_{in}
90%
10%
V_{DD}
V_{SS}

FIGURE 5 — TEST CIRCUIT

Device
Under
Test Output C_L
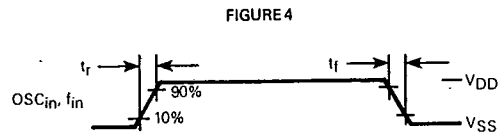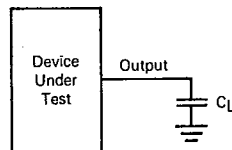
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FIGURE 6
PHASE DETECTOR OUTPUT WAVEFORMS
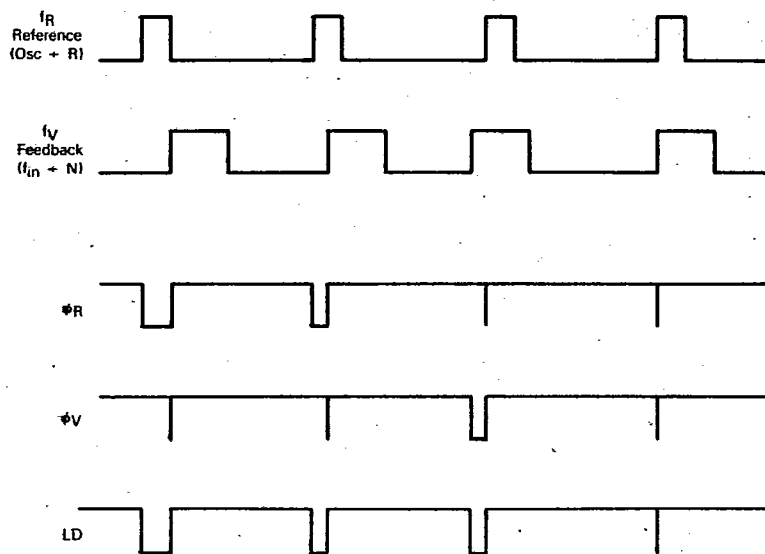
NOTE: The P$_D$ output state is approximately equal to either V$_{DD}$ or V$_{SS}$ when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

RECOMMENDED FOR READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.

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DUAL MODULUS PRESCALING

The technique of dual modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that would otherwise result if a fixed (single modulus) divider was used for the prescaler.

In dual modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). The MC145152-1 contains this feature and can be used with a variety of dual modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷3/÷4 to ÷64/÷65 can be controlled by the MC145152-1.

Several dual modulus prescaler approaches suitable for use with the MC145152-1 are given in Figure 7. The approaches range from the low cost ÷15/÷16, MC3393P device capable of system speeds in excess of 100 MHz to the MC12000 series having capabilities extending to greater than 500 MHz. Synthesizers featuring the MC145152-1 and dual modulus prescaling are shown in Figures 8 and 9 for two typical applications.

DESIGN GUIDELINES APPLICABLE TO THE MC145152-1

The system total divide value (N_{total}) will be dictated by the application. i.e.

$$N_{total} = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷N counter; A is the number programmed into the ÷A counter. P and P + 1 are the two selectable divide ratios available in the two modulus prescalers. To have a range of N_{total} values in sequence, the ÷A counter is programmed from zero through P − 1 for a particular value N in the divide N counter. N is then incremented to N + 1 and the ÷A is sequenced from zero through P − 1 again.

There are minimum and maximum values that can be achieved for N_{total}. These values are a function of P and the size of the ÷N and ÷A counters. The constraint N ≥ A always applies. If $A_{max} = P − 1$ then $N_{min} \geq P − 1$. Then $N_{total − min} = (P − 1) P + A$ or (P − 1) P since A is free to assume the value of zero.

$$N_{total − max} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its modulus control is low.

For the maximum frequency into the prescaler (f_{VCO} max), the value used for P must be large enough such that:

A. f_{VCO} max divided by P may not exceed the frequency capability of Pin 1 of the MC145152-1.

B. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the MC145152-1.

A sometimes useful simplification in the MC145152-1 programming code can be achieved by choosing the values for P of 8, 16, 32 or 64. For these cases, the desired value for N_{total} will result when N_{total} in binary is used as the program code to the ÷N and ÷A counters treated in the following manner:

A. Assume the ÷A counter contains "b" bits where 2^b = P.
B. Always program all higher order ÷A counter bits above "b" to zero.
C. Assume the ÷N counter and the ÷A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10 + b bits in length. The MSB of this "hypothetical" counter is to correspond to the MSB of ÷N and the LSB is to correspond to the LSB of ÷A. The system divide value, N_{total}, now results when the value of N_{total} in binary is used to program the "New" 10 + b bit counter.

FIGURE 7 — HIGH FREQUENCY DUAL MODULUS PRESCALERS FOR USE WITH THE MC145152-1

MC12009	÷5/÷6	440 MHz Min
MC12011	÷8/÷9	500 MHz Min
MC12013	÷10/÷11	500 MHz Min
MC12015	÷32/÷33	225 MHz Min
MC12016	÷40/÷41	225 MHz Min
MC12017	÷64/÷65	225 MHz Min
*MC12018	÷128/÷129	520 MHz Min
MC3393	÷15/÷16	140 MHz Typ

*Proposed introduction

By using two devices, several dual modulus values are achievable:
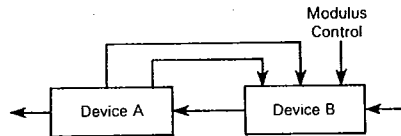
Device A \ Device B	MC12009	MC12011	MC12013
MC10131	÷20/÷21	÷32/÷33	÷40/÷41
MC10138	÷50/÷51	÷80/÷81	÷100/÷101
MC10154	÷40/÷41 or ÷80/÷81	÷64/÷65 or ÷128/÷129	÷80/÷81

NOTE: MC12009, MC12011 and MC12013 are pin equivalent.
   MC12015, MC12016, and MC12017 are pin equivalent.

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FIGURE 8 — AIRCRAFT NAV RECEIVER SYNTHESIZER DEMONSTRATES
A LOW COST DUAL MODULUS SYSTEM EMPLOYING THE MC145152-1
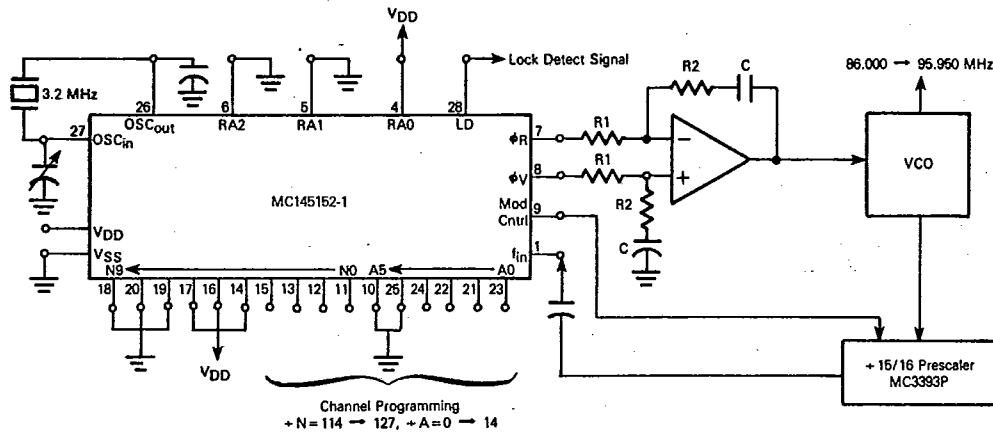
NOTES:
1. $f_R = 50$ kHz, $\div R = 64$; 22.0 MHz low side injection; $N_{TOTAL} = 1720 \rightarrow 1919$.
2. Using 22.0 MHz for the receiver I.F. demonstrates how the choice of I.F. value can sometimes reduce the number of $\div N$ bits that must be programmed. Using the more common 21.4 MHz I.F. would require six rather than four $\div N$ programming inputs.

FIGURE 9 — SYNTHESIZER FOR LAND MOBILE RADIO UHF BAND
COVERAGE DEMONSTRATES USE OF THE MC145152-1
IN SYSTEMS OPERATING TO SEVERAL HUNDRED MHz
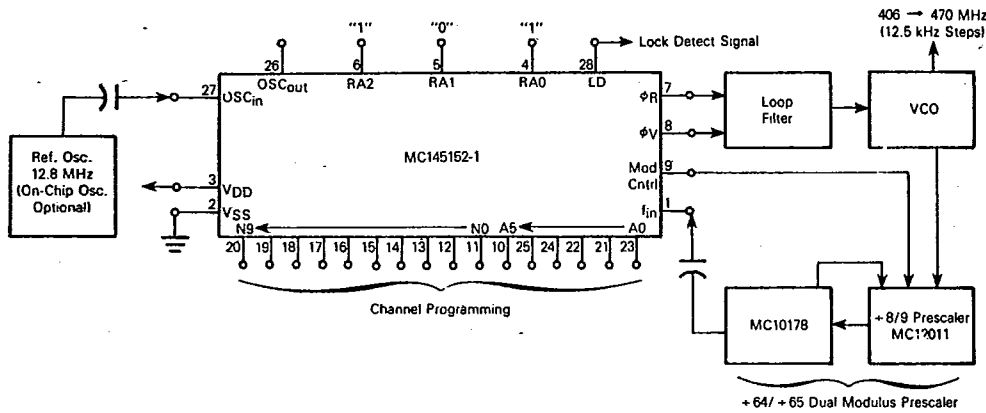
NOTES:
1. $N_{TOTAL} = N \cdot 64 + A = 32480$ to 37600; $N = 507$ to 587; $A = 0$ to 63.
2. $f_R = 12.5$ kHz, $\div R = 1024$ (code 101).
3. The prescaling approach can be chosen for the application to enhance economy e.g., single chip MC3393P to approximately 100 MHz.
   MC12011 or MC12013 with dual flip flop to approximately 250 MHz.
   MC12011 or MC12013 with MC10178 to over 500 MHz.

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CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TXCOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TXCOs and data clock oscillators, please contact: Motorola Inc., Component Products, 2553 N. Edgington St., Franklin Park, IL 60131, phone (312) 451-1000.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12060, MC12061, MC12560, or MC12561 MECL devices. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure A.

For $V_{DD}=5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in

the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1+C2}$$

where C_{in} = 5 pF (see Figure C)
        C_{out} = 6 pF (see Figure C)
        C_a = 5 pF (see Figure C)
        C_O = The crystal's holder capacitance (see Figure B)
        C1 and C2 = External capacitors (see Figure A)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure B. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure A limits the drive level. The use of R1 may not be necessary in some cases; i.e. R1=0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table A.

TABLE A — PARTIAL LIST OF CRYSTAL MANUFACTURERS

NAME	ADDRESS	PHONE
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	1000 Crystal Dr., Ft. Myers, FL 33906	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.
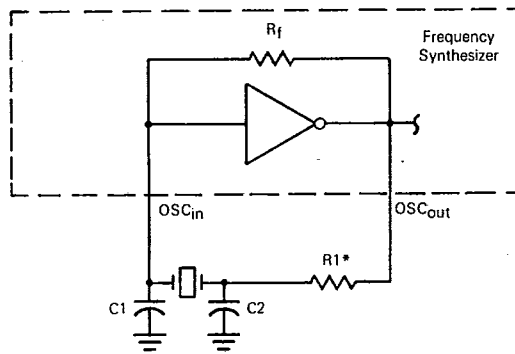
Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June, 1969.

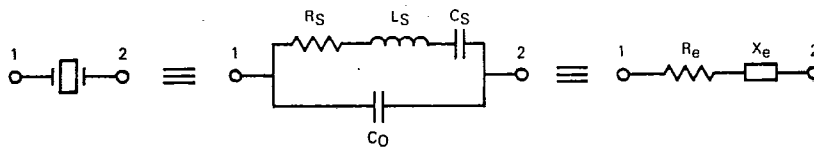P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

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FIGURE A — PIERCE CRYSTAL OSCILLATOR CIRCUIT

* May be deleted in certain cases. See text.

FIGURE B — EQUIVALENT CRYSTAL NETWORKS

Values are supplied by crystal manufacturer (parallel resonant crystal).

FIGURE C — PARASITIC CAPACITANCES
OF THE AMPLIFIER