16K x 4 SRAM
SRAM MEMORY ARRAY

AVAILABLE AS MILITARY SPECIFICATIONS
- SMD 5962-86859
- MIL-STD-883

FEATURES
- High Speed: 12, 15, 20, 25, 35, 45, 55, and 70ns
- Battery Backup: 2V data retention
- High-performance, low-power CMOS double-metal process
- Single +5V (±10%) Power Supply
- Easy memory expansion with CE\
- All inputs and outputs are TTL compatible

OPTIONS MARKING

- **Timing**

12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45*
55ns access	-55*
70ns access	-70*

- **Package(s)**

Ceramic DIP (300 mil)	C	No. 106
Ceramic LCC	EC	No. 204

- **Operating Temperature Ranges**

Industrial (-40°C to +85°C)	IT
Military (-55°C to +125°C)	XT

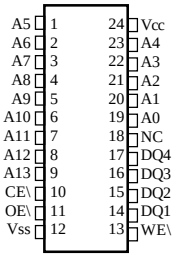
- 2V data retention/low power L

*Electrical characteristics identical to those provided for the 35ns access devices.

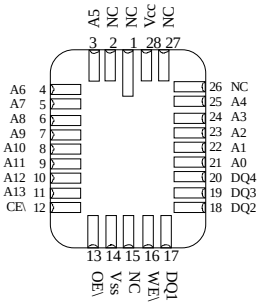
For more products and information please visit our web site at *www.austinsemiconductor.com*

PIN ASSIGNMENT
(Top View)

24-Pin DIP (C)
(300 MIL)



28-Pin LCC (EC)



GENERAL DESCRIPTION

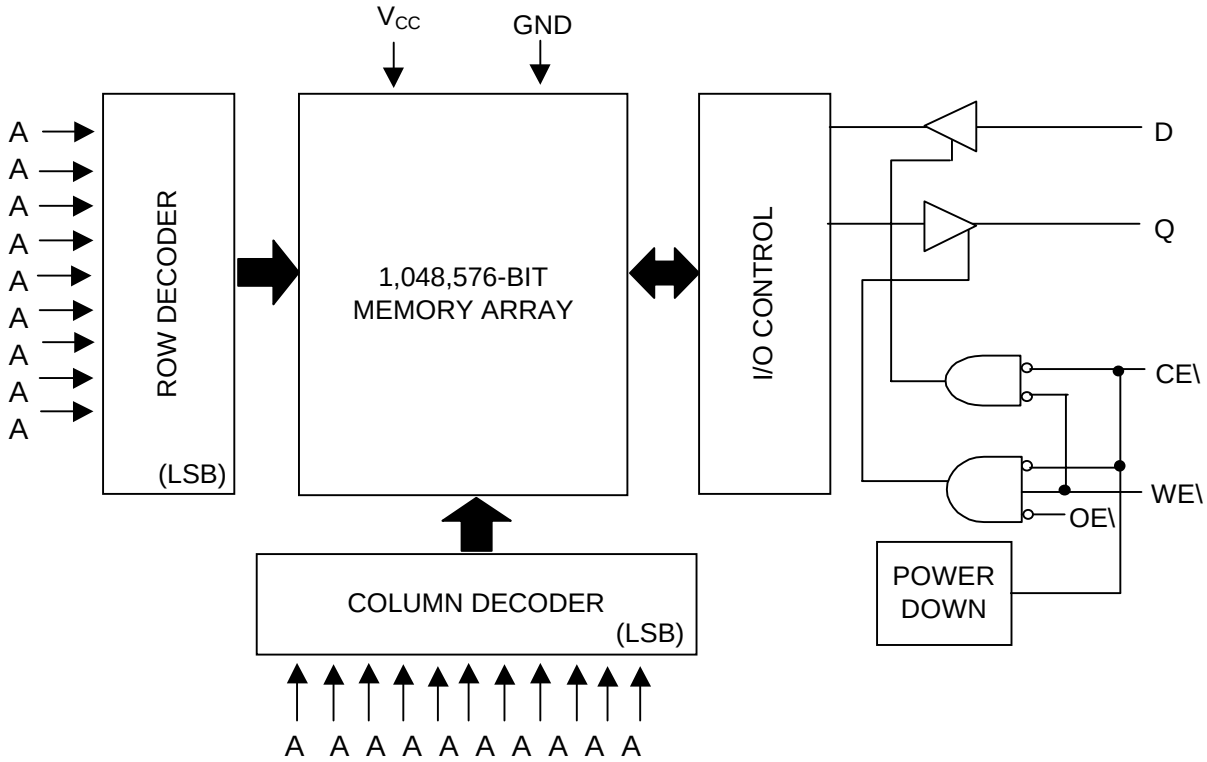
The Austin Semiconductor SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Austin Semiconductor SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Austin Semiconductor offers chip enable (CE\) and output enable (OE\) capability. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH and CE\ and OE\ go LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	OE\	CE\	WE\	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Input or DQ Relative to Vss....-0.5V to +7.0V[1]
Storage Temperature….....-65°C to +150°C
Power Dissipation.....1W
Max Junction Temperature.....+175°C
Lead Temperature (soldering 10 seconds).....+260°C
Short Circuit Output Current.....20mA

1 All voltage referenced to Vss.

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T_C ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYM	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+0.5V	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	IL_I	-10	10	µA	
Output Leakage Current	Outputs Disabled 0V ≤ V_{OUT} ≤ V_{CC}	IL_O	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
PARAMETER	CONDITIONS	SYM	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	CE\ ≤ V_{IL}; V_{CC} = MAX Output Open	I_{CC}	140	125	110	100	90	mA	3
Power Supply Current: Standby	CE\ ≥ V_{IH}; V_{CC} = MAX f = 0 Hz	I_{SBT1}	50	45	40	35	30	mA	
	CE\ ≥ (V_{CC} -0.2); V_{CC} = MAX All Other Inputs ≤ 0.2V or ≥ (V_{CC} - 0.2V), f = 0 Hz	I_{SBC2}	25	25	25	25	25	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYM	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz Vcc = 5V	C_I	8	pF	4
Output Capacitance		C_O	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($-55^{o}C \leq T_C \leq 125^{o}C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYMBOL	-12		-15		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE													
READ cycle time	t_{RC}	12		15		20		25		35		ns	
Address access time	t_{AA}		12		15		20		25		35	ns	
Chip Enable access time	t_{ACE}		12		15		20		25		35	ns	
Output hold from address change	t_{OH}	2		2		2		2		2		ns	
Chip Enable to output in Low-Z	t_{LZCE}	2		2		2		2		2		ns	7
Chip disable to output in High-Z	t_{HZCE}		7		8		10		12		15	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		ns	
Chip disable to power-down time	t_{PD}		12		15		20		25		35	ns	
Output Enable access time	t_{AOE}		6		7		8		10		15	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		8		ns	
Output disable to output in High-Z	t_{HZOE}		6		7		8		10		15	ns	6
WRITE CYCLE													
WRITE cycle time	t_{WC}	12		15		20		25		35		ns	
Chip Enable to end of write	t_{CW}	10		12		15		20		25		ns	
Address valid to end of write	t_{AW}	10		12		15		20		25		ns	
Address setup time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		ns	
WRITE pulse width	t_{WP}	10		12		15		20		25		ns	
Data setup time	t_{DS}	7		8		10		12		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	2		2		2		2		2		ns	7
Write Enable to output in High-Z	t_{HZWE}	0	6	0	7	0	8	0	10	0	15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

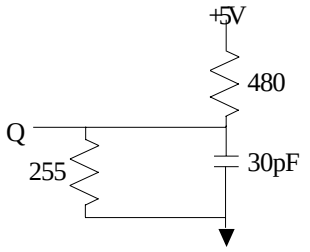


Fig. 1 Output Load Equivalent

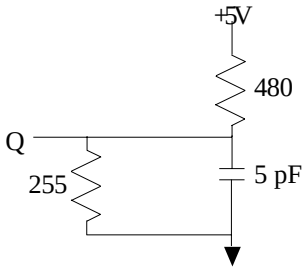


Fig. 2 Output Load Equivalent

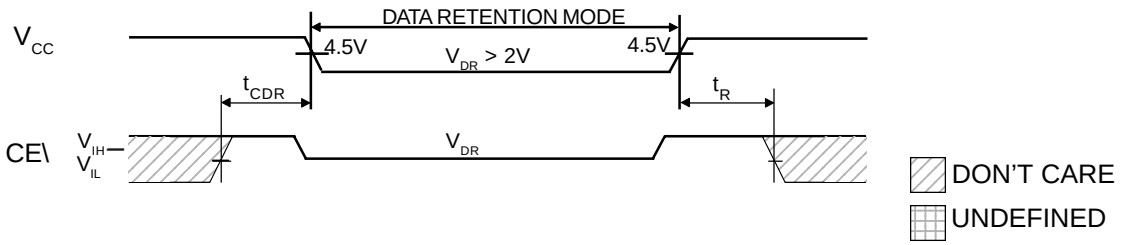
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3V for pulse width < 20ns
3. I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and f = $\frac{1}{t_{RC}\ (MIN)}$ Hz.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV typical from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE}.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC} = Read Cycle Time.
12. CE2 timing is the same as CE1\ timing. The waveform is inverted.

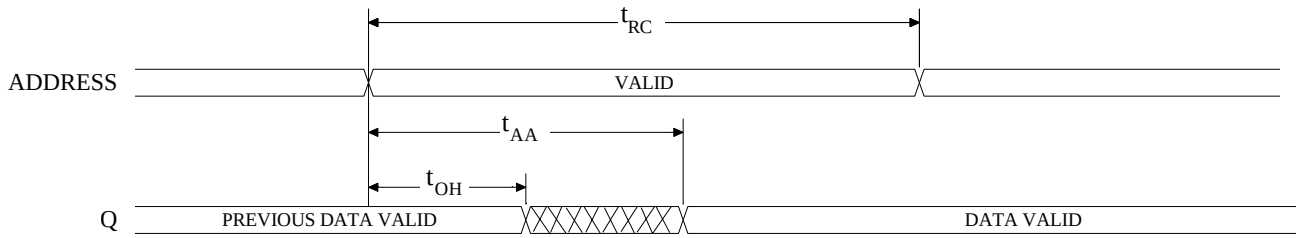
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYM	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2	---	V	
Data Retention Current	CE\ ≥ (V_{CC} - 0.2V) V_{IN} ≥ (V_{CC} - 0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		1	mA	
Chip Deselect to Data Retention Time			t_{CDR}	0	---	ns	4
Operation Recovery Time			t_R	t_{RC}		ns	4, 11

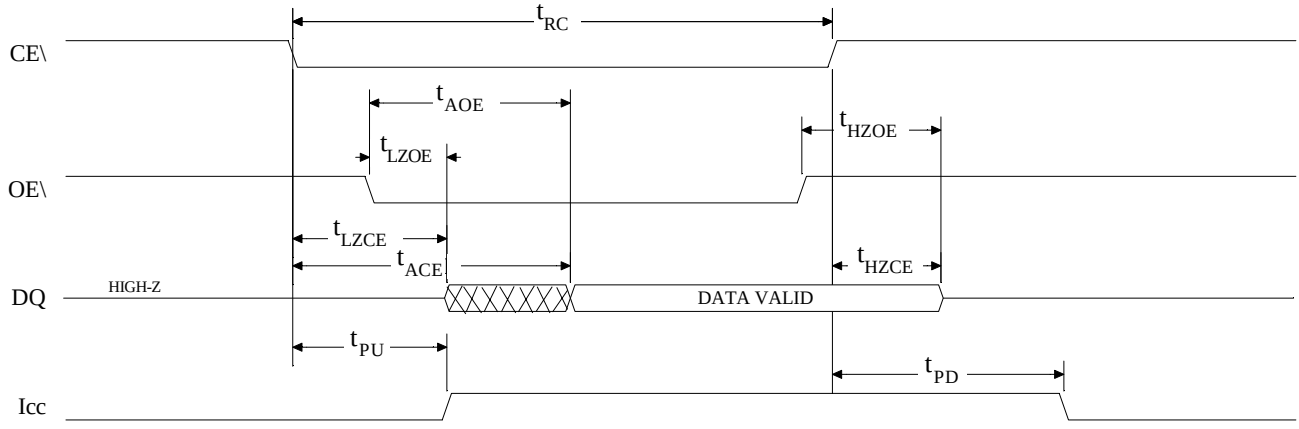
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]

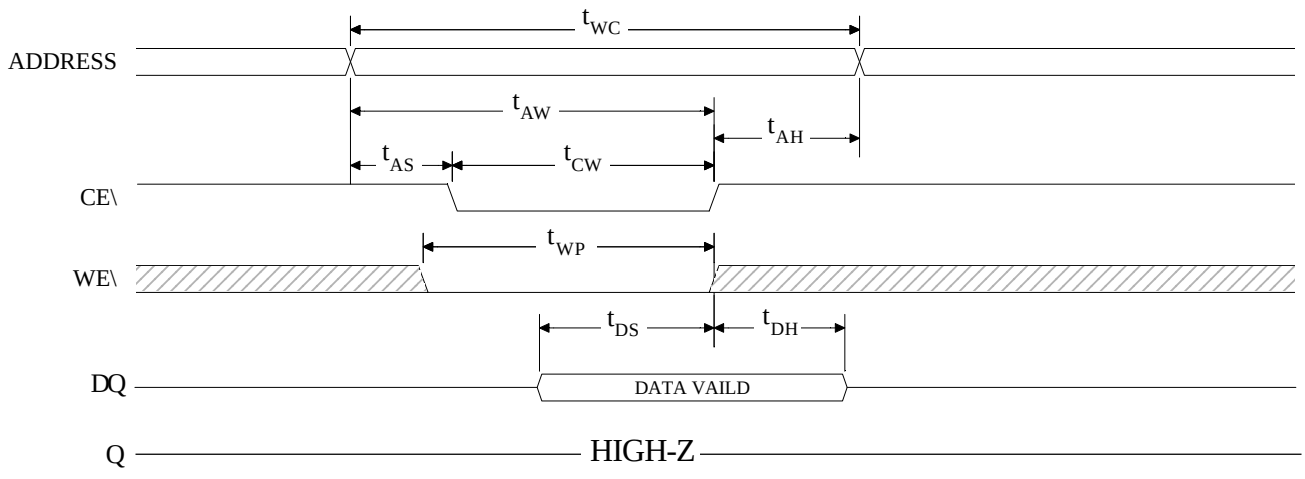


READ CYCLE NO. 2 [7, 8, 10]

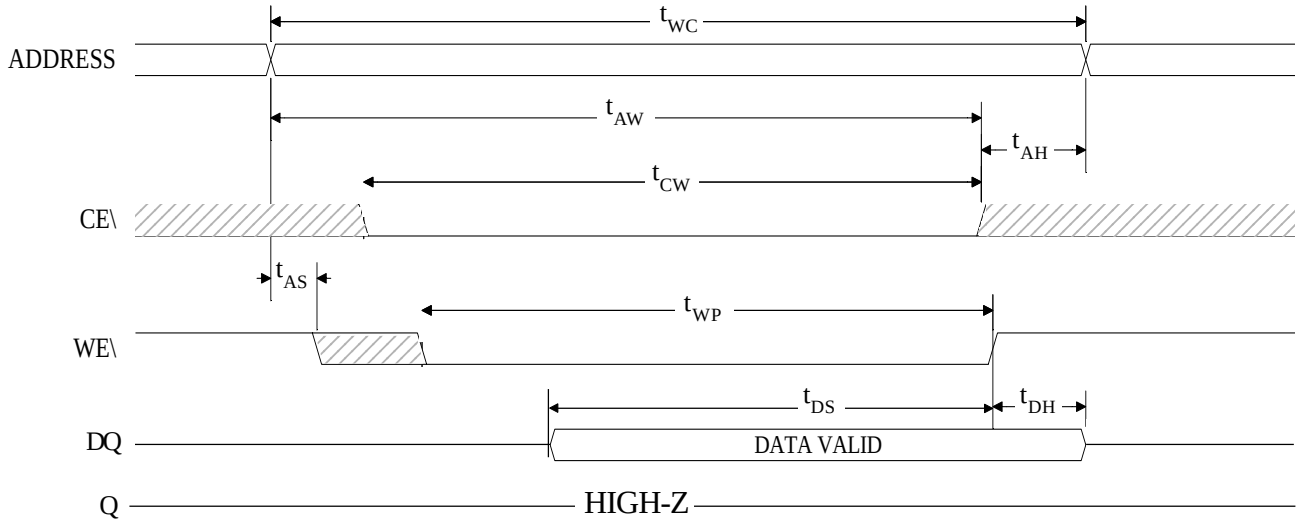


DON'T CARE
UNDEFINED

WRITE CYCLE NO. 1 [12]
(Chip Enabled Controlled)



WRITE CYCLE NO. 2 [7, 12, 13]
(Write Enabled Controlled)



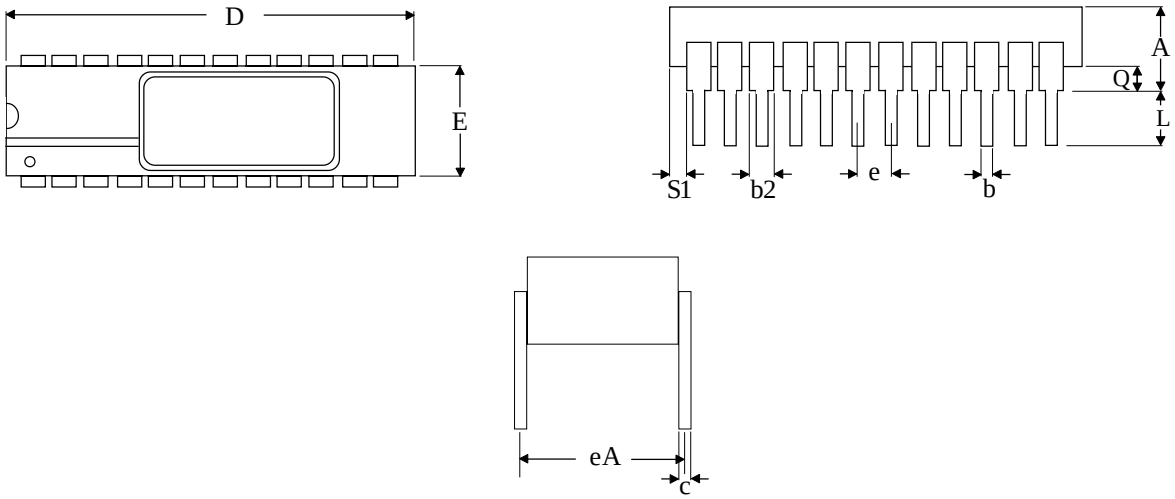
DON'T CARE

UNDEFINED

NOTE: Output enable (OE\) is inactive (HIGH).

MECHANICAL DEFINITIONS*

ASI Case #106 (Package Designator C)
SMD 5962-86859, Case Outline L



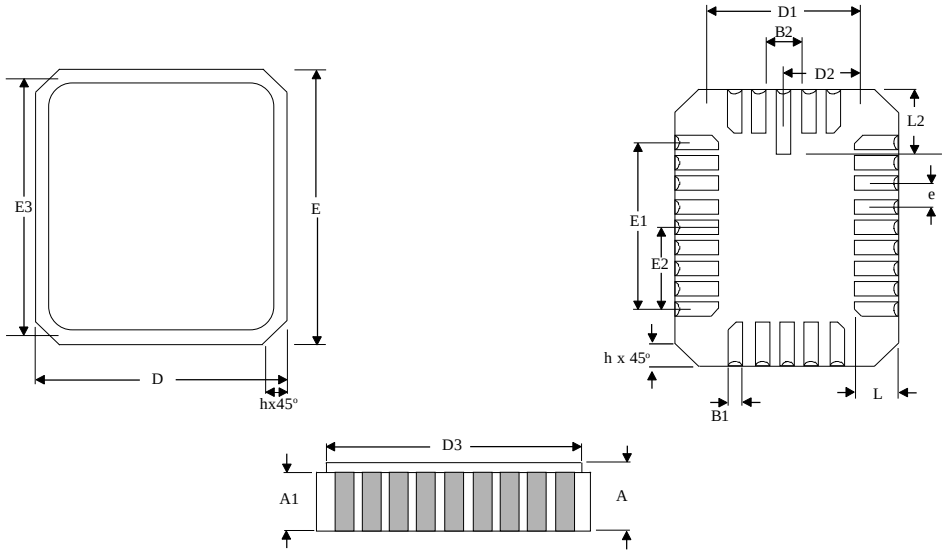
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	---	0.200
b	0.014	0.026
b2	0.045	0.065
c	0.008	0.018
D	---	1.280
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	---

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

**** All measurements are in inches.***

MECHANICAL DEFINITIONS*

ASI Case #204 (Package Designator EC)
SMD 5962-86859, Case Outline U



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
B2	0.072 REF	
D	0.342	0.358
D1	0.200 BSC	
D2	0.100 BSC	
D3	---	0.358
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	---	0.558
e	0.050 BSC	
h	0.040 REF	
L	0.045	0.055
L2	0.075	0.095

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

**** All measurements are in inches.***

ORDERING INFORMATION

EXAMPLE: MT5C6405C-25L/XT

Device Number	Package Type	Speed ns	Options**	Process
MT5C6405	C	-12	L	/*
MT5C6405	C	-15	L	/*
MT5C6405	C	-20	L	/*
MT5C6405	C	-25	L	/*
MT5C6405	C	-35	L	/*
MT5C6405	C	-45	L	/*
MT5C6405	C	-55	L	/*
MT5C6405	C	-70	L	/*

EXAMPLE: MT5C6405EC-15L/IT

Device Number	Package Type	Speed ns	Options**	Process
MT5C6405	EC	-12	L	/*
MT5C6405	EC	-15	L	/*
MT5C6405	EC	-20	L	/*
MT5C6405	EC	-25	L	/*
MT5C6405	EC	-35	L	/*
MT5C6405	EC	-45	L	/*
MT5C6405	EC	-55	L	/*
MT5C6405	EC	-70	L	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range -40°C to +85°C
XT = Extended Temperature Range -55°C to +125°C
883C = Full Military Processing -55°C to +125°C

**** OPTIONS**

L = 2V Data Retention/Low Power

ASI TO DSCC PART NUMBER CROSS REFERENCE*

ASI Package Designator C

ASI Part #	SMD Part #
MT5C6805C-35/883C	5962-8685918LA
MT5C6805C-35L/883C	5962-8685917LA
MT5C6805C-45/883C	5962-8685916LA
MT5C6805C-45L/883C	5962-8685915LA
MT5C6805C-55/883C	5962-8685914LA
MT5C6805C-55L/883C	5962-8685913LA
MT5C6805C-70/883C	5962-8685912LA
MT5C6805C-70L/883C	5962-8685911LA

ASI Package Designator EC

ASI Part #	SMD Part #
MT5C6805EC-35/883C	5962-8685918UA
MT5C6805EC-35L/883C	5962-8685917UA
MT5C6805EC-45/883C	5962-8685916UA
MT5C6805EC-45L/883C	5962-8685915UA
MT5C6805EC-55/883C	5962-8685914UA
MT5C6805EC-55L/883C	5962-8685913UA
MT5C6805EC-70/883C	5962-8685912UA
MT5C6805EC-70L/883C	5962-8685911UA

** ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*