

Features

- High speed access times
Com'l: 12, 15, 17 and 20 ns
Ind'l: 15, 17 and 20 ns
- Low power operation (typical)
 - PDM41027SA
Active: 400 mW
Standby: 150 mW
 - PDM41027LA
Active: 350 mW
Standby: 100 mW
- Single +5V ($\pm 10\%$) power supply
- TTL-compatible inputs and outputs
- Packages
 - Plastic SOJ (400 mil) - SO

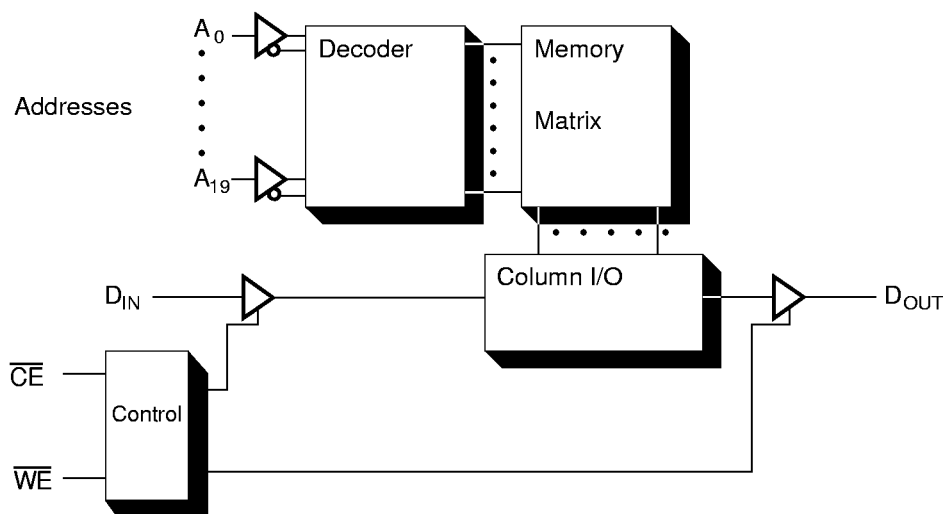
Description

The PDM41027 is a high-performance CMOS static RAM organized as 1,048,576 x 1-bit. Writing is accomplished when the write enable (\overline{WE}) and the chip enable (\overline{CE}) inputs are both LOW. Reading is accomplished when \overline{WE} remains HIGH and \overline{CE} goes LOW.

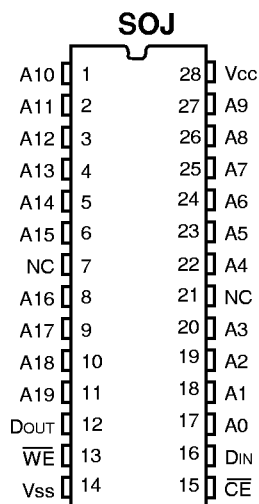
The PDM41027 operates from a single +5V power supply and all the inputs and outputs are fully TTL-compatible. The PDM41027 comes in two versions, the standard power version PDM41027SA and a low power version the PDM41027LA. The two versions are functionally the same and only differ in their power consumption.

The PDM41027 is available in a 28-pin plastic 400-mil plastic SOJ package for surface mount applications.

Functional Block Diagram



Pin Configuration



Pin Description

Name	Description
A19-A0	Address Inputs
D _{IN}	Data Input
D _{OUT}	Data Output
\overline{WE}	Write Enable Input
\overline{CE}	Chip Enable Input
NC	No Connect
V _{CC}	Power (+5V)
V _{SS}	Ground

Truth Table⁽¹⁾

\overline{WE}	\overline{CE}	I/O	MODE
X	H	Hi-Z	Standby
H	L	D _{OUT}	Read
L	L	D _{IN}	Write

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Com'l.	Ind.	Unit
V _{TERM}	Terminal Voltage with Respect to V _{SS}	-0.5 to +7.0	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA
T _J	Maximum Junction Temperature ⁽²⁾	125	145	°C

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Appropriate thermal calculations should be performed in all cases and specifically for those where the chosen package has a large thermal resistance (e.g., TSOP). The calculation should be of the form: $T_j = T_a + P * \theta_{ja}$ where T_a is the ambient temperature, P is average operating power and θ_{ja} the thermal resistance of the package. For this product, use the following θ_{ja} values:

SOJ: 76° C/W
 TSOP: 100° C/W

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{SS}	Supply Voltage	0	0	0	V
Industrial	Ambient Temperature	-40	25	85	°C
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions		PDM41027SA		PDM41027LA		Unit
				Min.	Max.	Min.	Max.	
I _{LI}	Input Leakage Current	V _{CC} = MAX., V _{IN} = V _{SS} to V _{CC}	Com'l/ Ind.	-5	5	-5	5	μA
I _{LO}	Output Leakage Current	V _{CC} = MAX., CE = V _{IH} , V _{OUT} = V _{SS} to V _{CC}	Com'l/ Ind.	-5	5	-5	5	μA
V _{IL}	Input Low Voltage			-0.5 ⁽¹⁾	0.8	-0.5 ⁽¹⁾	0.8	V
V _{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V _{OL}	Output Low Voltage	I _{OL} = 8 mA, V _{CC} = Min.		—	0.4	—	0.4	V
		I _{OL} = 10 mA, V _{CC} = Min.		—	0.5	—	0.5	V
V _{OH}	Output High Voltage	I _{OH} = -4 mA, V _{CC} = Min.		2.4	—	2.4	—	V

NOTE: 1. V_{IL}(min) = -3.0V for pulse width less than 20 ns

Power Supply Characteristics

Symbol	Parameter	Power	-12		-15		-17		-20		Unit
			Com'l	Ind.	Com'l	Ind.	Com'l	Ind.	Com'l	Ind.	
I _{CC}	Operating Current CE = V _{IL} f = f _{MAX} = 1/t _{RC} V _{CC} = Max. I _{OUT} = 0 mA	SA	230	240	185	195	165	185	155	165	mA
		LA	210	220	165	175	155	160	140	150	mA
I _{SB}	Standby Current CE = V _{IH} f = f _{MAX} = 1/t _{RC} V _{CC} = Max.	SA	70	70	55	55	50	50	45	45	mA
		LA	65	65	50	50	45	50	40	40	mA
I _{SB1}	Full Standby Current CE ≥ V _{HC} f = 0 V _{CC} = Max., V _{IN} ≥ V _{CC} - 0.2V or ≤ 0.2V	SA	15	25	10	15	10	15	10	15	mA
		LA	10	10	5	10	5	10	5	10	mA

NOTES: All values are maximum guaranteed values.
V_{LC} ≤ 0.2V, V_{HC} ≥ V_{CC} - 0.2V

Capacitance⁽¹⁾ ($T_A = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	8	pF

NOTE:1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input Pulse Levels	V_{SS} to 3.0V
Input rise and fall times	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

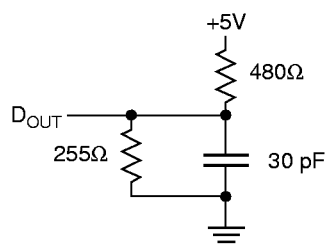


Figure 1. Output Load Equivalent

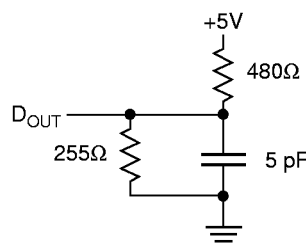
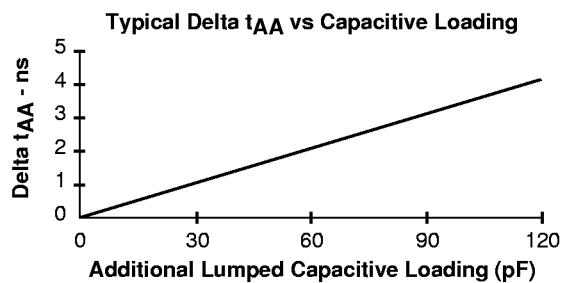
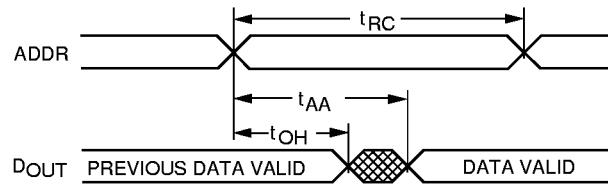


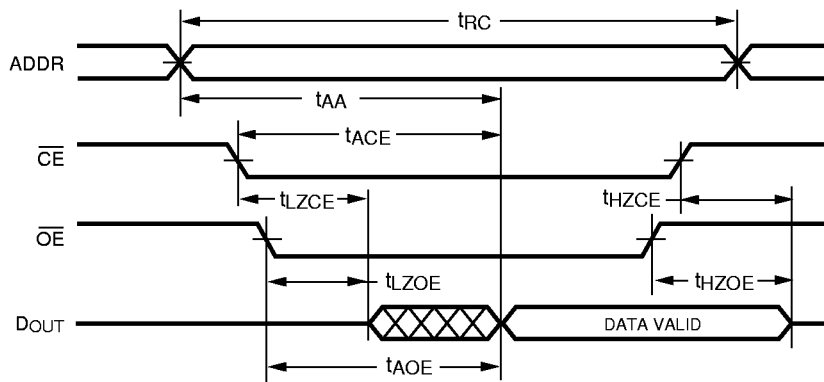
Figure 2. Output Load Equivalent
(for t_{LZCE} , t_{HZCE} , t_{LZWE} , t_{HZWE})



Read Cycle No. 1^(4,5)



Read Cycle No. 2^(2,4,6)

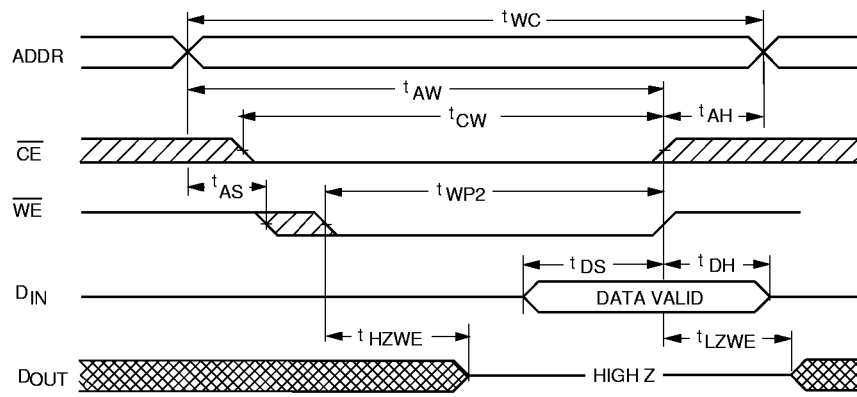


AC Electrical Characteristics

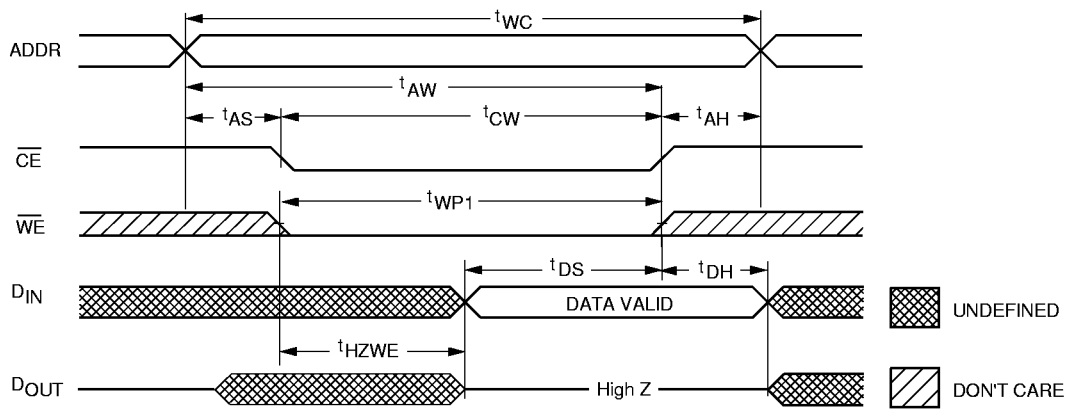
Description		-12 ⁽⁷⁾		-15		-17		-20		
READ Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
READ cycle time	t _{RC}	12		15		17		20		ns
Address access time	t _{AA}		12		15		17		20	ns
Chip enable access time	t _{ACE}		12		15		17		20	ns
Output hold from address change	t _{OH}	3		3		3		3		ns
Chip enable to output in low Z ^(1,3)	t _{LZCE}	5		5		5		5		ns
Chip disable to output in high Z ^(1,2,3)	t _{HZCE}		6		7		7		8	ns
Chip enable to power up time ⁽³⁾	t _{PU}	0		0		0		0		ns
Chip disable to power down time ⁽³⁾	t _{PD}		12		15		17		20	ns

Notes referenced are after Data Retention Table.

Write Cycle No. 1 (Write Enable Controlled)



Write Cycle No. 2 (Chip Enable Controlled)

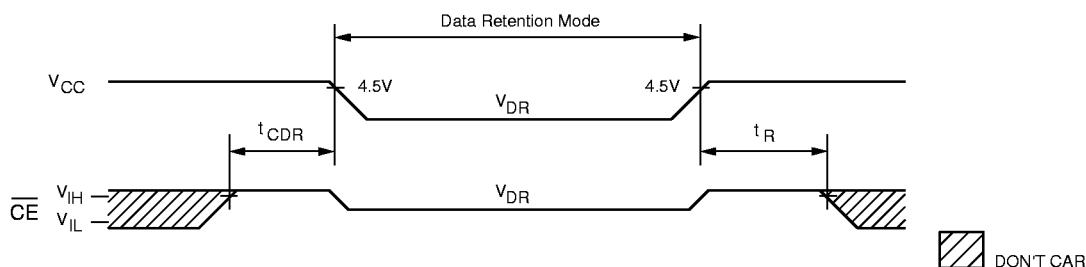


AC Electrical Characteristics

Description	Sym	-12 ⁽⁷⁾		-15		-17		-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE cycle time	t _{WC}	12		15		17		20		ns
Chip enable active time	t _{CW}	10		11		12		13		ns
Address valid to end of write	t _{AW}	10		11		11		13		ns
Address setup time	t _{AS}	0		0		0		0		ns
Address hold from end of write	t _{AH}	0		0		0		0		ns
Write pulse width	t _{WP1}	10		11		12		13		ns
Write pulse width	t _{WP2}	11		12		13		14		ns
Data setup time	t _{DS}	7		7		8		8		ns
Data hold time	t _{DH}	0		0		0		0		ns
Write disable to output in low Z ^(1,3)	t _{LZWE}	0		0		0		0		ns
Write enable to output in high Z ^(1,3)	t _{HZWE}		7		7		8		8	ns

Notes referenced are after Data Retention Table

Low V_{CC} Data Retention Waveform



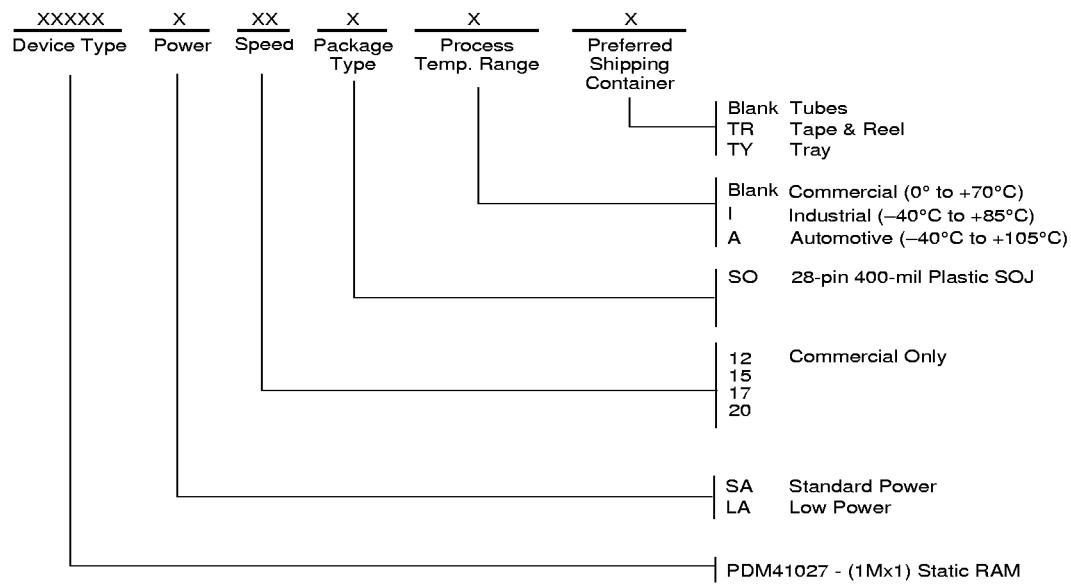
Data Retention Electrical Characteristics (LA Version Only) for JEDEC Version

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{DR}	V _{CC} for Retention Data		2	—	—	V
I _{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	$V_{CC} = 2V$ $V_{CC} = 3V$	— 95 350	500 750	μA μA
t _{CDR}	Chip Deselect to Data Retention Time		0	—	—	ns
t _R ⁽³⁾	Operation Recovery Time		t _{RC} ⁽⁵⁾	—	—	ns

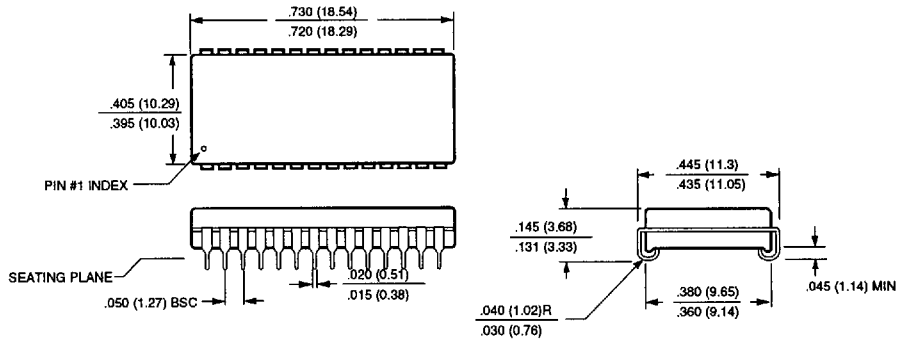
NOTES: (For three previous Electrical Characteristics tables)

1. The parameter is tested with CL = 5 pF as shown in Figure 2. Transition is measured ±200 mV from steady state voltage.
2. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}.
3. This parameter is sampled.
4. \overline{WE} is HIGH for a READ cycle.
5. The device is continuously selected. Chip Enable is held in its active state.
6. The address is valid prior to or coincident with the latest occurring Chip Enable.
7. V_{cc} = 5V ±5%.

Ordering Information

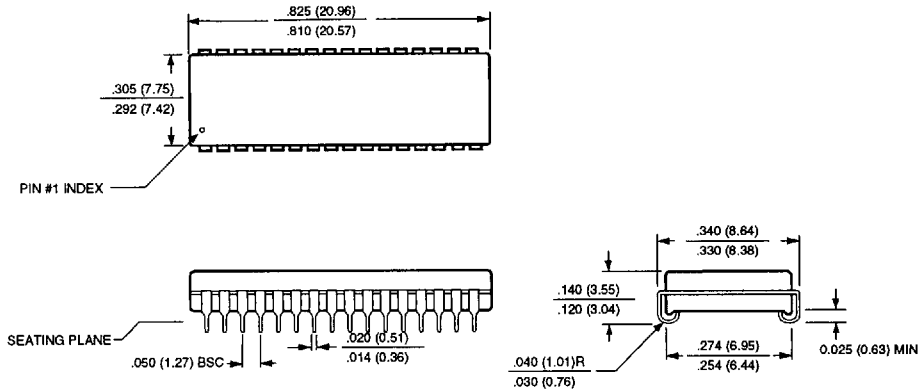


28-pin 400 Mil Plastic SOJ (SO)



All dimensions in inches (millimeters) Max.
Min

32-pin 300 Mil Plastic SOJ (TSO)



All dimensions in inches (millimeters) Max.
Min

10