TA7521P

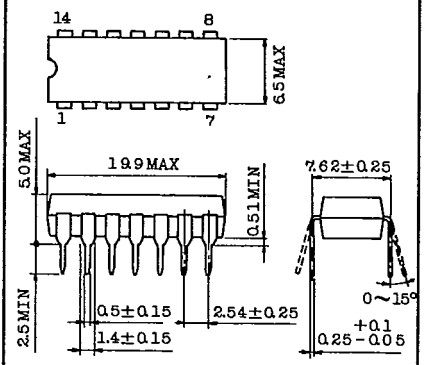
BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

T-73-53

DUAL COMPARATOR
VOLTAGE COMPARATOR

- Tow Circuits/Package
- Possible to operate at +3V Single Supply
- Possible to gain Inverted Output
- Large Common Mode Voltage Range
- Absence of Latch-Up

Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.14 leads.

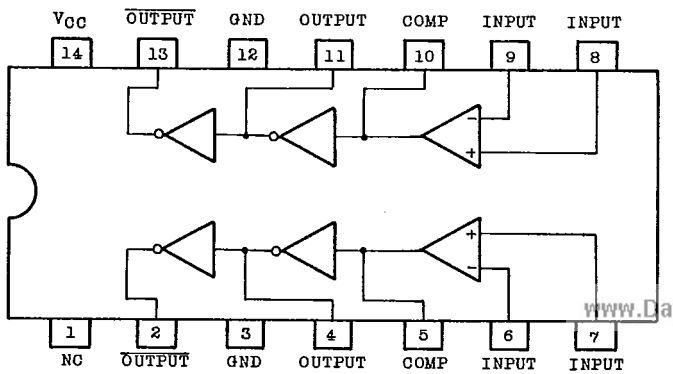
JEDEC	—
TOSHIBA	3D14A-P

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	18	V
Power Dissipation	P_D	300	mW
Differential Input Voltage	DV_{IN}	±18	V
Common Mode Input Voltage	CMV_{IN}	$+V_{CC}$ ~ -5	V
Sink Current	I_{sink}	20	mA
Operating Temperature	T_{opr}	-40 ~ 85	°C
Storage Temperature	T_{stg}	-55 ~ 125	°C

PIN CONNECTION (TOP VIEW)

COMP : FREQUENCY COMPENSATION TERMINAL



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RECOMMENDED CONDITION

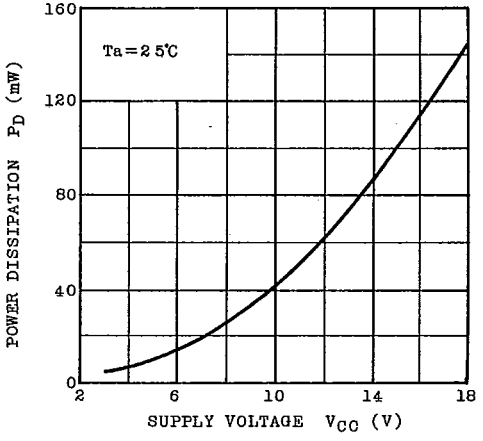
Supply Voltage	5 ~ 12	V
Common Mode Input Voltage	1 ~ (V_{CC}-0.5)	V
Sink Current	10	mA

ELECTRICAL CHARACTERISTICS (V_{CC}=6V, Ta=25°C)

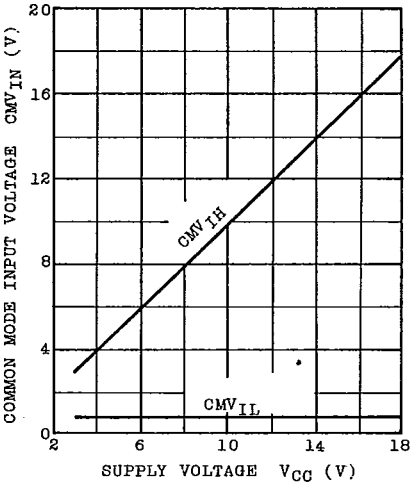
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage		V_{IO}	-	$R_S \leqq 100\Omega$	-	1	5	mV
Input Offset Current		I_{IO}	-	-	-	15	50	nA
Input Bias Current		I_I	-	-	-	120	300	nA
Voltage Gain		$G_{\overline{V}}$	-	$R_L \geqq 1k\Omega$, f=100Hz	75	85	-	dB
		$G_{\overline{V}}^{\ddagger}$	-	$R_L \geqq 1k\Omega$, f=100Hz	80	95	-	dB
Output Voltage	"H" Level	V_{OH}	-	I_{OH}=-2mA	4.6	5.1	-	V
	"L" Level	V_{OL}	-	I_{OL}=10mA	-	0.2	0.4	V
Common Mode Input Voltage	"H" Level	$CMV_{IN(H)}$	-	-	5.8	5.9	-	V
	"L" Level	$CMV_{IN(L)}$	-	-	-	0.8	0.9	V
Common Mode Input Signal Rejection Ratio		CMRR	-	f=100Hz	80	90	-	dB
Power Dissipation		P_D	-	-	-	15	25	mW

Note: $G_{\overline{V}}$: Inverted output voltage gain.

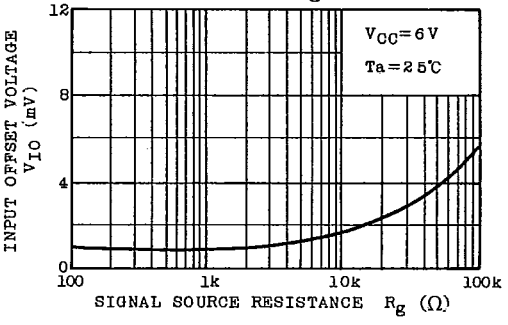
$P_D - V_{CC}$



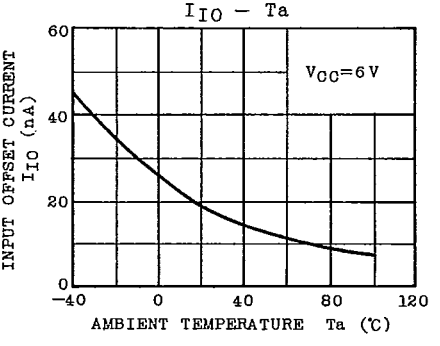
$CMV_{IN} - V_{CC}$



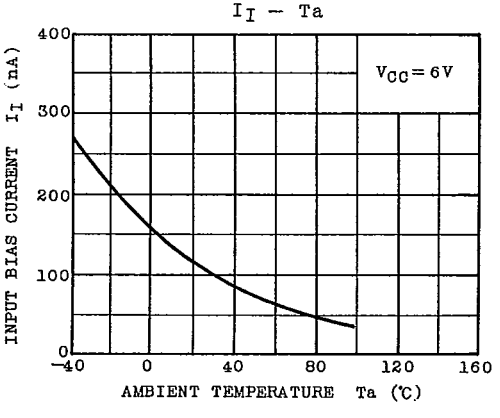
$V_{IO} - R_g$



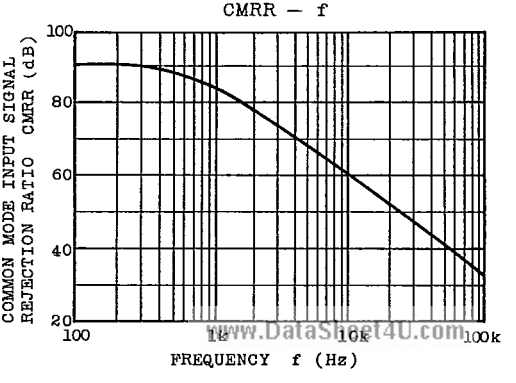
$I_{IO} - Ta$



$I_I - Ta$



CMRR — f



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FREQUENCY CHARACTERISTICS OF OPEN LOOP GAIN