DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD703078Y, 703079Y, 70F3079Y

V850/SF1™
32-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD703078Y, 703079Y, and 70F3079Y (V850/SF1) are 32-bit single-chip microcontrollers of the V850 Series™ for AV equipment. A 32-bit CPU, ROM, RAM, timer/counters, serial interfaces, an A/D converter, DMA controller, and FCAN controller are integrated on a single chip.

The μPD70F3079Y has flash memory in place of the internal mask ROM of the μPD703078Y and 703079Y. Because flash memory allows the program to be written and erased electrically with the device mounted on the board, these products are ideal for the evaluation stages of system development, small-scale production of a variety of products, and rapid development of new products.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850/SF1 Hardware User's Manual: U14665E
V850 Series Architecture User's Manual: U10243E

FEATURES

- Number of instructions: 74
- Minimum instruction execution time: 62.5 ns (16 MHz internal operation)
- General-purpose registers: 32 bits × 32 registers
- Instruction set: Signed multiplication, saturation operations, 32-bit shift instructions, bit manipulation instructions, load/store instructions
- Memory space: 16 MB linear address space
- Internal memory ROM: 256 KB (μPD703078Y, 703079Y: mask ROM)
  256 KB (μPD70F3079Y: flash memory)
  RAM: 16 KB (μPD703078Y, 703079Y, 70F3079Y)
- Interrupt/exception: μPD703078Y (external: 8, internal: 35 sources, exception: 1 source)
  μPD703079Y, 70F3079Y (external: 8, internal: 38 sources, exception: 1 source)
- I/O lines Total: 83
- Timer/counters: 16-bit timer (3 channels: TM0, TM1, TM7)
  8-bit timer (5 channels: TM2 to TM6)
- Watch timer: 1 channel
- Watchdog timer: 1 channel
- Serial interface
  - Asynchronous serial interface (UART0, UART1)
  - Clocked serial interface (CSI0, CSI1, CSI3)
  - 3-wire variable length serial interface (CSI4)
  - I^2C bus interface (I^2C0)

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The mark ★ shows major revised points.

- ○ 10-bit resolution A/D converter: 12 channels
- ○ DMA controller: 6 channels
- ★ ○ Regulator: 3.5 to 5.5 V input → internal 3.0 V (μPD703078Y, 703079Y)
  4.0 to 5.5 V input → internal 3.0 V (μPD70F3079Y)
- ○ ROM correction: 4 places can be corrected
- ○ Power-saving function: HALT/IDLE/STOP modes
- ○ Motor vehicle LAN (FCAN controller): 2 ch (μPD703079Y, 70F3079Y)
  1 ch (μPD703078Y)
- ○ Packages: 100-pin plastic LQFP (fine pitch) (14 × 14)
  100-pin plastic QFP (14 × 20)
- ○ μPD70F3079Y
  - Can be replaced with μPD703078Y and 703079Y (internal mask ROM) in mass production

APPLICATIONS

- ○ AV equipment (car audio, etc.)

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD703078YGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Mask ROM
μPD703078YGF-×××-3BA[Note]	100-pin plastic QFP (14 × 20)	Mask ROM
μPD703079YGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Mask ROM
μPD703079YGF-×××-3BA[Note]	100-pin plastic QFP (14 × 20)	Mask ROM
μPD70F3079YGC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Flash memory
μPD70F3079YGF-3BA[Note]	100-pin plastic QFP (14 × 20)	Flash memory

Note Under development

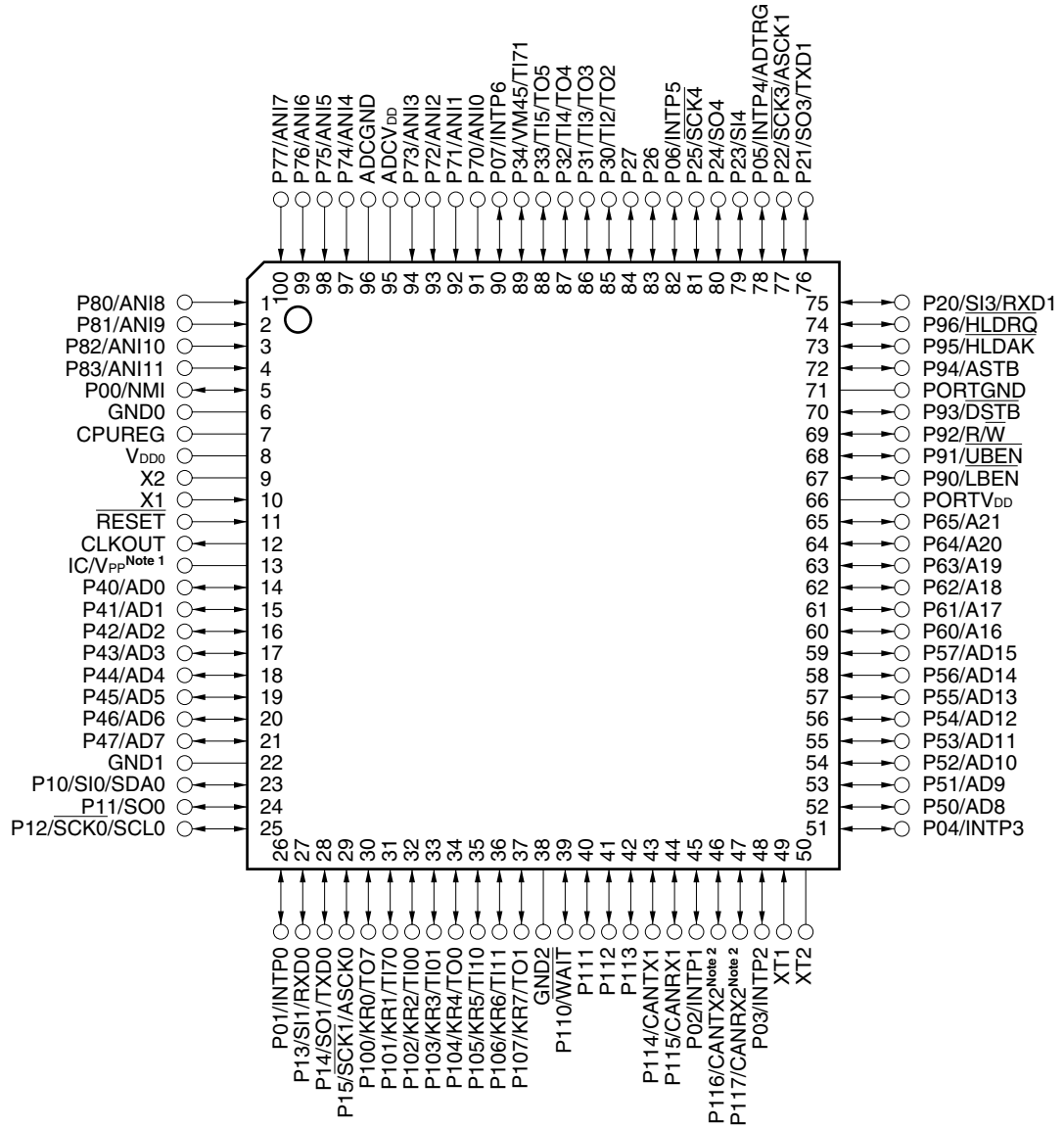
Remarks 1. ××× indicates ROM code suffix.

2. ROMless versions are not provided.

PIN CONFIGURATION (Top View)

100-pin plastic LQFP (fine pitch) (14 × 14)

- μPD703078YGC-×××-8EU
- μPD703079YGC-×××-8EU
- μPD70F3079YGC-8EU

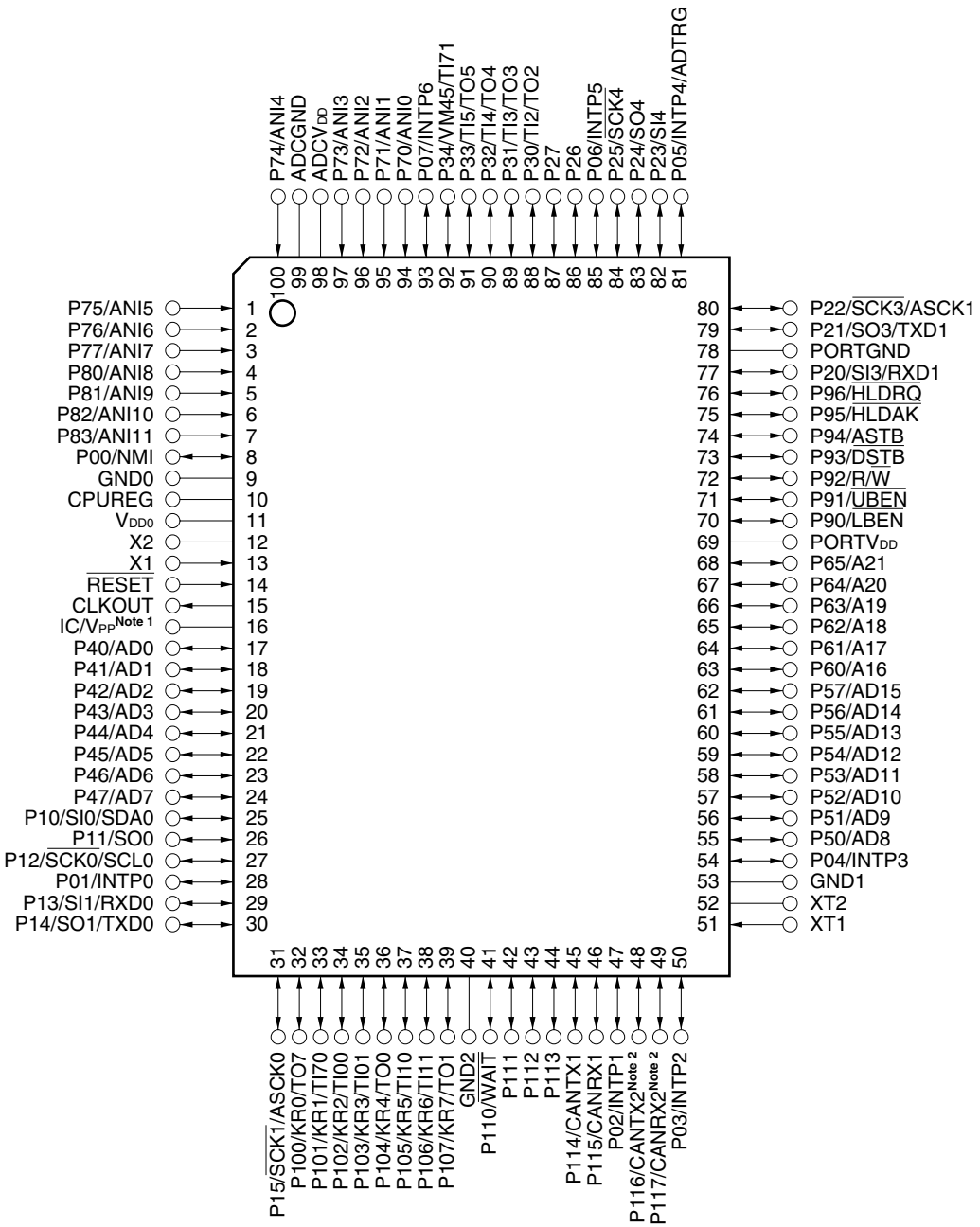


Notes 1. IC: Connect directly to VSS (μPD703078Y, 703079Y).
VPP: Connect to GND0 to GND2 in normal operation mode (μPD70F3079Y).

2. CANTX2 and CANRX2 are available only in the μPD703079Y and 70F3079Y.

100-pin plastic QFP (14 × 20)

- μPD703078YGF-×××-3BA
- μPD703079YGF-×××-3BA
- μPD70F3079YGF-3BA



Notes 1. IC: Connect directly to VSS (μPD703078Y, 703079Y).

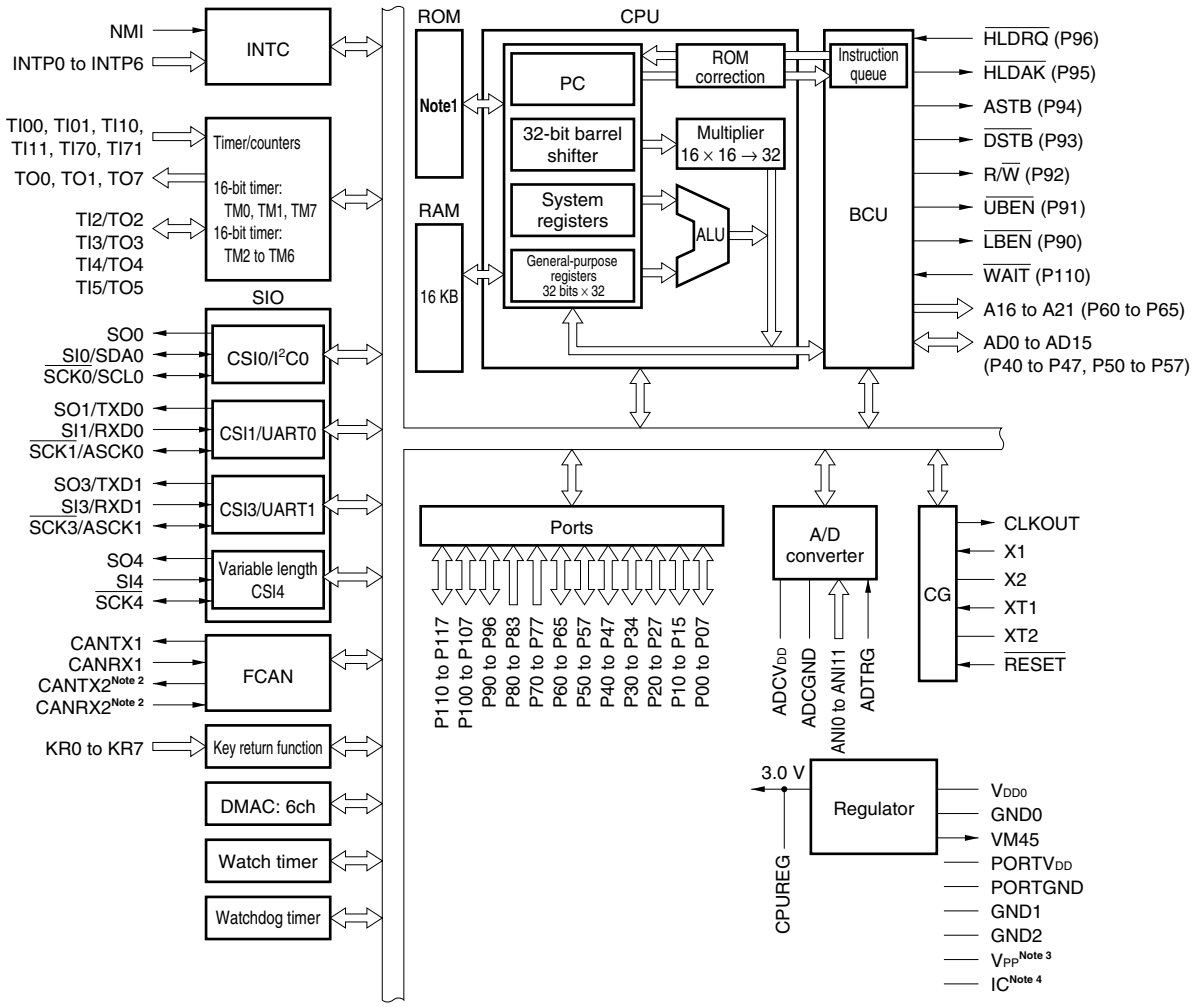
VPP: Connect to GND0 to GND2 in normal operation mode (μPD70F3079Y).

2. CANTX2 and CANRX2 are available only in the μPD703079Y and 70F3079Y.

PIN IDENTIFICATION

A16 to A21:	Address bus	P50 to P57:	Port 5
AD0 to AD15:	Address/data bus	P60 to P65:	Port 6
ADCGND:	Ground for analog	P70 to P77:	Port 7
$ADCV_{DD}$	Power supply for analog	P80 to P83:	Port 8
ADTRG:	A/D trigger input	P90 to P96:	Port 9
ANI0 to ANI11:	Analog input	P100 to P107:	Port 10
ASCK0, ASCK1:	Asynchronous serial clock	P110 to P117:	Port 11
ASTB:	Address strobe	$\overline{RESET}$:	Reset
CANRX1, CANRX2:	FCAN receive data	R/$\overline{W}$:	Read/write status
CANTX1, CANTX2:	FCAN transmit data	RXD0, RXD1:	Receive data
CLKOUT:	Clock output	$\overline{SCK0}$, $\overline{SCK1}$,	
CPUREG:	Regulator control	$\overline{SCK3}$, $\overline{SCK4}$:	Serial clock
$\overline{DSTB}$:	Data strobe	SCL0:	Serial clock
GND0, GND1,		SDA0:	Serial data
GND2:	Ground	SI0, SI1, SI3, SI4:	Serial input
$\overline{HLDAK}$:	Hold acknowledge	SO0, SO1, SO3,	
$\overline{HLDRQ}$:	Hold request	SO4:	Serial output
IC:	Internally connected	TI00, TI01, TI10,	
INTP0 to INTP6:	Interrupt request from peripherals	TI11, TI2 to TI5,	
KR0 to KR7:	Key return	TI70, TI71:	Timer input
$\overline{LBEN}$:	Lower byte enable	TO0 to TO5, TO7:	Timer output
NMI:	Non-maskable interrupt request	TXD0, TXD1:	Transmit data
PORTGND:	Ground for port	$\overline{UBEN}$:	Upper byte enable
$PORTV_{DD1}$	Power supply for port	V_{DD0}:	Power supply
P00 to P07:	Port 0	VM45:	V_{DD} = 4.5 V monitor output
P10 to P15:	Port 1	V_{PP}:	Programming power supply
P20 to P27:	Port 2	$\overline{WAIT}$:	Wait
P30 to P34:	Port 3	X1, X2:	Crystal for main clock
P40 to P47:	Port 4	XT1, XT2:	Crystal for subclock

INTERNAL BLOCK DIAGRAM



Notes 1. μPD703078Y, 703079Y: 256 KB (mask ROM)
μPD70F3079Y: 256 KB (flash memory)

2. μPD7030379Y, 70F3079Y only

3. μPD70F3079Y only

4. μPD703078Y, 703079Y only

CONTENTS

1. DIFFERENCES BETWEEN PRODUCTS

Product Name		ROM		RAM Size	I^2C	FCAN
Common Name	Part Number	Type	Size			
V850/SF1	μPD703078Y	Mask ROM	256 KB	16 KB	I^2C incorporated	1 channel
	μPD703079Y					2 channels
	μPD70F3079Y	Flash memory				

Cautions 1. There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

2. When replacing the flash memory versions with mask ROM versions, write the same code in the empty area of the internal ROM.

2. PIN FUNCTIONS

2.1 Port Pins

(1/3)

Pin Name	I/O	PULL	Function	Alternate Function
P00	I/O	No	Port 0 8-bit I/O port Input/output can be specified in 1-bit units.	NMI
P01				INTP0
P02				INTP1
P03				INTP2
P04				INTP3
P05				INTP4/ADTRG
P06				INTP5
P07				INTP6
P10	I/O	No	Port 1 6-bit I/O port Input/output can be specified in 1-bit units.	SI0/SDA0
P11				SO0
P12				$\overline{\text{SCK0}}$/SCL0
P13				SI1/RXD0
P14				SO1/TXD0
P15				$\overline{\text{SCK1}}$/ASCK0
P20	I/O	No	Port 2 8-bit I/O port Input/output can be specified in 1-bit units.	SI3/RXD1
P21				SO3/TXD1
P22				$\overline{\text{SCK3}}$/ASCK1
P23				SI4
P24				SO4
P25				$\overline{\text{SCK4}}$
P26				–
P27				–
P30	I/O	No	Port 3 5-bit I/O port Input/output can be specified in 1-bit units.	TI2/TO2
P31				TI3/TO3
P32				TI4/TO4
P33				TI5/TO5
P34				VM45/TI71
P40	I/O	No	Port 4 8-bit I/O port Input/output can be specified in 1-bit units.	AD0
P41				AD1
P42				AD2
P43				AD3
P44				AD4
P45				AD5
P46				AD6
P47				AD7

Remark PULL: On-chip pull-up resistor

(2/3)

Pin Name	I/O	PULL	Function	Alternate Function
P50	I/O	No	Port 5 8-bit I/O port Input/output can be specified in 1-bit units.	AD8
P51				AD9
P52				AD10
P53				AD11
P54				AD12
P55				AD13
P56				AD14
P57				AD15
P60	I/O	No	Port 6 6-bit I/O port Input/output can be specified in 1-bit units.	A16
P61				A17
P62				A18
P63				A19
P64				A20
P65				A21
P70	Input	No	Port 7 8-bit input port	ANI0
P71				ANI1
P72				ANI2
P73				ANI3
P74				ANI4
P75				ANI5
P76				ANI6
P77				ANI7
P80	Input	No	Port 8 4-bit input port	ANI8
P81				ANI9
P82				ANI10
P83				ANI11
P90	I/O	No	Port 9 7-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{LBEN}}$
P91				$\overline{\text{UBEN}}$
P92				R/$\overline{\text{W}}$
P93				$\overline{\text{DSTB}}$
P94				ASTB
P95				$\overline{\text{HLDAK}}$
P96				$\overline{\text{HLDRQ}}$

Remark PULL: On-chip pull-up resistor

(3/3)

Pin Name	I/O	PULL	Function	Alternate Function
P100	I/O	Yes	Port 10 8-bit I/O port Input/output can be specified in 1-bit units.	KR0/TO7
P101				KR1/TI7
P102				KR2/TI00
P103				KR3/TI01
P104				KR4/TO0
P105				KR5/TI10
P106				KR6/TI11
P107				KR7/TO1
P110	I/O	No	Port 11 8-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{WAIT}}$
P111				–
P112				–
P113				–
P114				CANTX1
P115				CANRX1
P116				CANTX2[Note]
P117				CANRX2[Note]

Note Only for the μPD703079Y, 70F3079Y

Remark PULL: On-chip pull-up resistor

2.2 Non-Port Pins

(1/3)

Pin Name	I/O	PULL	Function	Alternate Function
A16 to A21	Output	No	Higher address bus used for external memory expansion	P60 to P65
AD0 to AD7	I/O	No	16-bit multiplexed address/data bus used for external memory expansion	P40 to P47
AD8 to AD15				P50 to P57
ADCGND	–	–	Ground potential for A/D converter	–
$ADCV_{DD}$	–	–	Power supply pin and reference voltage pin for A/D converter	–
ADTRG	Input	No	A/D converter external trigger input	P05/INTP4
ANI0 to ANI7	Input	No	Analog input to A/D converter	P70 to P77
ANI8 to ANI11				P80 to P83
ASCK0	Input	No	Baud rate clock input for UART0 and UART1	P15/$\overline{SCK1}$
ASCK1				P22/$\overline{SCK3}$
ASTB	Output	No	External address strobe signal output	P94
CANRX1	Input	No	CAN1 receive data input	P115
CANRX2	Input		CAN2 receive data input (μPD703079Y and 70F3079Y only)	P117
CANTX1	Output		CAN1 transmit data output	P114
CANTX2	Output		CAN2 transmit data output (μPD703079Y and 70F3079Y only)	P116
CLKOUT	Output	–	Internal system clock output	–
CPUREG	–	–	Connection of regulator output stabilize capacitance	–
$\overline{DSTB}$	Output	No	External data strobe signal output	P93
GND0 to GND2	–	–	Ground potential	–
$\overline{HLDAK}$	Output	No	Bus hold acknowledge output	P95
$\overline{HLDRQ}$	Input	No	Bus hold request input	P96
IC	–	–	Internally connected (μPD703078Y and 703079Y only)	–
INTP0 to INTP3	Input	No	External interrupt request input (analog noise elimination)	P01 to P04
INTP4			External interrupt request input (digital noise elimination)	P05/ADTRG
INTP5				P06
INTP6			External interrupt request input (digital noise elimination for remote control)	P07
KR0	Input	Yes	Key return input	P100/TO7
KR1				P101/TI70
KR2				P102/TI00
KR3				P103/TI01
KR4				P104/TO0
KR5				P105/TI10
KR6				P106/TI11
KR7				P107/TI01
$\overline{LBEN}$	Output	No	External data bus's lower byte enable signal output	P90
NMI	Input	No	Non-maskable interrupt request input	P00
PORTGND	–	–	Ground potential for port output	–
$PORTV_{DD}$	–	–	Positive power supply for port output	–

Remark PULL: On-chip pull-up resistor

(2/3)

Pin Name	I/O	PULL	Function	Alternate Function
$\overline{\text{RESET}}$	Input	–	System reset input	–
R/$\overline{\text{W}}$	Output	No	External read/write status	P92/$\overline{\text{WRH}}$
RXD0	Input	No	Serial receive data input for UART0 and UART1	P13/SI1
RXD1				P20/SI3
$\overline{\text{SCK0}}$	I/O	No	Serial clock I/O for CSI0, CSI1, CSI3 (3-wire type)	P12/SCL0
$\overline{\text{SCK1}}$				P15/ASCK0
$\overline{\text{SCK3}}$				P22/ASCK1
$\overline{\text{SCK4}}$			Serial clock I/O for variable-length CSI4 (3-wire type)	P25
SCL0	I/O	No	Serial clock I/O for I^2C0	P12/$\overline{\text{SCK0}}$
SDA0	I/O	No	Serial transmit/receive data I/O for I^2C0	P10/SI0
SI0	Input	No	Serial receive data input for CSI0, CSI1, CSI3 (3-wire type)	P10/SDA0
SI1				P13/RXD0
SI3				P20/RXD1
SI4			Serial receive data input for variable-length CSI4 (3-wire type)	P23
SO0	Output	No	Serial transmit data output for CSI0, CSI1, CSI3 (3-wire type)	P11
SO1				P14/TXD0
SO3				P21/TXD1
SO4			Serial transmit data output for variable-length CSI4 (3-wire type)	P24
TI00	Input	Yes	External count clock input/external capture trigger input for TM0	P102/KR2
TI01			External capture trigger input for TM0	P103/KR3
TI10			External count clock input/external capture trigger input for TM1	P105/KR5
TI11			External capture trigger input for TM1	P106/KR6
TI2		No	External count clock input for TM2	P30/TO2
TI3			External count clock input for TM3	P31/TO3
TI4			External count clock input for TM4	P32/TO4
TI5			External count clock input for TM5	P33/TO5
TI70		Yes	External count clock input/external capture trigger input for TM7	P101/KR1
TI71		No	External capture trigger input for TM7	P34/VM45
TO0	Output	Yes	Pulse signal output for TM0	P104/KR4
TO1			Pulse signal output for TM1	P107/KR7
TO2		No	Pulse signal output for TM2	P30/TI2
TO3			Pulse signal output for TM3	P31/TI3
TO4			Pulse signal output for TM4	P32/TI4
TO5			Pulse signal output for TM5	P33/TI5
TO7		Yes	Pulse signal output for TM7	P100/KR0
TXD0	Output	No	Serial transmit data output for UART0 and UART1	P14/SO1
TXD1				P24/SO3

Remark PULL: On-chip pull-up resistor

(3/3)

Pin Name	I/O	PULL	Function	Alternate Function
$\overline{\text{UBEN}}$	Output	No	Higher byte enable signal output for external data bus	P91
V_{DD0}	–	–	Positive power supply pin	–
VM45	Output	No	V_{DD} = 4.5 V monitor output	P34/TI71
V_{PP}	–	–	High-voltage apply pin for program write/verify (μPD70F3079Y only)	–
$\overline{\text{WAIT}}$	Input	Yes	Control signal input for inserting wait in bus cycle	P110
X1	Input	No	Resonator connection for main clock	–
X2	–			–
XT1	Input	No	Resonator connection for subsystem clock	–
XT2	–			–

Remark PULL: On-chip pull-up resistor

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 2-1. For the I/O schematic circuit diagram of each type, refer to Figure 2-1.

Table 2-1. Types of Pin I/O Circuits and Connection of Unused Pins (1/2)

Pin	Alternate Function	I/O Circuit Type	I/O Buffer Power Supply	Recommended Connection of Unused Pins
P00	NMI	8	PORTV$_{DD}$	Input: Individually connect to PORTV$_{DD}$ or PORTGND via a resistor. Output: Leave open.
P01 to P04	INTP0 to INTP3			
P05	INTP4/ADTRG			
P06, P07	INTP5, INTP6			
P10	SI0/SDA0	10	PORTV$_{DD}$	
P11	SO0	5		
P12	$\overline{\text{SCK0}}$/SCL0	10		
P13	SI1/RXD0	8		
P14	SO1/TXD0	5		
P15	$\overline{\text{SCK1}}$/ASCK0	8		
P20	SI3/RXD1	8	PORTV$_{DD}$	
P21	SO3/TXD1	5		
P22	$\overline{\text{SCK3}}$/ASCK1	8		
P23	SI4			
P24	SO4	5		
P25	$\overline{\text{SCK4}}$	8		
P26	–			
P27	–	5		
P30 to P33	TI2/TO2 to TI5/TO5	8	PORTV$_{DD}$	
P34	VM45/TI71			
P40 to P47	AD0 to AD7	5	PORTV$_{DD}$	
P50 to P57	AD8 to AD15	5	PORTV$_{DD}$	
P60 to P65	A16 to A21	5	PORTV$_{DD}$	
P70 to P77	ANI0 to ANI7	9	ADCV$_{DD}$	Individually connect to ADCV$_{DD}$ or ADCGND via a resistor.
P80 to P83	ANI8 to ANI11	9	ADCV$_{DD}$	
P90	$\overline{\text{LBEN}}$	5	PORTV$_{DD}$	Input: Individually connect to PORTV$_{DD}$ or PORTGND via a resistor. Output: Leave open.
P91	$\overline{\text{UBEN}}$			
P92	R/$\overline{\text{W}}$			
P93	$\overline{\text{DSTB}}$			
P94	ASTB			
P95	$\overline{\text{HLDAK}}$			
P96	$\overline{\text{HLDRQ}}$			

Table 2-1. Types of Pin I/O Circuits and Connection of Unused Pins (2/2)

Pin	Alternate Function	I/O Circuit Type	I/O Buffer Power Supply	Recommended Connection of Unused Pins
P100	KR0/TO7	8-A	$PORTV_{DD}$	Input: Individually connect to $PORTV_{DD}$ or PORTGND via a resistor. Output: Leave open.
P101	KR1/TI70			
P102	KR2/TI00			
P103	KR3/TI01			
P104	KR4/TO0			
P105	KR5/TI10			
P106	KR6/TI11			
P107	KR7/TO1			
P110	$\overline{WAIT}$	5	$PORTV_{DD}$	Input: Individually connect to $PORTV_{DD}$ or PORTGND via a resistor. Output: Leave open.
P111 to P113	–			
P114	CANTX1	5		
P115	CANRX1	8		
P116	CANTX2[Note 1]	5		
P117	CANRX2[Note 1]	8		
CLKOUT	–	4	$PORTV_{DD}$	Leave open.
$\overline{RESET}$	–	2	$PORTV_{DD}$	–
X1	–	–	–	–
X2	–	–	–	–
XT1	–	–	–	Connect to GND0 to GND2 via a resistor.
XT2	–	–	–	Leave open.
V_{PP}[Note 2]	–	–	–	Connect to GND0 to GND2.
IC[Note 3]	–	–	–	Connect directly to GND0 to GND2.
CPUREG	–	–	–	–
V_{DD0}	–	–	–	–
GND0 to GND2	–	–	–	–
$ADCV_{DD}$	–	–	–	–
ADCGND	–	–	–	–
$PORTV_{DD}$	–	–	–	–
PORTGND	–	–	–	–

Notes 1. μPD703079Y, 70F3079Y only

2. μPD70F3079Y only

3. μPD703078Y, 703079Y only

Figure 2-1. Pin I/O Circuits (1/2)

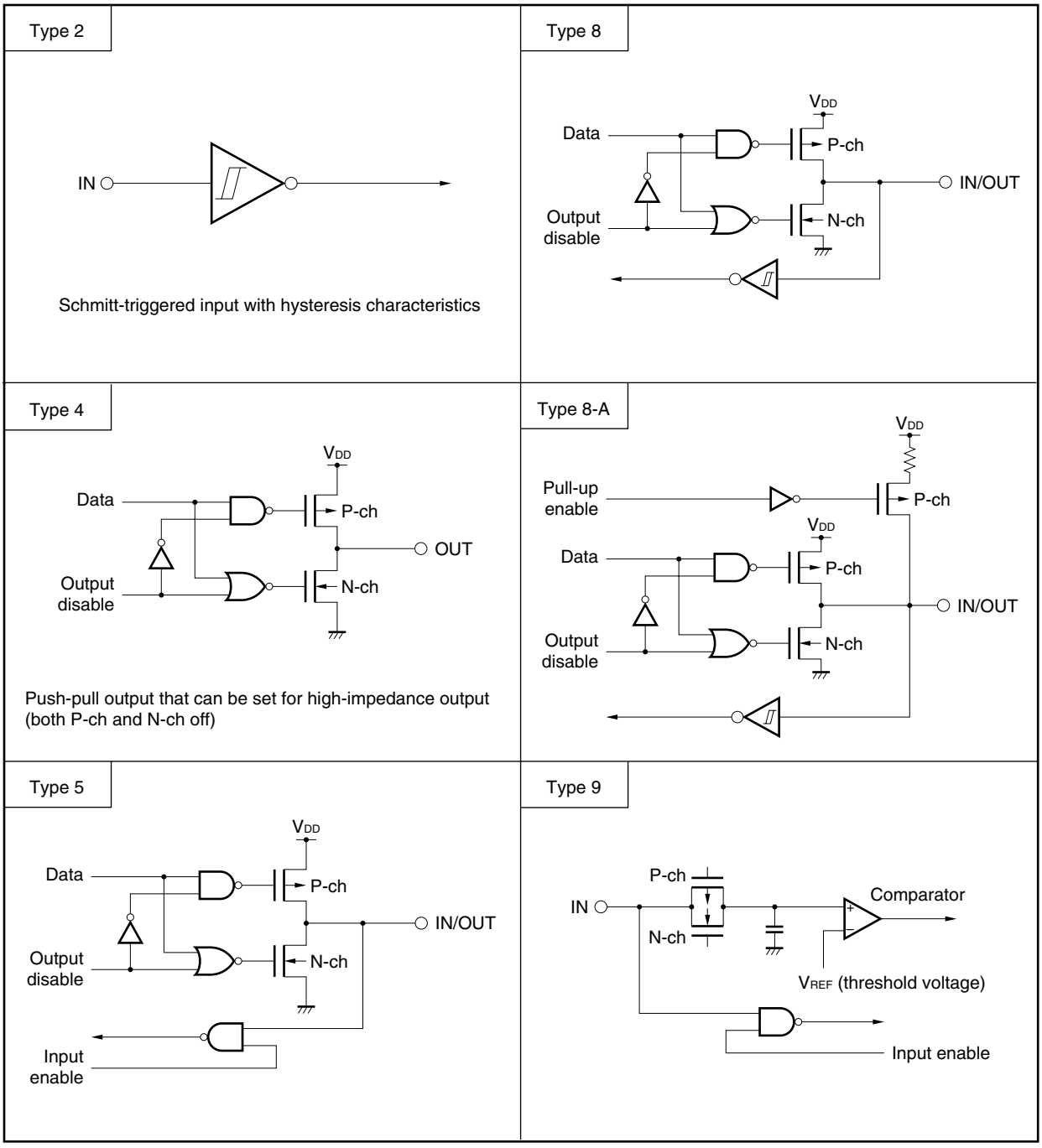
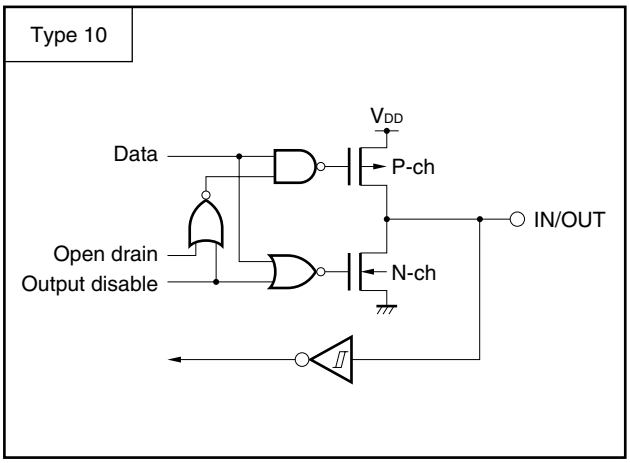


Figure 2-1. Pin I/O Circuits (2/2)



3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD0}, $PORTV_{DD}$, $ADCV_{DD}$ pins	–0.3 to +6.0	V
Input voltage	V_{I1}	V_{DD0}, $PORTV_{DD}$, $ADCV_{DD}$ pins	–0.3 to V_{DD} +0.3 Note 1	V
	V_{I2}	V_{PP} pin (μPD70F3079Y only)	–0.3 to +8.5	V
Analog input voltage	V_{AN}	**Note 2** ($ADCV_{DD}$ pin)	–0.3 to V_{DD} +0.3 Note 1	V
Output current, low	I_{OL}	Per pin	8.0	mA
		Total for all pins	25	mA
Output current, high	I_{OH}	Per pin	–8.0	mA
		Total for P00, P05 to P07, P20 to P27, P30 to P34, P90 to 96 and their alternate-function pins	–25	mA
		Total for P01 to P04, P10 to P15, P40 to P47, P50 to P57, P60 to P65, P100 to P107, P110 to P117 and their alternate-function pins	–25	mA
Output voltage	V_O		–0.3 to V_{DD} + 0.3 Note 1	V
Operating ambient temperature	T_A	Normal operation mode	–40 to +85	°C
		Flash memory programming mode (μPD70F3079Y only)	–20 to +85	°C
Storage temperature	T_{stg}	μPD703078Y, 703079Y	–65 to +150	°C
		μPD70F3079Y	–40 to +125	°C

Notes 1. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

2. Ports 7, 8, and their alternate-function pins

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND. However, direct connections among open-drain and open-collector pins are possible, as are direct connections to external circuits that have timing designed to prevent output conflict with pins that become high-impedance.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

3.1 Normal Operation Mode

Operating Conditions

★ **(1) Operating voltage**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD0}	0.5 ≤ f_{CPU} ≤ 16 MHz, when all functions are operating (except the A/D converter)	μPD70F3079Y	4.5		5.5	V
			μPD703078Y, 703079Y	4.0		5.5	V
		0.5 ≤ f_{CPU} ≤ 12 MHz, f_{XT} = 32.768 kHz, when all functions are operating (except the A/D converter)	μPD70F3079Y	4.0		5.5	V
			μPD703078Y, 703079Y	3.5		5.5	V
	$PORTV_{DD}$	0.5 ≤ f_{CPU} ≤ 16 MHz	μPD70F3079Y	4.5		5.5	V
			μPD703078Y, 703079Y	4.0		5.5	V
		0.5 ≤ f_{CPU} ≤ 12 MHz, f_{XT} = 32.768 kHz	μPD70F3079Y	4.0		5.5	V
			μPD703078Y, 703079Y	3.5		5.5	V
	$ADCV_{DD}$	When the A/D converter is operating, V_{DD0} = $ADCV_{DD}$		4.5		5.5	V
		When the A/D converter is stopped		4.0		5.5	V

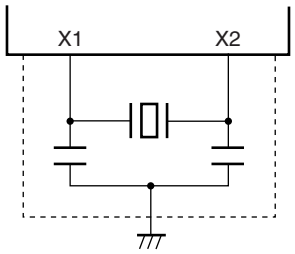
(2) CPU operating frequency

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU operating frequency	f_{CPU}	Main system clock operation	0.5		16	MHz
		Subsystem clock operation		32.768		kHz

Recommended Oscillator

(1) Main system clock oscillator (T_A = –40 to +85°C)

(a) Connection of ceramic resonator or crystal resonator



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{XX}		4		16	MHz
Oscillation stabilization time	–	Upon reset release		$2^{21}/f_{XX}$		s
	–	Upon STOP mode release		**Note**		s

Note The TYP. value differs depending on the setting of the oscillation stabilization time select register (OSTS).

Cautions 1. Main system clock oscillator operates on the output voltage of the on-chip regulator. External clock input is prohibited.

2. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

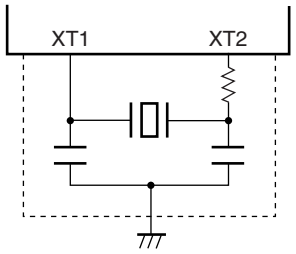
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

3. Ensure that the duty of oscillation waveform is between 5.5 and 4.5.

4. For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

(2) Subsystem clock oscillator (T_A = –40 to +85°C)

(a) Connection of crystal resonator



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{XT}			32.768		kHz
★ Oscillation stabilization time	–	When reset is released		10		s

Cautions 1. Subsystem clock oscillator operates on the output voltage of the on-chip regulator. External clock input is prohibited.

2. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

3. Sufficiently evaluate the matching between the resonator and the μPD703078Y, 703079Y, and 70F3079Y.

DC Characteristics (T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = ADCGND = 0 V,
μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, $ADCV_{DD}$ = 4.5 to 5.5 V,
μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V, $ADCV_{DD}$ = 4.5 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	**Note 1**		0.7V_{DD}		V_{DD}	V
	V_{IH2}	**Note 2**		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	**Note 1**		0		0.3V_{DD}	V
	V_{IL2}	**Note 2**		0		0.2V_{DD}	V
Output current, high	I_{OH1}	**Note 3**	V_{OH} = V_{DD} – 1 V	–1.0			mA
			V_{OH} = V_{DD} – 0.5 V	–100			μA
Output current, low	I_{OL1}	**Note 3**	V_{OL} = 1 V			1.0	mA
			V_{OL} = 0.5 V			100	μA
Input leakage current, high	I_{IH1}	**Note 4**	V_{IN} = V_{DD}			5.0	μA
Input leakage current, low	I_{IL1}	**Note 4**	V_{IN} = 0 V			–5.0	μA
Output off-leakage current	I_{L1}	**Note 5**	V_{OH} = V_{DD}			5.0	μA
Pull-up resistor	R_{L1}	**Note 6**	V_{IN} = 0 V	10	30	100	kΩ

Notes 1. P11, P14, P21, P24, P27, P34, P40 to P47, P50 to P57, P60 to P65, P70 to P77, P80 to P83, P90 to P96, P100, P104, P107, P110 to P114, P116, and other alternate-function pins

2. P00 to P07, P10, P12, P13, P15, P20, P22, P23, P25, P26, P30 to P33, P101 to P103, P105, P106, P115, P117, $\overline{\text{RESET}}$, and other alternate-function pins

★ **3.** All output pins and other alternate-function pins

4. All input pins and other alternate-function pins

5. P10, P12 (in N-ch open-drain mode)

6. P100 to P107 (in key return mode)

DC Characteristics (T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = ADCGND = 0 V,
μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, $ADCV_{DD}$ = 4.5 to 5.5 V,
μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V, $ADCV_{DD}$ = 4.5 to 5.5 V) (2/2)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	μPD703078Y, μPD703079Y	I_{DD1}	In normal operation mode[Note 1]		15	30	mA
		I_{DD2}	In HALT mode[Note 2]		9	20	mA
		I_{DD3}	In IDLE mode[Note 3]		0.5	3	mA
		I_{DD4}	In STOP mode[Note 4]		15	100	μA
		I_{DD5}	In normal mode (subsystem operation)[Note 5]		50	200	μA
		I_{DD6}	In HALT mode (subsystem operation)[Note 6]		30	180	μA
		I_{DD7}	In IDLE mode (subsystem operation)[Note 7]		20	160	μA
	μPD70F3079Y	I_{DD1}	In normal operation mode[Note 1]		25	50	mA
		I_{DD2}	In HALT mode[Note 2]		9	20	mA
		I_{DD3}	In IDLE mode[Note 3]		0.5	4	mA
		I_{DD4}	In STOP mode[Note 4]		15	100	μA
		I_{DD5}	In normal mode (subsystem operation)[Note 5]		200	600	μA
		I_{DD6}	In HALT mode (subsystem operation)[Note 6]		150	300	μA
		I_{DD7}	In IDLE mode (subsystem operation)[Note 7]		90	200	μA

Notes 1. f_{CPU} = f_{XX} = 16 MHz, V_{IN} = V_{CPUREG}, peripheral functions operating (except FCAN)

2. f_{CPU} = f_{XX} = 16 MHz, V_{IN} = V_{CPUREG}, CPU stopped, peripheral functions operating (except FCAN)

3. f_{XX} = 16 MHz, V_{IN} = V_{CPUREG}, all peripheral functions stopped (watch timer operating)

4. f_{XT} = 32.768 kHz, V_{IN} = V_{CPUREG}, main clock oscillator stopped, all peripheral functions stopped (watch timer operating with subsystem clock)

5. f_{CPU} = f_{XT} = 32.768 kHz, V_{IN} = V_{CPUREG}, main clock oscillator stopped, all peripheral functions operating (except FCAN)

6. f_{CPU} = f_{XT} = 32.768 kHz, V_{IN} = V_{CPUREG}, main clock oscillator stopped, CPU stopped, peripheral functions operating (except FCAN)

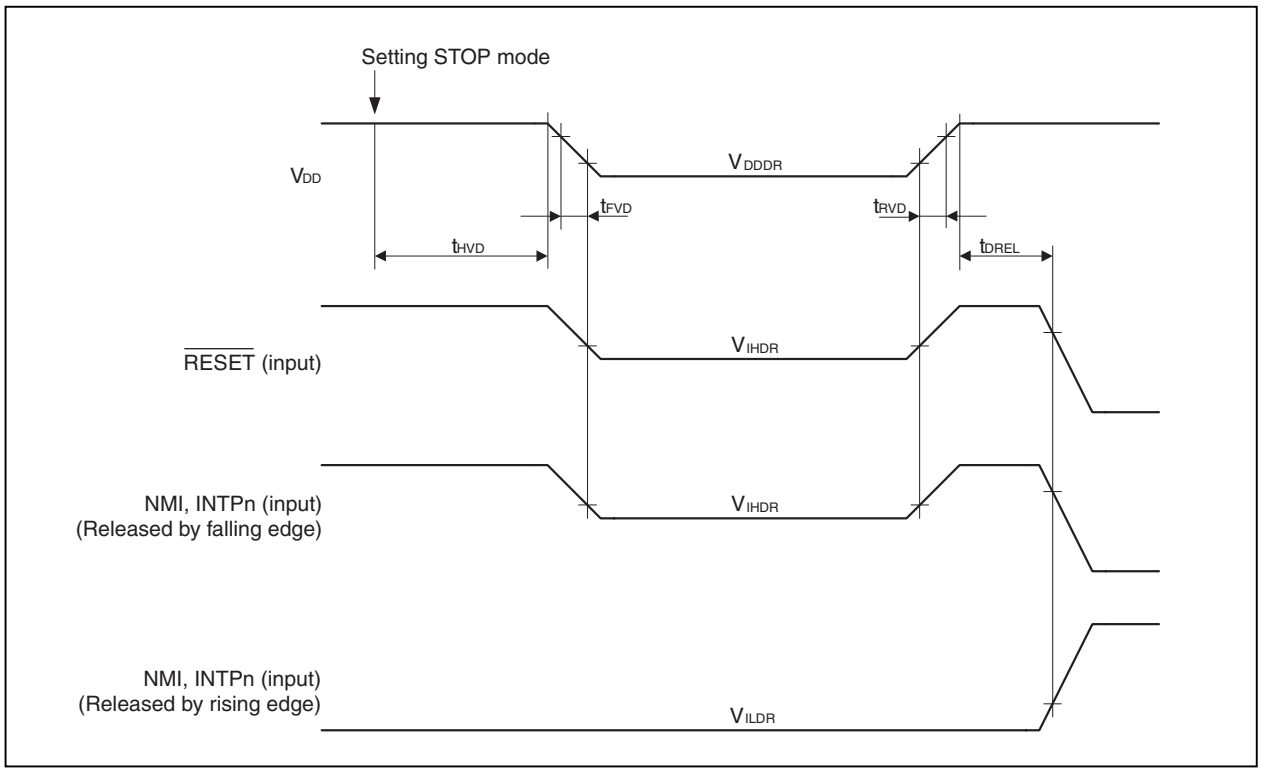
7. f_{XT} = 32.768 kHz, V_{IN} = V_{CPUREG}, main clock oscillator stopped, all peripheral functions stopped (watch timer operating)

Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode[Note] (no functions operating)	2.2		5.5	V
Data retention current	I_{DDDR}	STOP mode[Note] (no functions operating)		10	100	μA
Supply voltage rise time	t_{RVD}		200			μs
Supply voltage fall time	t_{FVD}		200			μs
Supply voltage hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ns
Data retention high-level input voltage	V_{IHDR}	All input ports	0.9V_{DDDR}		V_{DDDR}	V
Data retention low-level input voltage	V_{ILDR}	All input ports	0		0.1V_{DDDR}	V

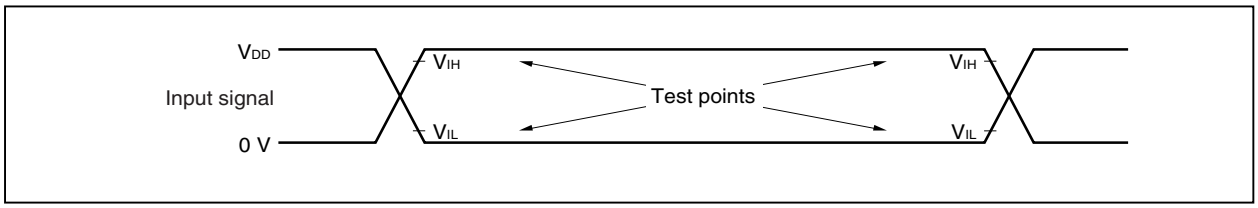
Note Subsystem stopped

★

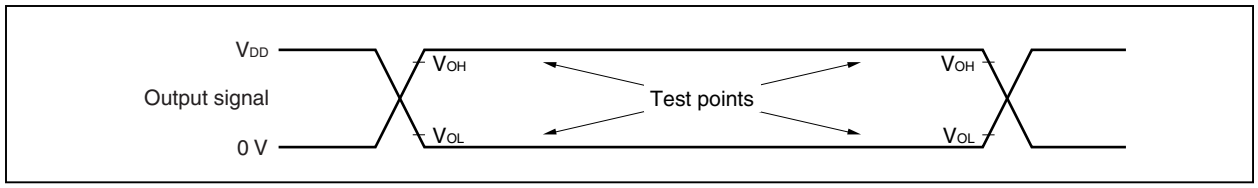


AC Characteristics (T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = ADCGND = 0 V,
μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, $ADCV_{DD}$ = 4.0 to 5.5 V,
μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = $ADCV_{DD}$ = 4.0 to 5.5 V)

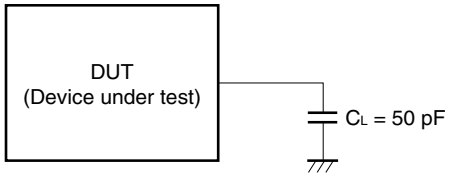
AC Test Input Test Points (V_{DD}: V_{DD0}, $PORTV_{DD}$, $ADCV_{DD}$)



AC Test Output Test Points (V_{DD}: V_{DD0}, $PORTV_{DD}$)



Load Conditions



Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

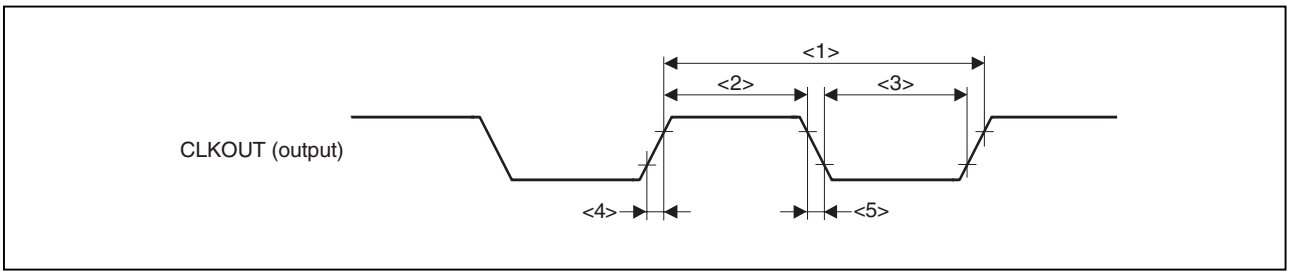
(1) Clock timing

(a) T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V, μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.5 to 5.5 V

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
CLKOUT output cycle	<1>	t_{CYK}		62.5 ns	31 μs	
CLKOUT high-level width	<2>	t_{WKH}		$0.4t_{CYK}$ – 12		ns
CLKOUT low-level width	<3>	t_{WKL}		$0.4t_{CYK}$ – 12		ns
CLKOUT rise time	<4>	t_{KR}			12	ns
CLKOUT fall time	<5>	t_{KF}			12	ns

★ **(b) T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V, μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V**

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
CLKOUT output cycle	<1>	t_{CYK}		83 ns	31 μs	
CLKOUT high-level width	<2>	t_{WKH}		$0.4t_{CYK}$ – 15		ns
CLKOUT low-level width	<3>	t_{WKL}		$0.4t_{CYK}$ – 15		ns
CLKOUT rise time	<4>	t_{KR}			15	ns
CLKOUT fall time	<5>	t_{KF}			15	ns



⋆ **(2) Output waveform (other than port 4, port 5, port 6, port 9, and CLKOUT)**

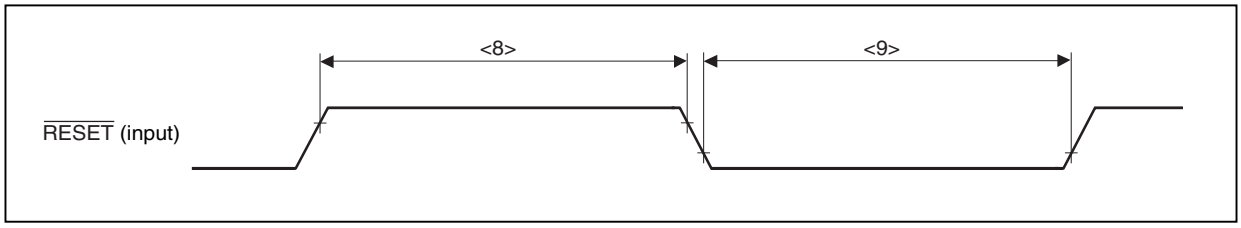
(T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V, μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Output rise time	<6>	t_{OR}			35	ns
Output fall time	<7>	t_{OF}			35	ns

(3) Reset timing

(T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V, μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{RESET}$ pin high-level width	<8>	t_{WRSH}		500		ns
$\overline{RESET}$ pin low-level width	<9>	t_{WRSL}		500		ns



(4) Bus timing

(a) Clock asynchronous

(T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V, μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.5 to 5.5 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	<10>	t_{SAST}		0.5T – 25		ns
Address hold time (from ASTB↓)	<11>	t_{HSTA}		0.5T – 15		ns
Delay time from $\overline{DSTB}$↓ to address float	<12>	t_{FDA}			0	ns
Data input setup time from address	<13>	t_{SAID}			(2 + n)T – 55	ns
Data input setup time from $\overline{DSTB}$↓	<14>	t_{SDID}			(1 + n)T – 45	ns
★ Data input setup time from ASTB↓	<15>	t_{SASID}			(1.5 + n)T – 62	ns
Delay time from ASTB↓ to $\overline{DSTB}$↓	<16>	t_{DSTD}		0.5T – 15		ns
Data input hold time (from $\overline{DSTB}$↑)	<17>	t_{HDID}		0		ns
Address output time from $\overline{DSTB}$↑	<18>	t_{DDA}		(1 + i)T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↑	<19>	t_{DDST1}		0.5T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↓	<20>	t_{DDST2}		(1.5 + i)T – 15		ns
$\overline{DSTB}$ low-level width	<21>	t_{WDL}		(1 + n)T – 20		ns
ASTB high-level width	<22>	t_{WSTH}		T – 15		ns
Data output time from $\overline{DSTB}$↓	<23>	t_{DDOD}			20	ns
Data output setup time (to $\overline{DSTB}$↑)	<24>	t_{SODD}		(1 + n)T – 30		ns
Data output hold time (from $\overline{DSTB}$↑)	<25>	t_{HDOD}		T – 15		ns
$\overline{WAIT}$ setup time (to address)	<26>	t_{SAWT1}	n ≥ 1		1.5T – 55	ns
	<27>	t_{SAWT2}			(1.5 + n)T – 55	ns
$\overline{WAIT}$ hold time (from address)	<28>	t_{HAWT1}	n ≥ 1	(0.5 + n)T		ns
	<29>	t_{HAWT2}		(1.5 + n)T		ns
$\overline{WAIT}$ setup time (to ASTB↓)	<30>	t_{SSTWT1}	n ≥ 1		T – 40	ns
	<31>	t_{SSTWT2}			(1 + n)T – 40	ns
$\overline{WAIT}$ hold time (from ASTB↓)	<32>	t_{HSTWT1}	n ≥ 1	nT		ns
	<33>	t_{HSTWT2}		(1 + n)T		ns
$\overline{HLDRQ}$ high-level width	<34>	t_{WHQH}		T + 10		ns
$\overline{HLDAK}$ low-level width	<35>	t_{WHAL}		T – 15		ns
Delay time from $\overline{HLDAK}$↑ to bus output	<36>	t_{DHAC}		0		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	<37>	t_{DHQHA1}		1.5T	(2n + 7.5)T + 25	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	<38>	t_{DHQHA2}		0.5T	1.5T + 25	ns

Remarks 1. T: $1/f_{CPU}$ (f_{CPU}: CPU clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

3. i: Number of idle cycles inserted in the bus cycle.

4. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

★ **(b) Clock asynchronous**

(T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V, μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	<10>	t_{SAST}		0.5T – 32		ns
Address hold time (from ASTB↓)	<11>	t_{HSTA}		0.5T – 22		ns
Delay time from $\overline{DSTB}$↓ to address float	<12>	t_{FDA}			0	ns
Data input setup time from address	<13>	t_{SAID}			(2 + n)T – 70	ns
Data input setup time from $\overline{DSTB}$↓	<14>	t_{SDID}			(1 + n)T – 60	ns
Data input setup time from ASTB↓	<15>	t_{SASID}			(1.5 + n)T – 70	ns
Delay time from ASTB↓ to $\overline{DSTB}$↓	<16>	t_{DSTD}		0.5T – 15		ns
Data input hold time (from $\overline{DSTB}$↑)	<17>	t_{HDID}		0		ns
Address output time from $\overline{DSTB}$↑	<18>	t_{DDA}		(1 + i)T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↑	<19>	t_{DDST1}		0.5T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↓	<20>	t_{DDST2}		(1.5 + i)T – 15		ns
$\overline{DSTB}$ low-level width	<21>	t_{WDL}		(1 + n)T – 35		ns
ASTB high-level width	<22>	t_{WSTH}		T – 15		ns
Data output time from $\overline{DSTB}$↓	<23>	t_{DDOD}			25	ns
Data output setup time (to $\overline{DSTB}$↑)	<24>	t_{SODD}		(1 + n)T – 35		ns
Data output hold time (from $\overline{DSTB}$↑)	<25>	t_{HDOD}		T – 25		ns
$\overline{WAIT}$ setup time (to address)	<26>	t_{SAWT1}	n ≥ 1		1.5T – 70	ns
	<27>	t_{SAWT2}			(1.5 + n)T – 70	ns
$\overline{WAIT}$ hold time (from address)	<28>	t_{HAWT1}	n ≥ 1	(0.5 + n)T		ns
	<29>	t_{HAWT2}		(1.5 + n)T		ns
$\overline{WAIT}$ setup time (to ASTB↓)	<30>	t_{SSTWT1}	n ≥ 1		T – 55	ns
	<31>	t_{SSTWT2}			(1 + n)T – 55	ns
$\overline{WAIT}$ hold time (from ASTB↓)	<32>	t_{HSTWT1}	n ≥ 1	nT		ns
	<33>	t_{HSTWT2}		(1 + n)T		ns
$\overline{HLDRQ}$ high-level width	<34>	t_{WHQH}		T + 10		ns
$\overline{HLDAK}$ low-level width	<35>	t_{WHAL}		T – 25		ns
Delay time from $\overline{HLDAK}$↑ to bus output	<36>	t_{DHAC}		0		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	<37>	t_{DHQHA1}		1.5T	(2n + 7.5)T + 25	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	<38>	t_{DHQHA2}		0.5T	1.5T + 25	ns

Remarks 1. T: 1/f_{CPU} (f_{CPU}: CPU clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

3. i: Number of idle cycles inserted in the bus cycle.

4. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(c) Clock synchronous

(T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V, μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.5 to 5.5 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<39>	t_{DKA}		0	35	ns
Delay time from CLKOUT↑ to address float	<40>	t_{FKA}		–12	15	ns
Delay time from CLKOUT↓ to ASTB	<41>	t_{DKST}		0	30	ns
Delay time from CLKOUT↑ to $\overline{DSTB}$	<42>	t_{DKD}		0	30	ns
Data input setup time (to CLKOUT↑)	<43>	t_{SIDK}		20		ns
Data input hold time (from CLKOUT↑)	<44>	t_{HKID}		5		ns
Delay time from CLKOUT↑ to data output	<45>	t_{DKOD}			35	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	<46>	t_{SWTK}		25		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	<47>	t_{HKWT}		5		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	<48>	t_{SHQK}		20		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	<49>	t_{HKHQ}		5		ns
Delay time from CLKOUT↑ to address float (during bus hold)	<50>	t_{DKF}			19	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	<51>	t_{DKHA}			35	ns

Remark The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

★ **(d) Clock synchronous**

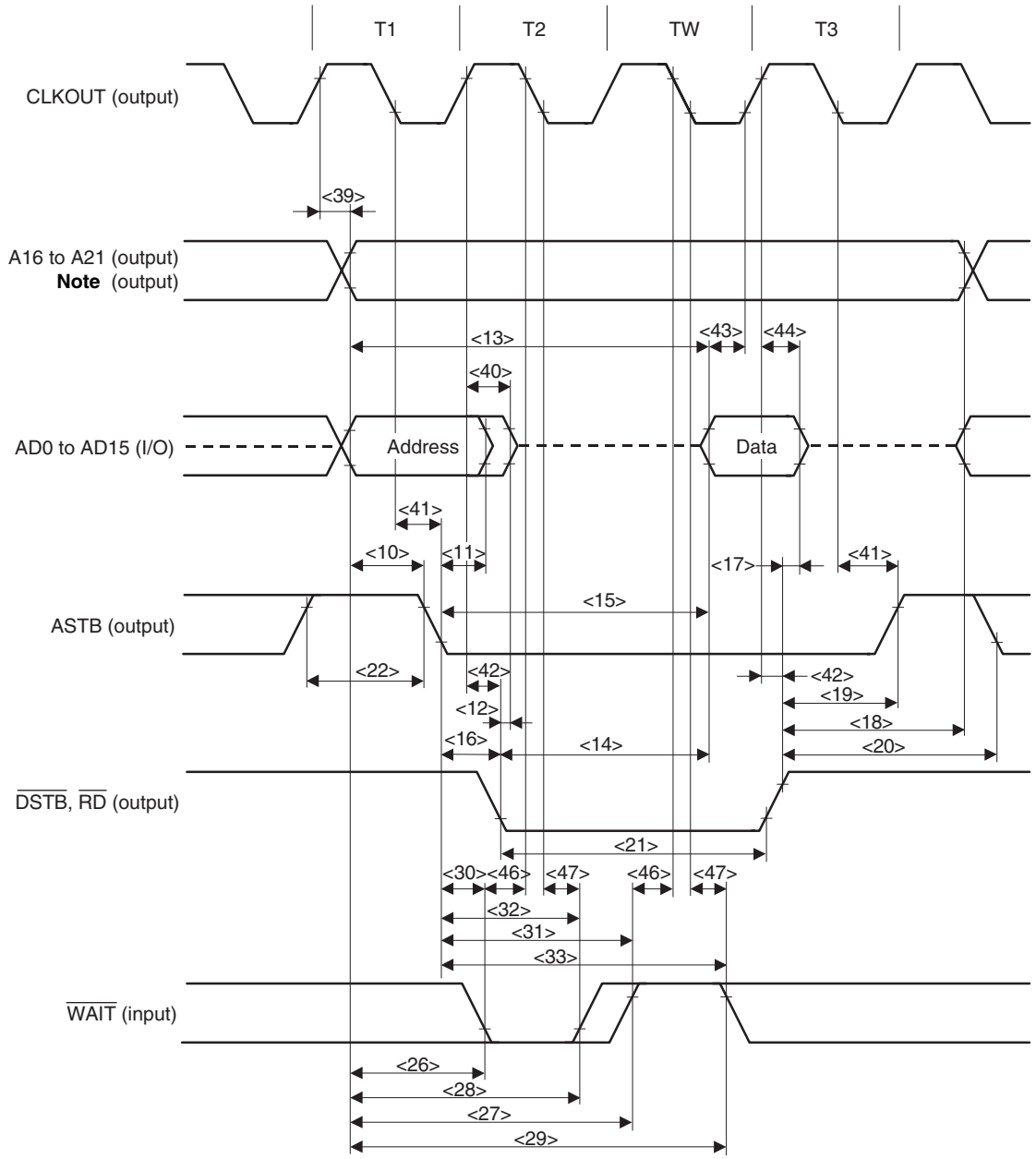
(T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V, μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<39>	t_{DKA}		0	45	ns
Delay time from CLKOUT↑ to address float	<40>	t_{FKA}		–17	15	ns
Delay time from CLKOUT↓ to ASTB	<41>	t_{DKST}		0	35	ns
Delay time from CLKOUT↑ to $\overline{DSTB}$	<42>	t_{DKD}		0	35	ns
Data input setup time (to CLKOUT↑)	<43>	t_{SIDK}		20		ns
Data input hold time (from CLKOUT↑)	<44>	t_{HKID}		5		ns
Delay time from CLKOUT↑ to data output	<45>	t_{DKOD}			45	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	<46>	t_{SWTK}		29		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	<47>	t_{HKWT}		5		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	<48>	t_{SHQK}		24		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	<49>	t_{HKHQ}		5		ns
Delay time from CLKOUT↑ to address float (during bus hold)	<50>	t_{DKF}			19	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	<51>	t_{DKHA}			40	ns

Remark The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(e) Read cycle (CLKOUT synchronous/asynchronous, 1 wait)

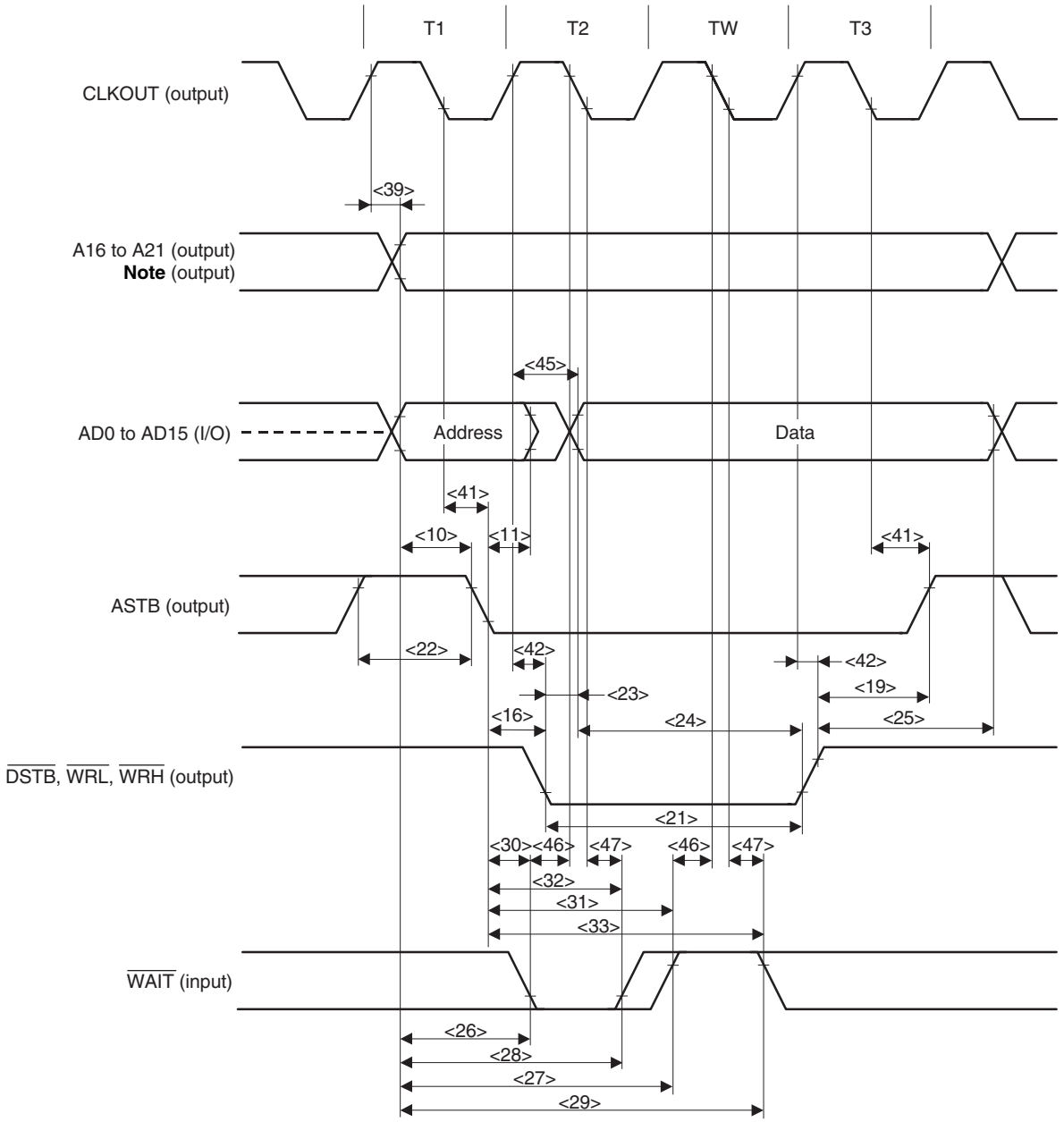
★



Note R/$\overline{W}$, $\overline{UBEN}$, $\overline{LBEN}$

Remark Broken lines indicate high impedance.

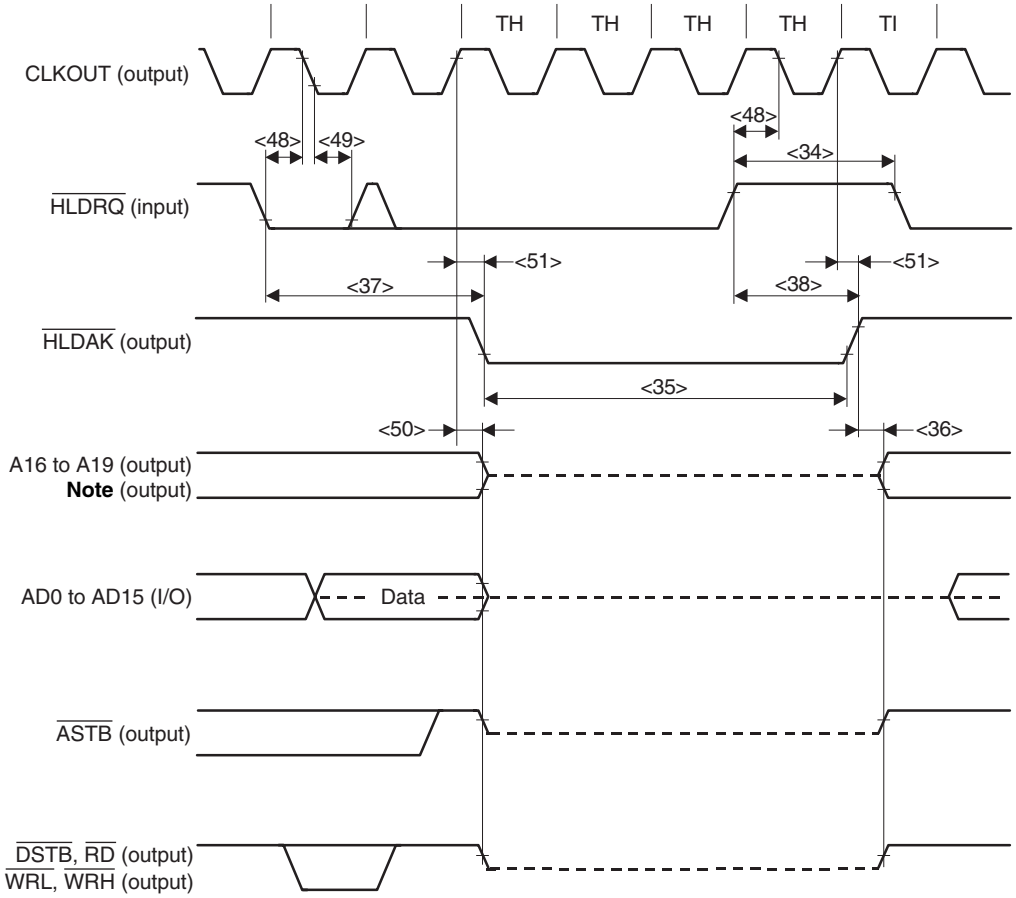
(f) Write cycle (CLKOUT synchronous/asynchronous, 1 wait)



Note R/W, UBEN, LBEN

Remark Broken lines indicate high impedance.

(g) Bus hold timing



Note R/W, UBEN, LBEN

Remark Broken lines indicate high impedance.

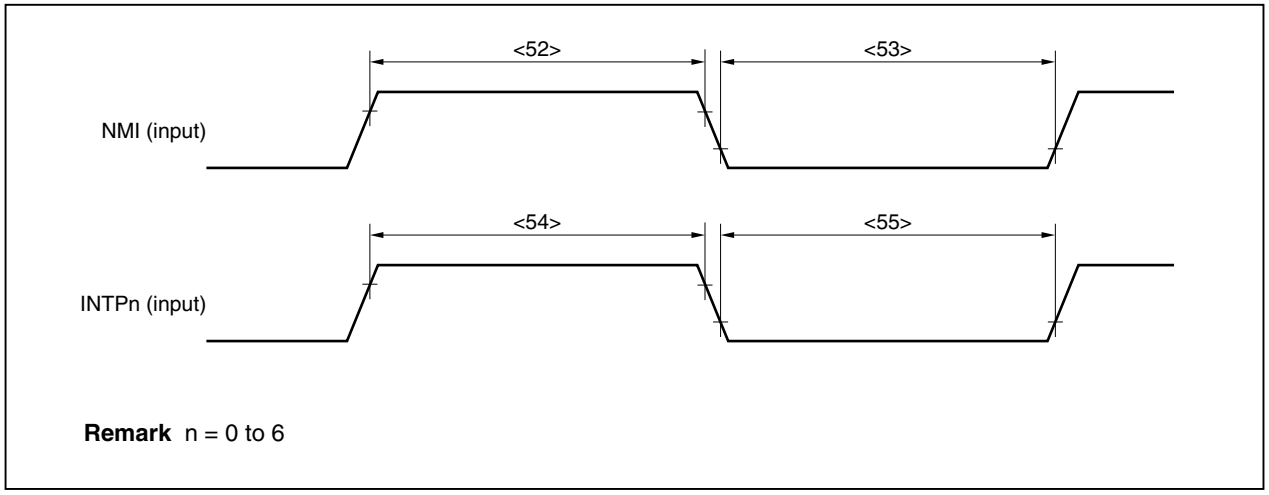
(5) Interrupt timing

(T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V, μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
NMI high-level width	<52>	t_{WNIH}		500		ns
NMI low-level width	<53>	t_{WNIL}		500		ns
INTPn high-level width	<54>	t_{WITH}	n = 0 to 3, analog noise elimination	500		ns
			n = 4, 5, digital noise elimination	3T + 20		ns
			n = 6, digital noise elimination	3Tsmp + 20		ns
INTPn low-level width	<55>	t_{WITL}	n = 0 to 3, analog noise elimination	500		ns
			n = 4, 5, digital noise elimination	3T + 20		ns
			n = 6, digital noise elimination	3Tsmp + 20		ns

Remarks 1. T: 1/fxx

2. Tsmp: Noise elimination sampling clock cycle



Remark n = 0 to 6

(6) RPU timing

(T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V, μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
TIn0, TIn1 high-level width	<56>	t_{TIHn}	n = 0, 1, 7	$2T_{sam}$ + 20[Note]		ns
TIn0, TIn1 low-level width	<57>	t_{TILn}	n = 0, 1, 7	$2T_{sam}$ + 20[Note]		ns
TIm high-level width	<58>	t_{TIHm}	m = 2 to 5	3T + 20		ns
TIm low-level width	<59>	t_{TILm}	m = 2 to 5	3T + 20		ns

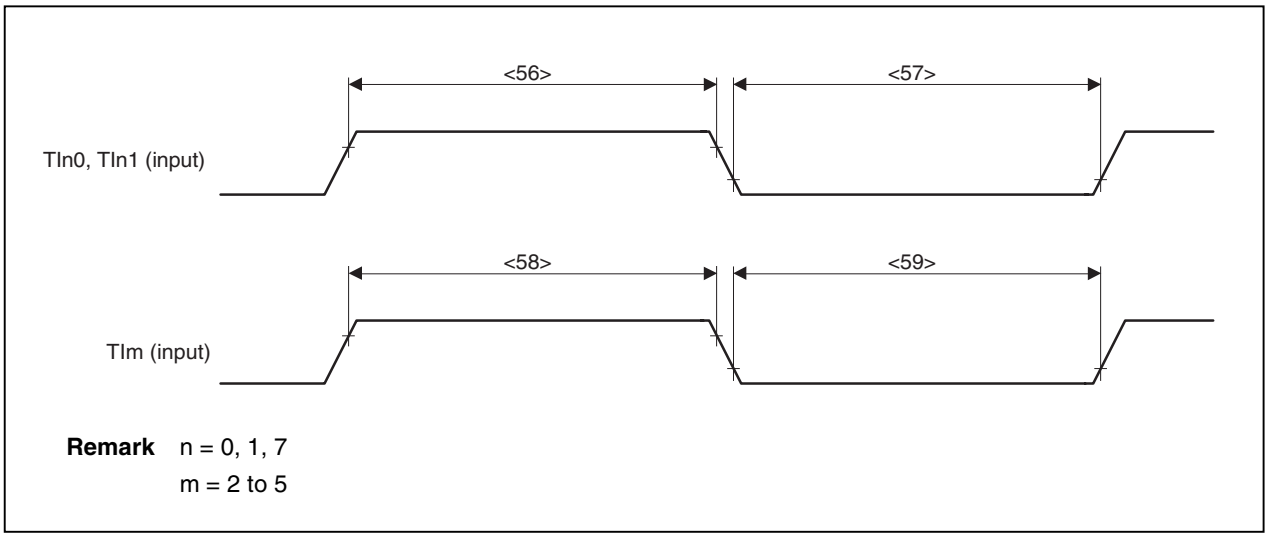
Note T_{sam} (count clock cycle) can select the following cycles by setting the PRMn2 to PRMn0 bits of prescaler mode registers n0, n1 (PRMn0, PRMn1).

When n = 0 (TM0), T_{sam} = 2T, 4T, 16T, 64T, 256T, or 1/INTWTNI cycle

When n = 1 (TM1), T_{sam} = 2T, 4T, 16T, 32T, 128T, or 256T cycle

However, when the TIn0 valid edge is selected as the count clock, T_{sam} = 4T.

Remark T: 1/fxx



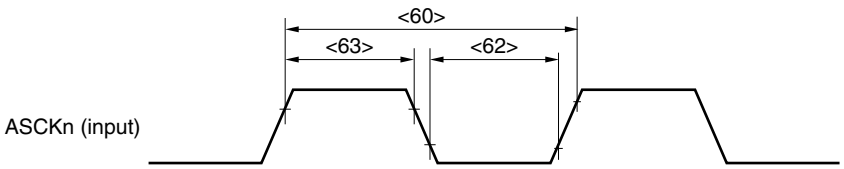
Remark n = 0, 1, 7
m = 2 to 5

(7) Asynchronous serial interface (UART0, UART1) timing

(T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V, μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
ASCKn cycle time	<60>	t_{KCY13}		200		ns
ASCKn high-level width	<61>	t_{KH13}		80		ns
ASCKn low-level width	<62>	t_{KL13}		80		ns

Remark n = 0, 1



Remark n = 0, 1

(8) 3-wire serial interface (CSI0, CSI1 CSI3) timing

(T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V)

(a) Master mode

	Parameter	Symbol		Conditions	MIN.	MAX.	Unit
	$\overline{SCKn}$ cycle	<63>	t_{KCY1}	**Note 1**	400		ns
	$\overline{SCKn}$ high-level width	<64>	t_{KH1}	**Note 1**	140		ns
	$\overline{SCKn}$ low-level width	<65>	t_{KL1}	**Note 1**	140		ns
	SIn setup time (to $\overline{SCKn}$↑)	<66>	t_{SIK1}	**Note 1**	50		ns
	SIn hold time (from $\overline{SCKn}$↑)	<67>	t_{KSI1}	**Note 1**	50		ns
★	Delay time from $\overline{SCKn}$↓ to SOn output	<68>	t_{KSO1}	**Note 2**		80	ns
				Note 1		100	ns

★ **Notes 1.** μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V

2. μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.5 to 5.5 V

Remark n = 0, 1, 3

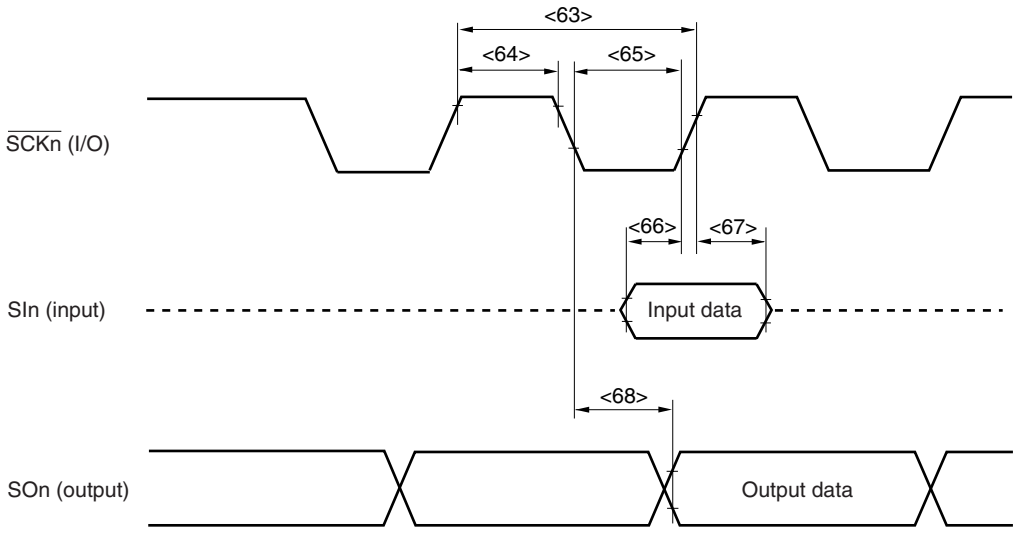
(b) Slave mode

	Parameter	Symbol		Conditions	MIN.	MAX.	Unit
	$\overline{SCKn}$ cycle	<63>	t_{KCY2}	**Note 1**	400		ns
	$\overline{SCKn}$ high-level width	<64>	t_{KH2}	**Note 1**	140		ns
	$\overline{SCKn}$ low-level width	<65>	t_{KL2}	**Note 1**	140		ns
	SIn setup time (to $\overline{SCKn}$↑)	<66>	t_{SIK2}	**Note 1**	50		ns
	SIn hold time (from $\overline{SCKn}$↑)	<67>	t_{KSI2}	**Note 1**	50		ns
★	Delay time from $\overline{SCKn}$↓ to SOn output	<68>	t_{KSO2}	**Note 2**		80	ns
				Note 1		100	ns

★ **Notes 1.** μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V

2. μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.5 to 5.5 V

Remark n = 0, 1, 3



Remarks 1. Broken lines indicate high impedance.

2. n = 0, 1, 3

(9) 3-wire variable length serial interface (CSI4) timing

(T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V)

(a) Master mode

	Parameter	Symbol		Conditions	MIN.	MAX.	Unit
	$\overline{SCK4}$ cycle	<69>	t_{KCY1}	**Note 1**	200		ns
	$\overline{SCK4}$ high-level width	<70>	t_{KH1}	**Note 1**	60		ns
	$\overline{SCK4}$ low-level width	<71>	t_{KL1}	**Note 1**	60		ns
	SI4 setup time (to $\overline{SCK4}$↑)	<72>	t_{SIK1}	**Note 1**	25		ns
	SI4 hold time (from $\overline{SCK4}$↑)	<73>	t_{KSI1}	**Note 1**	20		ns
★	Delay time from $\overline{SCK4}$↓ to SO4 output	<74>	t_{KSO1}	**Note 2**		55	ns
				Note 1		70	ns

★ **Notes 1.** μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V

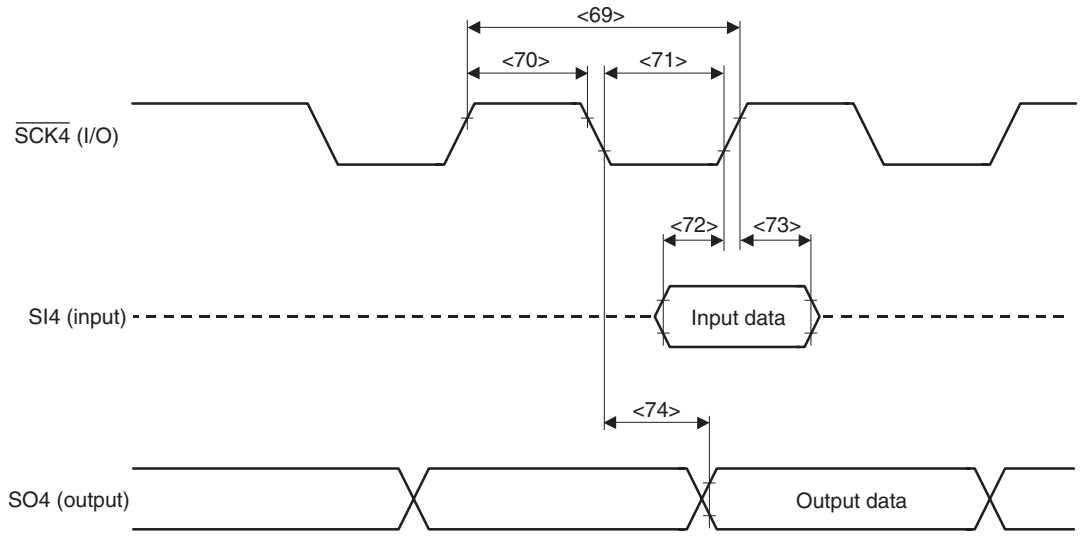
2. μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.5 to 5.5 V

(b) Slave mode

	Parameter	Symbol		Conditions	MIN.	MAX.	Unit
	$\overline{SCK4}$ cycle	<69>	t_{KCY2}	**Note 1**	200		ns
	$\overline{SCK4}$ high-level width	<70>	t_{KH2}	**Note 1**	60		ns
	$\overline{SCK4}$ low-level width	<71>	t_{KL2}	**Note 1**	60		ns
	SI4 setup time (to $\overline{SCK4}$↑)	<72>	t_{SIK2}	**Note 1**	25		ns
	SI4 hold time (from $\overline{SCK4}$↑)	<73>	t_{KSI2}	**Note 1**	20		ns
★	Delay time from $\overline{SCK4}$↓ to SO4 output	<74>	t_{KSO2}	**Note 2**		55	ns
				Note 1		70	ns

★ **Notes 1.** μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V

2. μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.5 to 5.5 V



Remark Broken lines indicate high impedance.

(10) I^2C bus mode

(T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V, μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V) (1/2)

Parameter		Symbol		Normal Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		–	f_{CLK}	0	100	0	400	kHz
Bus-free time (between stop/start conditions)		<75>	t_{BUF}	4.7	–	1.3	–	μs
Hold time[Note 1]		<76>	$t_{HD:STA}$	4.0	–	0.6	–	μs
SCL0 clock low-level width		<77>	t_{LOW}	4.7	–	1.3	–	μs
SCL0 clock high-level width		<78>	t_{HIGH}	4.0	–	0.6	–	μs
Setup time for start/restart conditions		<79>	$t_{SU:STA}$	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	<80>	$t_{HD:DAT}$	5.0	–	–	–	μs
	I^2C mode			0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		<81>	$t_{SU:DAT}$	250	–	100[Note 4]	–	ns
SDA0 and SCL0 signal rise time		<82>	t_R	–	1000	20 + 0.1Cb[Note 5]	300	ns
SDA0 and SCL0 signal fall time		<83>	t_F	–	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		<84>	$t_{SU:STO}$	4.0	–	0.6	–	μs
Pulse width of spike suppressed by input filter		<85>	t_{SP}	–	–	0	50	ns
Capacitance load of each bus line		–	Cb	–	400	–	400	pF

Notes 1. At the start condition, the first clock pulse is generated after the hold time.

2. The system requires a minimum of 300 ns hold time internally for the SDA0 signal (at $V_{IHmin.}$ of SCL0 signal) in order to occupy the undefined area at the falling edge of SCL0.

3. If the system does not extend the SCL0 signal low hold time (t_{LOW}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

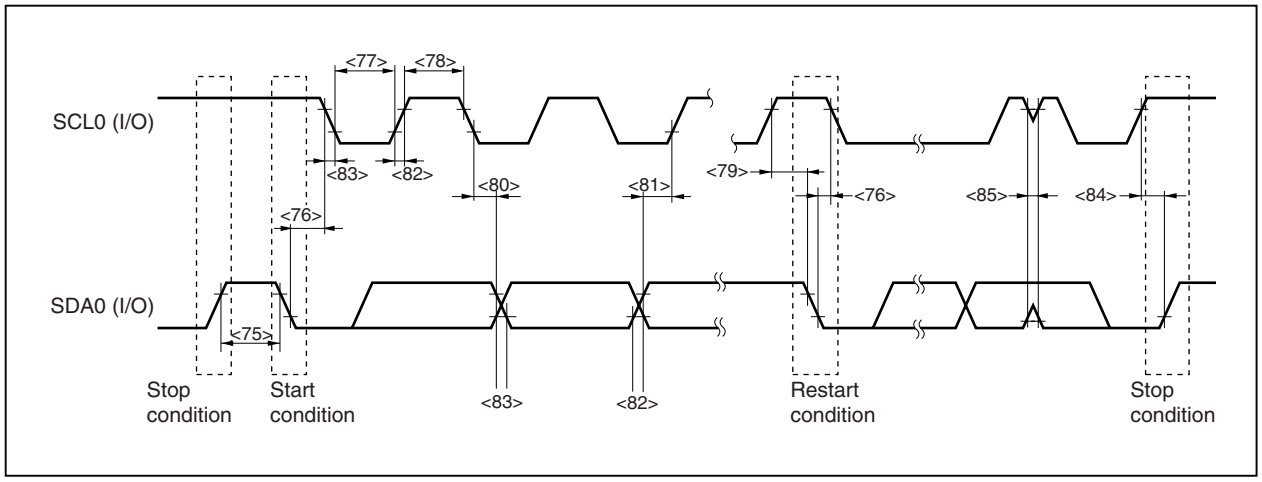
4. The high-speed mode I^2C bus can be used in the normal-mode I^2C bus system. In this case, set the high-speed mode I^2C bus so that it meets the following conditions.

- If the system does not extend the SCL0 signal's low state hold time:
  $t_{HD:DAT} \geq 250$ ns
- If the system extends the SCL0 signal's low state hold time:
  Transmit the following data bit to the SDA0 line prior to the SCL0 line release ($t_{Rmax.} + t_{SU:DAT}$ = 1000 + 250 = 1250 ns: Normal mode I^2C bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

★ **(10) I^2C bus mode**

(T_A = –40 to +85°C, GND0 = GND1 = GND2 = PORTGND = 0 V, μPD703078Y, 703079Y: V_{DD0} = $PORTV_{DD}$ = 3.5 to 5.5 V, μPD70F3079Y: V_{DD0} = $PORTV_{DD}$ = 4.0 to 5.5 V) (2/2)



A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD0} = $ADCV_{DD}$ = 4.5 to 5.5 V, GND0 = GND1 = GND2 = ADCGND = 0 V, Output pin load capacitance: C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	–		10	10	10	bit
Overall error[Note 1]	–	ADM2 = 01H			±1.0	%FSR
Conversion time	t_{CONV}		5		10	μs
Zero-scale error[Note 1]	AINL				±0.4	%FSR
Full-scale error[Note 1]	AINL	ADM2 = 01H			±0.6	%FSR
Integral linearity error[Note 2]	INL	ADM2 = 01H			±6.0	LSB
Differential linearity error[Note 2]	DNL	ADM2 = 01H			±6.0	LSB
Analog power supply voltage	AV_{DD}	$ADCV_{DD}$ pin	4.5		5.5	V
Analog input voltage	V_{IAN}		0		$ADCV_{DD}$	V
$ADCV_{DD}$ current	AI_{DD}	ADM2 = 01H		4	8	mA

Notes 1. Excluding quantization error (±0.05 %FSR)

2. Excluding quantization error (±0.5 LSB)

Remarks 1. LSB: Least Significant Bit
FSR: Full Scale Range

2. ADM2: A/D converter mode register 2

Power-On-Clear Circuit, 4.5 V Detection Flag Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
POC circuit detection voltage	V_{POCH}	CPU operation	2.7	3.0	3.3	V
	V_{POCL}	STOP mode	1.5	1.8	2.1	V
VM45 flag setting voltage	VM45		3.7	4.2	4.5	V

3.2 Flash Memory Programming Mode (μPD70F3079Y only)

Basic Characteristics (T_A = –20 to +85°C, V_{DD} = $ADCV_{DD}$ = $PORTV_{DD}$ = 4.5 to 5.5 V, GND0 = GND1 = GND2 = ADCGND = PORTGND = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} supply voltage	V_{PP2}	During flash memory programming	7.5	7.8	8.1	V
★ V_{DD} supply current	I_{DD}	$V_{PP} = V_{PP2}$, f_{XX} = 16 MHz			53	mA
V_{PP} supply current	I_{PP}	$V_{PP} = V_{PP2}$			100	mA
Step erase time	t_{ER}	**Note 1**		0.2		s
Overall erase time per area	t_{ERA}	When the step erase time = 0.2 s **Note 2**			20	s/area
Write-back time	t_{WB}	**Note 3**		1		ms
Number of write-backs per write-back command	C_{WB}	When the write-back time = 1 ms **Note 4**			300	Count/write-back command
Number of erase/write-backs	C_{ERWB}				16	Count
Step writing time	t_{WR}	**Note 5**		20		μs
Overall writing time per word	t_{WRW}	When the step writing time = 20 μs (1 word = 4 bytes) **Note 6**	20		200	μs/word
Number of rewrites per area	C_{ERWR}	1 erase + 1 write after erase = 1 rewrite **Note 7**	100			Count/area

Notes 1. The recommended setting value of the step erase time is 0.2 s.

2. The prewrite time prior to erasure and the erase verify time (write-back time) are not included.

3. The recommended setting value of the write-back time is 1 ms.

4. Write-back is executed once by the issuance of the write-back command. Therefore, the retry count must be the maximum value minus the number of commands issued.

5. The recommended setting value of the step writing time is 20 μs.

6. 20 μs is added to the actual writing time per word. The internal verify time during and after the writing is not included.

7. When writing initially to shipped products, it is counted as one rewrite for both “erase to write” and “write only”.

Example (P: Write, E: Erase)

Shipped product ⟶ P → E → P → E → P: 3 rewrites

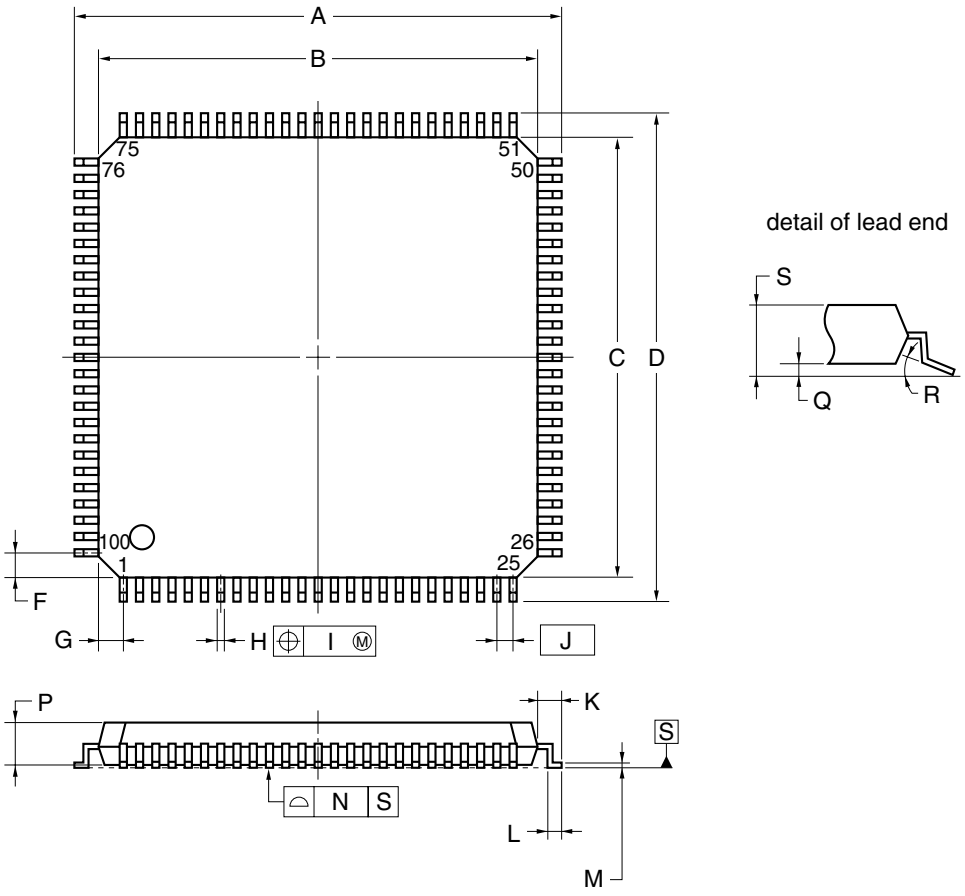
Shipped product → E → P → E → P → E → P: 3 rewrites

Remarks 1. When the PG-FP3 is used, a time parameter required for writing/erasing by downloading parameter files is automatically set. Do not change the settings otherwise specified.

2. Area 0 = 00000H to 1FFFFH, area 1 = 20000H to 3FFFFH

4. PACKAGE DRAWINGS

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



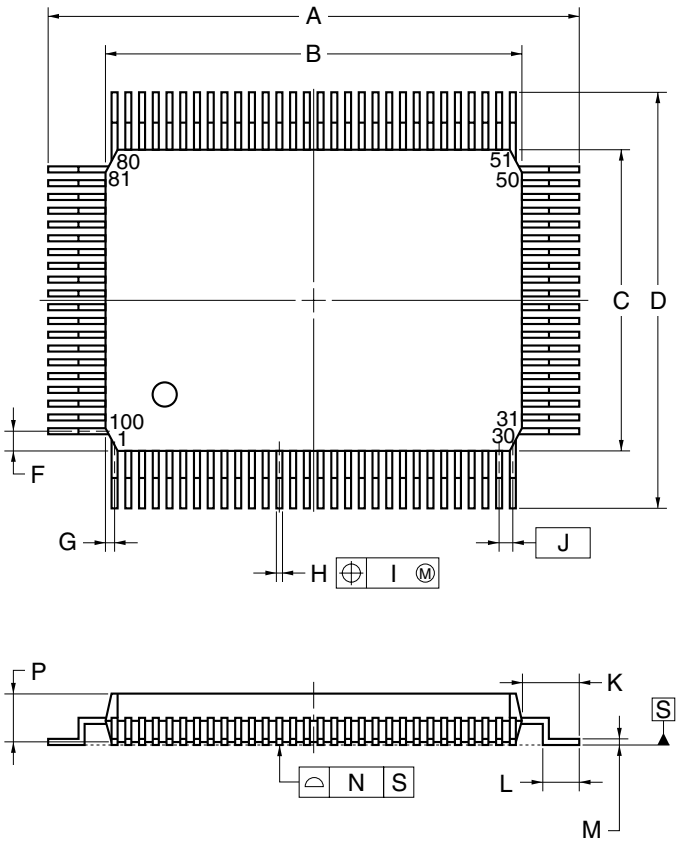
NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

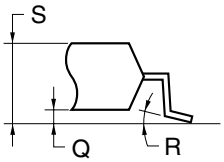
ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	3^{+7}_{-3}
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

100-PIN PLASTIC QFP (14x20)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	23.6±0.4
B	20.0±0.2
C	14.0±0.2
D	17.6±0.4
F	0.8
G	0.6
H	0.30±0.10
I	0.15
J	0.65 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

P100GF-65-3BA1-4

5. RECOMMENDED SOLDERING CONDITIONS

The μPD703078Y, 703079Y, and 70F3079Y should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Caution The recommended soldering conditions for the following products have not been determined.

- **μPD703078YGF-xxx-3BA**
- **μPD703079YGF-xxx-3BA**
- **μPD70F3079YGF-3BA**

Table 5-1. Surface Mounting Type Soldering Conditions

μPD703078YGC-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD703079YGC-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD70F3079YGC-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 20 to 40 seconds max. (at 200°C or higher), Count: Two times or less Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Caution Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Reference document Electrical Characteristics for Microcomputer (U15170J)[Note]

Note This document number is that of the Japanese version.

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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