

MAS 7848 RDS MODEM/ MANCHESTER DECODER

APPLICATIONS

RDS Receivers
MBS Pagers

GENERAL DESCRIPTION

The IC contains all the necessary function blocks to demodulate and decode the incoming modulated 57 kHz subcarrier. On the output the binary data and bit synchronous clock is available for further frame decoding. The above mentioned signal processing is performed digitally.

For MBS receivers the circuit also provides some analog function blocks such as a FM-tuner voltage generator, FM comparator, battery voltage and temperature indicators and a power savings function.

FUNCTIONAL DESCRIPTION

Manchester decoder

The circuit accepts an analog 57 kHz signal on its PSK input pin. The signal is amplified and converted to a digital signal by an autozeroing comparator. This digital signal is then fed to a 57 kHz PLL. The internally generated synchronous 57 kHz clock is then used to demodulate the product modulated PSK input signal.

The resultant baseband signal is then low pass filtered and fed to a 1187,5 Hz PLL. The internally generated synchronous 1187,5 Hz clock is used to demodulate the tone phase modulated differentially coded information. Finally the binary information can be decoded.

DATA and DCO are the end products of this process and corresponds to binary data and clock. A crystal of 3,648 MHz is connected between X1 and X2.

Tuner voltage generator

The generator contains a 9 bit D/A converter. The output voltage at UT is programmed by applying an appropriate number of pulses on the FST input.

The AFC input allows automatic frequency control to take place.

The AUD input is used to fine tune the output voltage. The DC level of the FM detector output in the tuner is normally used for this.

FM comparator

The circuit also includes a separate comparator with the inverting input FCN and the non-inverting input FCP. The output of the comparator is available at pin FCO.

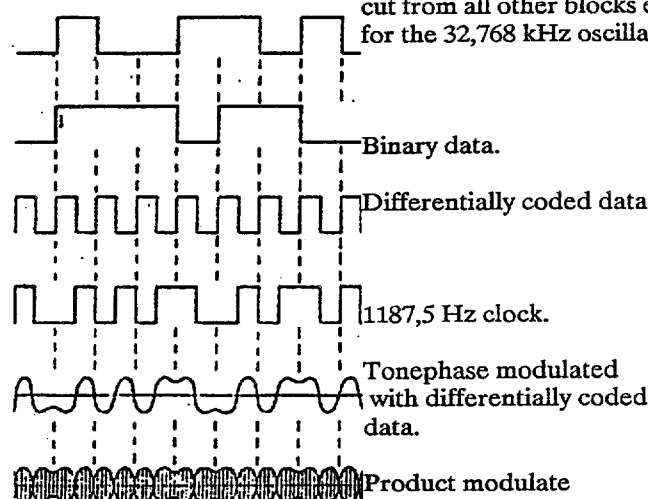
Battery voltage and temperature indicators.

The device can be used in monitoring the battery voltage. The outputs BTH, BTM and BTL change their states from 1 to 0 when the voltage at the UBAT input drops below the threshold's $(VDD + 0,14)/2$ V, $(VDD)/2$ V and $(VDD - 0,14)/2$ V correspondingly.

The temperature is monitored by an NTC resistor connected between the pins UTMP and VSS. When the voltage at UTMP drops below $VDD/2$ the output TMP changes its state from VDD to VSS.

The power-down circuitry and the 32,768 kHz oscillator.

The device is equipped with a power down feature to reduce power consumption in pager applications. When the PWR input is high power is cut from all other blocks except for the 32,768 kHz oscillator.

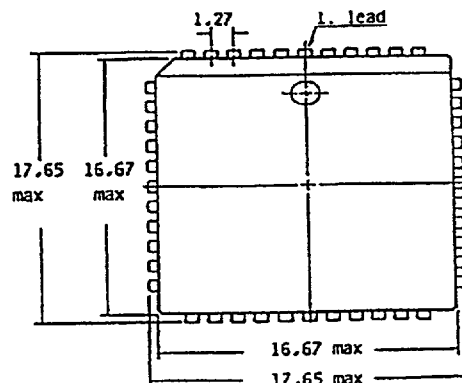


Signal description

Pin	Name	IO/AD	Function
8	PSK	I/A	Phase shift keyed 57 kHz input signal.
12	FST	I/D	Clock to tuner voltage generator.
5	POL	I/D	Polarity of the S-curve. POL = 1 raising voltage POL = 0 falling voltage
9	AFC	I/D	Automatic frequency control using AUD as fine tuning voltage. Active high.
11	AUD	I/A	A DC voltage level from the tuner used to fine adjust the tuning.
10	UT	O/A	Tuning voltage to tuner.
DIGI44 ANA1	VDD VDA	I	Positive power supply for digital circuits. Positive power supply for analog circuits.
DIGI23 ANA22	VSS VSA	I	Negative power supply, 0 V for digital circuits. Negative power supply, 0 V for analog circuits.
3	FCN	I/A	Inverting input of FM comparator.
2	FCP	I/A	Non-inverting input of FM comparator.
43	FCO	O/A	Output of FM comparator.
21	UTMP	I/A	DC voltage proportional to temperature. (From an NTC resistor)
27	TMP	O/D	When the voltage at UTMP drops below VDD/2 this pin changes its state from VDD to VSS.
20	UBAT	I/A	Comparator input used for monitoring the battery voltage.
31	BTH	O/D	Battery test high. BTH is high when the voltage at the UBAT input is over $(VDD + 0,14)/2$ V.
30	BTM	O/D	Battery test medium. BTM is high when the voltage at the UBAT input is over VDD/2 V.
32	BTL	O/D	Battery test low. BTL is high when the voltage at the UBAT input is over $(VDD - 0,14)/2$ V.
26	PWR	I/D	Power down control PWR = 0 Normal function PWR = 1 Reduced power consumption.

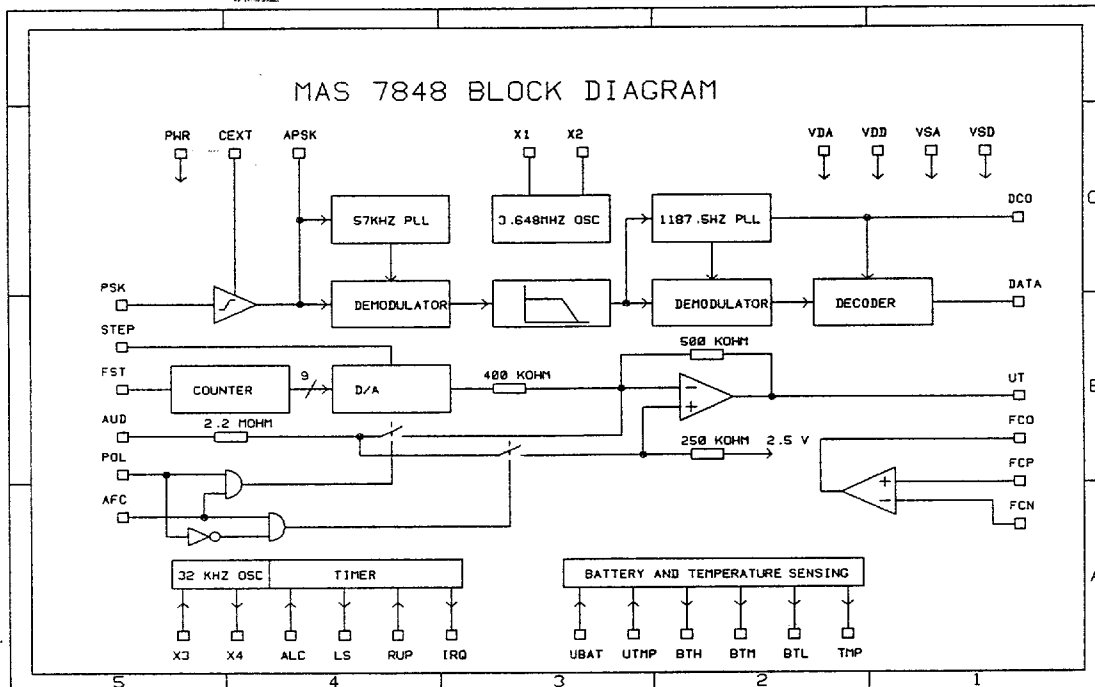
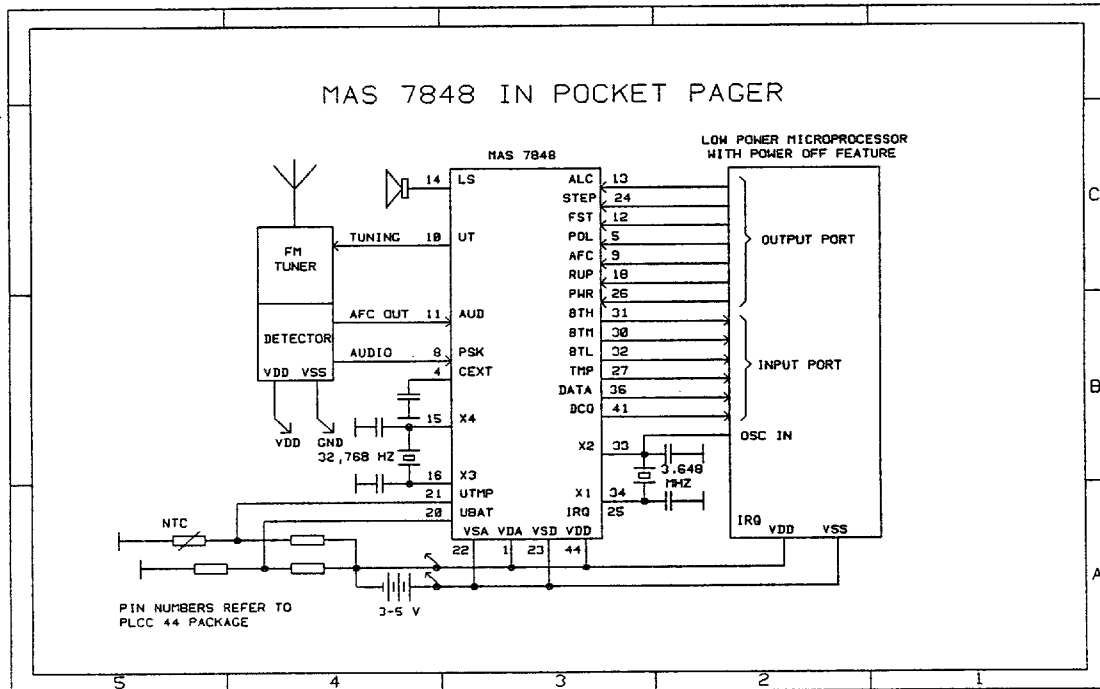
Pin	Name	IO/AD	Function
24	STEP	I/D	Activates the tuner voltage generator and sends an interrupt on IRQ to the micro controller when STEP goes from VDD to VSS and PWR = 1.
18	RUP	I/D	Reset from micro controller. Resets the 32,768 kHz counter and sets IRQ = 1.
25	IRQ	O/D	Interrupt request to micro controller. Active low. Time delay from RUP low/high transition to IRQ high/low is approx 31,2 sec.
14	LS	O/D	Loud speaker alarm. Freq = 2,048 kHz.
13	ALC	I/D	Alarm control. When ALC = 1 a 2,048 kHz square wave signal is available at the LS output.
16	X3	I	X-tal 32,768 kHz
15	X4	O	X-tal 32,768 kHz (Type: 32,768 kHz CX-IV Statek corp.)
34	X1	I	X-tal 3,648 MHz
33	X2	O	X-tal 3,648 MHz
41	DCO	O/D	1187,5 Hz clock from Manchester decoder.
36	DATA	O/D	Binary data from Manchester decoder.
4	CEXT	I/A	External filter capacitor for the auto-zeroing comparator. 4,7 uF typically.
19	Test	O/D	Test pad for 32,8 kHz oscillator.
42	APSK	O/D	Sliced PSK signal

Pin numbering refers to 44 lead PLCC package:





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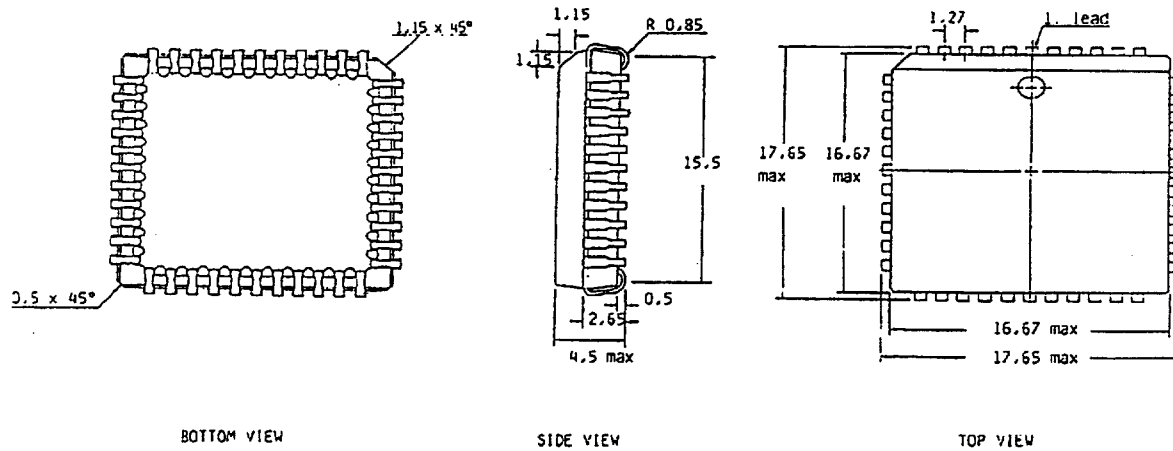




MICRONAS

PACKAGE INFORMATION

PLCC



ORDERING INFORMATION

Our product code:

7848PL44I

Product:

**MAS7848 RDS MODEM/
MANCHESTER DECODER**

Package:

44LD PLCC

Please refer to our product code in ordering.

Your Local Source:

