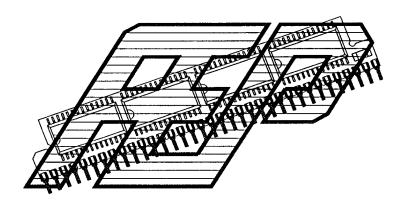
- >> 65,536 x 8 Organization
- >> Double sided to maximize bit density
- >> Low 0.66" stand-off height suited to 0.8" card spacing
- >> Completely Static operation
- >> TTL compatible
- >> Low power, battery back-up operation capability
- >> Uses single +5V power supply
- >> Super Low Power version available



64 KILOBYTE STATIC RAM MODULE

DESCRIPTION:

The AEPSx64K8 is a high density 64 Kilo-word by 8 bit static random access memory module in a 35 pin single-inline-package format. Physically it consists of an FR4 PC material substrate mounted with eight 8K x 8 SOP (small outline package) ICs, two 0.1 microfarad decoupling capacitors, and 35 edge-clip I/O pins.

The module can use any of the 8K x 8 SRAMs made by any of a large number of manufacturers in both Mix-MOS and CMOS technologies. A wide range of access speeds are available. Performance specifications and electrical characteristics are determined by the IC devices used. These items can vary according to the type and manufacturer of the components. The necessary information is obtained from the IC vendors data sheets, which are included here, or from data books.

Mechanical dimensions are 0.66 in. high by 3.48 in. long by 0.28 in. wide. The module is available with either vertical or 90 degree (horizontal) lead pins. The latter allows the module to be mounted on its side which gives a low 0.320 stand-off height.

Nearly 250 interconnections are accomplished within the substrate. Using AEP high density memory modules saves board space, reduces line lengths, and simplifies the layout design process.



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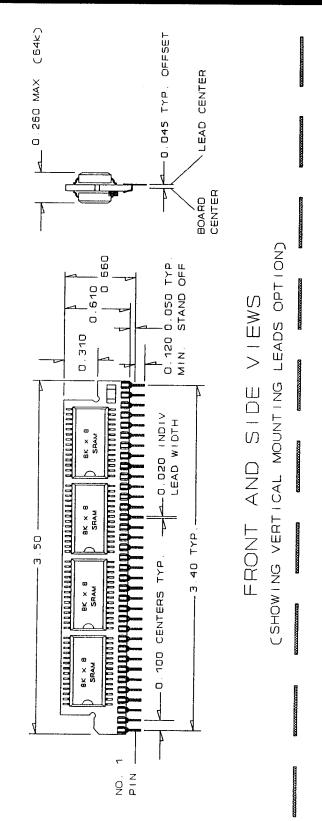
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BOTTOM, REAR, AND SIDES VIEWS (SHOWING HORIZONTAL MOUNTING LEADS OPTION)



64K x 8 STATIC RAM MODULE SIP PIN-OUT CONFIGURATION

1 — A0		
2 — A1		
3 — ANC		
4 — A2		
5 - A3		
6 — A4		
7 - CS12		
8 — A5		
9 - 1/0 1		
10 - 1/0 2		
11 - CS11		
12 - A6		
13 — A7		
14 - A8		
15 — CS14	A0 - A12	ADDRESS INPUTS
16 — A9	T/O 4 T/O 0	D. M. I. T. I. D. G.
17 — GND	I/O 1 - I/O 8	DATA LINES
18 — CS13	r.m	EID TMD 4
19 - VCC	WE	WRITE*
20 — CS2 21 — OE	OE	OUTPUT ENABLE*
22 — CS16	OE	OUIPUI ENABLE
23 - 1/0 3	CS11 - CS18	CHIP SELECTS*
24 1/0 4	0511 0510	CHII DBBBCID
25 -1/0 5	VCC	POWER +5V
26 — CS15		
27 ├──WE	GND	GROUND
28 — A10		
29 — A11	*ACTIVE LOW	
30 ├──CS18		
31 - I/O 6		
32 - I/O 7		
33 ├── CS17		
34 - A12		
35 -1/0 8		

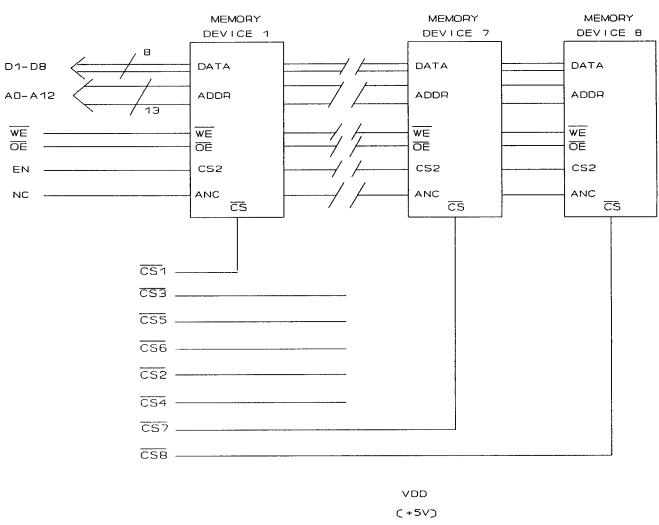


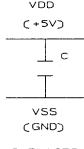
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64K x 8 STATIC RAM MODULE FUNCTIONAL DIAGRAM





2 PLACES



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PART NUMBERING CHART

	Vertical lead pins	Horizontal lead pins
Standard 64K x	8	
35ns SRAM I	Cs AEPSS64K8-35	AEPSH64K8-35
<u>55ns SRAM I</u>	Cs AEPSS64K8-55	AEPSH64K8-55
70ns SRAM I	Cs AEPSS64K8-70	AEPSH64K8-70
85ns SRAM I	Cs AEPSS64K8-85	AEPSH64K8-85
100ns SRAM I	Cs AEPSS64K8-10	AEPSH64K8-10
120ns SRAM I	Cs AEPSS64K8-12	AEPSH64K8-12
Super Low Power		
100ns SRAM I	Cs AEPSS64K8-10SL	AEPSH64K8-10SL
120ns SRAM I	Cs AEPSS64K8-12SL	AEPSH64K8-12SL

Memory notes:

Memory access speeds specified in the part numbers are maximums. AEP reserves the right to use faster rated devices unless requested not to. As an example, 100ns parts may be substituted for 120ns parts depending on stocks on hand.

Due to the rapidly progressing nature of SRAM development, devices with access speeds other than those listed are likely to be available also. Check with AEP.

Vendor notes:

The IC device specification information which may be included is typical and does not limit AEP to that vendor. The actual devices used will be equivalent depending on price, availability, and customer requirements. AEP will gladly use or exclude particular manufacturers upon request. However, this may affect module price.

Disclaimers:

The information in this document has been carefully checked and is believed to be reliable. However, Advanced Electronic Packaging Inc. assumes no responsibility for inaccuracies. AEP also reserves the right to change products or specifications without notice.



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