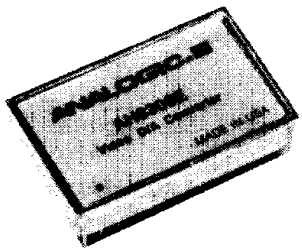


ANALOGIC®

AH8308E

8-Bit Composite Video D/A Converter

Description

The AH8308E is an optimally designed, low power, minimum glitch, high-speed 8-bit composite video D/A converter intended for use in both color and monochromatic Digital Display Systems. It accepts 8-bit digital video data plus sync and blanking commands from an ECL source and produces a composite video output to directly drive a 75Ω load at an update rate as high as 150 MHz.* The 150 MHz update rate, uncontested by competing units, makes this device compatible with the highest resolution monitors available.

A second generation unit drawing on the success of the current industry standard MP8308, the AH8308E represents a completely new design utilizing an optimum combination of hybrid techniques and the successful marriage of both analog and digital circuits on a single custom monolithic VLSI chip. This combination is a significant advance over competing units which are either discrete component devices (modules) or "hybridized" versions of discrete designs. Of particular importance is that the AH8308E achieves its remarkable 150 MHz data update rate at a power dissipation level 25% lower than that of the earlier generation MP8308 or of the other competing modular or hybrid devices patterned after it. All of this has been accomplished without

*A TTL version is also available from Analogic. Please consult the factory for information and applications assistance.

(continued)

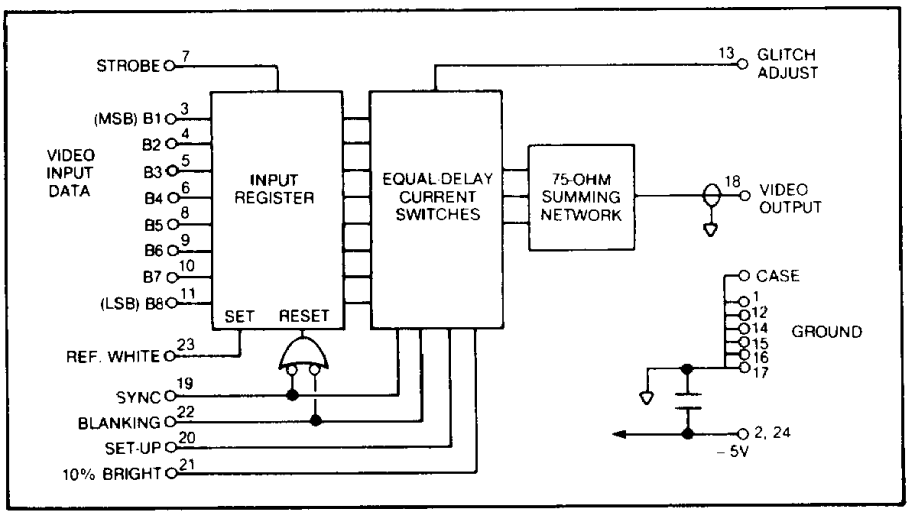


Figure 1. AH8308E Functional Block Diagram.

Features

- **Up to 150 MHz Update Rate**
  Extends display system capabilities
- **Direct Drive to 75Ω Coaxial Cable/TV Monitor**
  Requires no additional circuitry
- **"Glitch-free" performance**
  Simplifies display system design
- **Single −5V Supply**
  Reduces power requirements
- **Composite Sync and Blanking Control Inputs**
  Eliminates need for additional logic or amplifiers
- **10% Overbright Control Input**
  Provides Simple Cursor Generation
- **3 ns Rise and Fall Time**
  Provides accurate, high-speed data update
- **RS170A/RS343A Compatible Output**
  Directly drives monitor
- **Standard 0.790" X 1.305" X 0.295" Package Size**
  Reduces pc board area requirements
- **Pin Compatible with Hybrid Reproductions of Our Earlier Generation MP8308**

Applications

- **CAD/CAM Display Systems**
- **Medical Imaging Systems**
- **"Quick Look" Display Systems**
- **Image Processing Systems**
- **Workstations**
- **Monochrome or Color Display Systems**

SPECIFICATIONS

(All specification guaranteed at 25°C unless otherwise noted)

OUTPUT CHARACTERISTICS

Output Voltage Range

Composite Video
0V to −1.064V; ±3% into 75Ω termination

Gray Scale
−0.064V to −0.707V; ±3% into 75Ω termination

Output Current (Gray Scale)
−17 mA

Recommended Load Impedance
75Ω ±5%, dc to 50 MHz

Source (Thevenin) Impedance
75Ω ±5%, dc to 50 MHz

LSB Size
2.5 mV, nominal

Rise and Fall Time
3 ns, typical, 4 ns maximum (10% to 90%)

Full Step Settling Time
8 ns typical to 1 LSB (0.4%)

Glitch Settling Time
5 ns to <1 LSB for worst MSB transition

Glitch Area
50 pV-s typical, 70 pV-s max.

Compliance Voltage
+1.1V to −1.1V typical

Cable Drive Capacity
75Ω characteristic impedance. Total length to have 7.5Ω dc resistance maximum.

Composite Sync Level
−1.064V with Standard Setup
−0.286V (−40 IRE Units) with respect to blanking level (back porch)

Composite Blanking Level
−0.778V, with Standard Setup

10% Overbright Level
0V

TRANSFER CHARACTERISTICS

Resolution
8 Bits, 256 Gray Scale Levels
2.5 mV per step, nominal

Coding
Binary

Reference White Level
11111111 produces −0.064V absolute, +0.714V (100 IRE Units) relative to blanking level with Standard Set-up; +0.643V relative to Reference Black

Reference Black
00000000 produces −0.707V absolute, +0.071V (10 IRE Units) relative to blanking level with Standard Set-up

Differential Linearity
± ½ LSB maximum

Monotonicity
Guaranteed

Offset (dc output with 10% Overbright Actuated)
± ½ LSB maximum, 0°C to +70°C

Transfer Gain (Slope) Tempco
±0.1% FSR/°C maximum

Propagation Delay
5 ns typical, strobe to output, 50% points

Control Input Speed (Sync, Blanking, Ref. White and 10% Overbright)
8 ns typical to settle to 10% of final value

INPUT CHARACTERISTICS

Logic Levels (all inputs)
10,000 Series ECL
Logic 0 = −1.75V
Logic 1 = −0.9V

Loading (all inputs)
5 pF; open transistor base;
open input is logic "0"

Data
8 ECL compatible inputs

Validity
Data must be valid 2.0 ns min., prior to Strobe and remain valid for 1.5 ns after data Strobed

Update Rate
150 MHz maximum

Strobe Input
Data entered on positive-going edge (Timing Reference)

Pulse width
3 ns minimum

Setup (Reference Black to Blanking)
Input open: Standard 71 mV (10 IRE Units)
Input to −5.0V: 142 mV (20 IRE Units)
Input to Ground: 0 mV (0 IRE Units)

Composite Sync Level
Logic "0" on Sync and Blanking inputs simultaneously resets the input register to 00000000 and drives the output to −1.0643V

Composite Blanking Level
Logic "0" on Blanking input simultaneously resets the input register and drives the output to −0.778V

Reference White Level
Logic "0" on Ref. White input simultaneously sets input register to 11111111 and drives output to −0.064V

10% Overbright Level
Logic "0" on input raises output level by 0.064V. Logic "0" on Ref. White and 10% Overbright drives output to 0V

Rise and Fall Time (all inputs)
<10 ns (10% to 90%)

Glitch Adjust

Control Port Input Impedance
7.5 kΩ

Control Sensitivity
50 pV-s per volt applied to Glitch Adjust pin

POWER SUPPLY REQUIREMENTS

Power Dissipation
0.875 watt typical, 1.0 watt maximum

Power Supply Required Regulation
−5.0V @ 200 mA maximum 5 mV p-p ripple
−4.75V to −5.5V operating range

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range (Ambient)
0°C to +70°C

Storage Temperature
−25°C to +100°C

Relative Humidity
0 to 85%, non-condensing up to +40°C

Mechanical Dimensions
0.790" X 1.305" X 0.295"
(20.07 X 33.14 X 7.49 mm)
24-pin DIP (double width)

Shielding
Steel foil

Description (cont.)

sacrifice of the trend-setting features of its discrete predecessor such as composite video 75Ω output and "glitch free" performance.

Because of its single chip design, the unit has fewer internal wire bonds than other presently available devices and should therefore prove to be considerably more reliable over the life of the system in which it is used. Reliability is further enhanced by its reduced power consumption and lower resultant operating temperature rise.

The very fast (3 ns) rise time analog output directly drives a 75Ω coaxial cable and monitor with a 1 Vp-p signal. No additional amplifiers are required. Output transitions exhibit sufficiently low glitch that no further processing is required. Separate digital inputs for sync and blanking allow the AH8308E to produce EIA Standard RS170A and RS343A compatible composite video; these plus additional inputs for Reference White and 10% Overbright combine to provide a complete, highly flexible, improved performance video D/A converter subsystem in a 0.790" x 1.305" 24 pin dual-in-line package.

Theory of Operation

Eight bit digital data presented to the AH8308E on the data inputs is latched into the D flip-flops at the rising edge of the STROBE pulse applied to the STROBE control input. The outputs of the flip-flops, drive high speed switches that steer current into a summing network with an output impedance of 75Ω, developing a 1 Vp-p signal directly. Due to the extremely small differential delay among the eight data channels, the code switching output glitches are invisible even on the best video monitor.

Digital control inputs for REFERENCE WHITE, SYNC, BLANKING and 10% OVERBRIGHT are provided. A logic 0 on the REF. WHITE input sets the flip-flops and drives the output to −0.064V. Logic 0 on 10% OVERBRIGHT increases the output by 0.064V. Used in conjunction with REF. WHITE, the flip-flops are set and the output is driven to 0V. Logic 0 on the BLANKING and SYNC inputs resets the flip-flops and drives the output to −0.778V and −1.064V respectively. Combinations of BLANKING/SYNC and REF. WHITE/10% OVERBRIGHT should be avoided. While no damage will result, active levels on both the SET and RESET inputs of the D flip-flops will cause an indeterminate output. The condition of the SETUP line determines the relative levels between Reference Black and the Blanking level—left open, the standard 71 mV (10 IRE units) is produced; tied to −5.0V, 142 mV (20 IRE units) is produced; tied to ground, 0 mV (0 IRE units) is produced. (See Chart on last page).

Please refer to the Timing Diagram, Applications Considerations and Video System Display Application sections for examples of operation.

ENGINEER'S NOTEBOOK

Power Supply Requirements

The AH8308E is capable of operating from a single supply voltage between −4.75V and −5.5V. The output amplitudes specified are nominal values based on a −5.0V supply and will change in direct proportion to the supply voltage.

The unit can be powered from a +5.0V positive supply voltage if +5.0V is connected to the GROUND pin(s) and digital return is connected to the −5.0V pin. Under these conditions, the composite video signal will vary from +3.935V to +5.0V, and THE CASE WILL BE AT A +5.0V POTENTIAL.

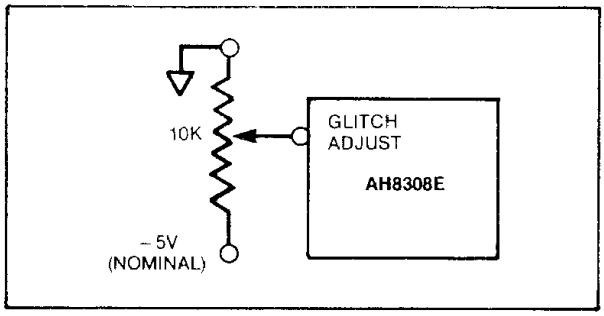


Figure 2. Glitch Adjust

The glitch area will vary as a function of the supply voltage. The factory trim is normally carried out at –5.0V, and may be done at another voltage if specified when ordering.

If other than –5.0V is used with a unit trimmed for –5.0V operation, provisions should be made on the PC board for a 10 kΩ potentiometer connected to the GLITCH ADJUST terminal as shown (in Figure 2). The pot should be adjusted to reduce the glitch area to a minimum.

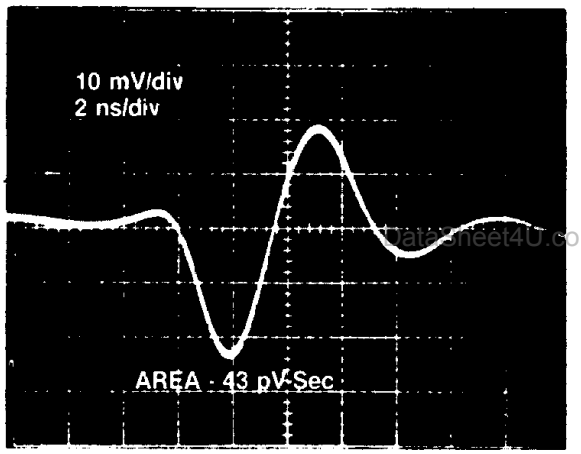


Figure 3. Glitch Area at Major Code Transition.

Grounding

There are six ground pins all tied together internally and to the case of the AH8308E.

ECL Terminators

ECL terminators are not included in the AH8308E. If the source of the video data and control inputs is more than a few inches away from these units, ECL terminators should be connected in close proximity to the inputs of the DAC.

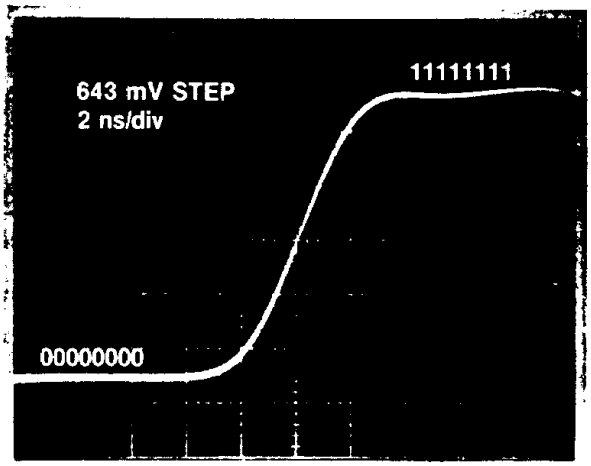


Figure 4. Full Scale Step Rise Time.

Current Output

The AH8308E can be used as a current output device by connecting the inverting input of an op-amp to the AH8308E output and then selecting the appropriate op amp feedback resistor for the required voltage output.

Timing

Figure 5 shows a detailed diagram depicting the timing required to generate composite video for the case of a full-scale (black to white) transition. 10% OVERBRIGHT, BLANKING PEDESTAL and SYNC are generated after the transition to illustrate their timing.

Cursor

To produce a cursor on a display, both 10% OVERBRIGHT and REF. WHITE should be brought to a logic "0" which will drive the output to 0V. If 10% OVERBRIGHT only is brought to logic "0", the output of the AH8308E will increase +0.064V above its prior output.

APPLICATION CONSIDERATIONS

Color Graphic Systems

The AH8308E is ideally suited for both monochrome composite video and RGB color applications. Normally only one channel (the green) carries the SYNC signal. For use in the other channels of such systems, the SYNC and BLANKING lines of the AH8308E can be disabled by tying them to logic "1".

While using a 4- or 5-bit DAC on each color channel may give the display system designer an acceptable color palette, the low resolution of these DACs may not be sufficient to allow anti-aliasing techniques to be employed successfully. One advantage to using an 8-bit DAC may not be readily apparent — one that is especially important in CAD/CAM type applications where single lines are drawn on the display. When a diagonal line is drawn on the screen, "bunching" of the pixels causes a stair-stepping effect as opposed to a smooth, straight line. Increased display resolution helps to reduce the size of the "jaggies" and smooth out the line, but cannot eliminate them. Various digital-differential analysis (DDA) procedures have been used to attempt to solve this problem and minimize its effect. By using a higher Z-axis resolution (8 bits versus 4 or 5), further improvements in the smoothing process are realized with these DDA procedures due to the increased control over the line intensity.

Broadcast Usage

The AH3808E is normally used in Digital Display applications. It can, however, be used for broadcast applications in which case additional circuitry is required in order to achieve full compliance with EIA Industrial Electronics Tentative Standard No. 1 (part of RS170A). This Standard details the exact waveform and timing characteristics of the broadcast composite video signal. The additional circuitry would, at a minimum, provide sinx/x correction and bandwidth filtering. In addition, the set-up on the AH8308E should be changed to 7.5 IRE units by placing a nominal 560Ω resistor between the SETUP terminal and ground.

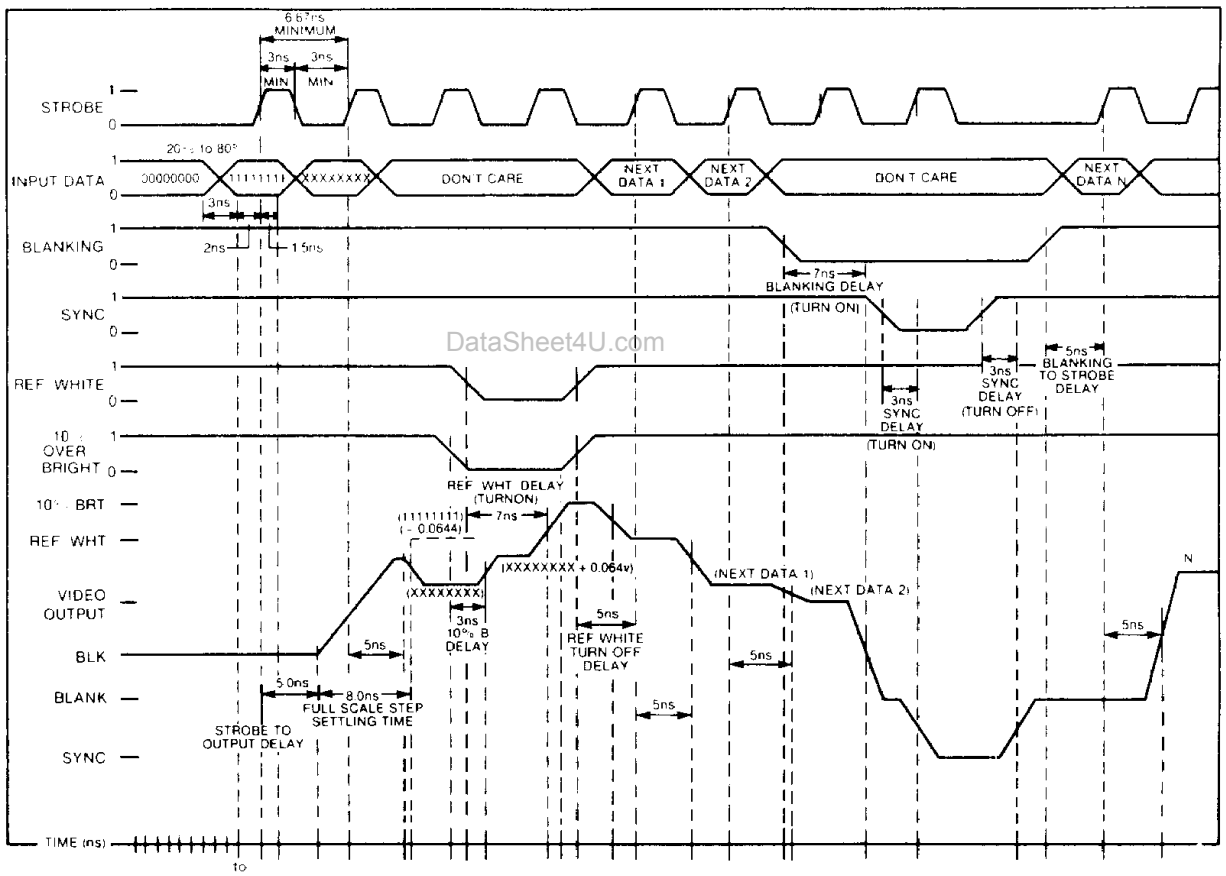


Figure 5. Typical Timing Diagram.

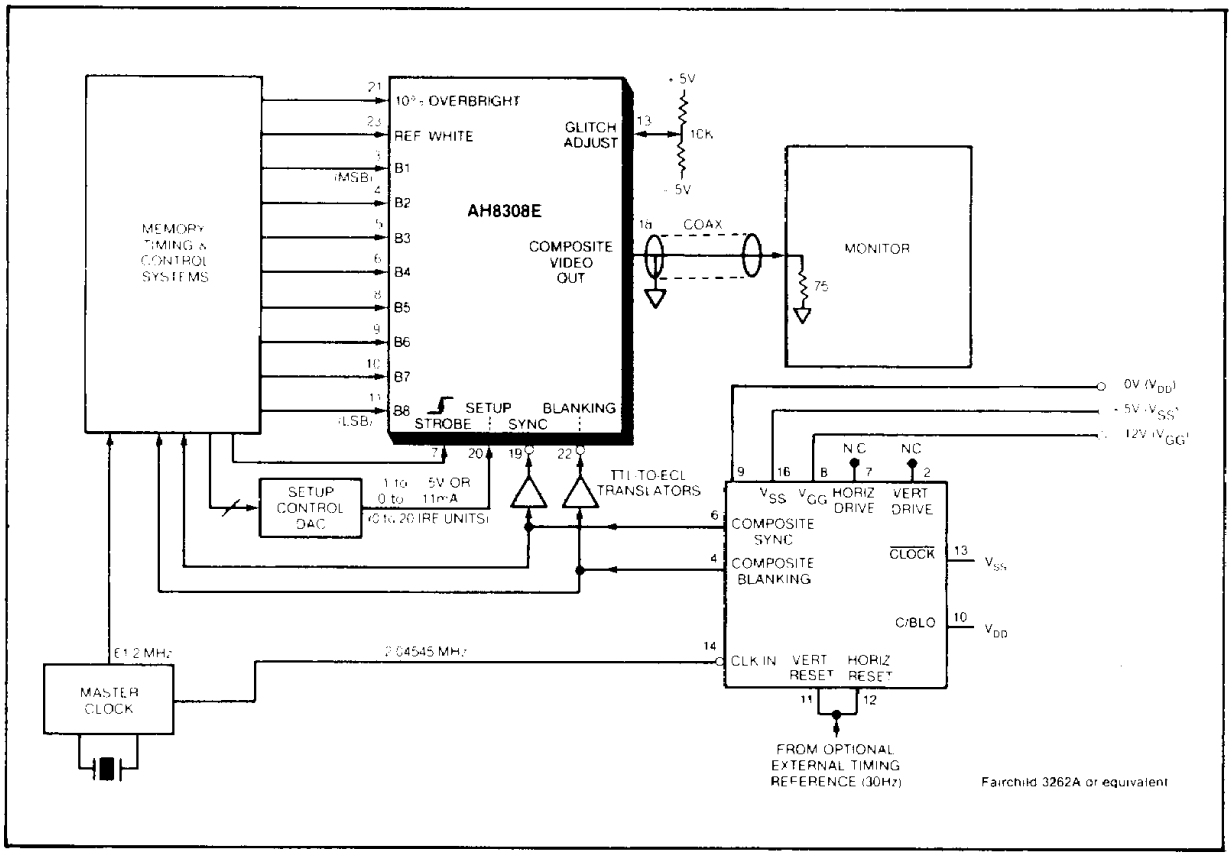


Figure 6. Typical AH8308E Application.

Video Display System Application

An example of a video display subsystem using the AH8308E is shown in block diagram form in Figure 6. Only the portion of the subsystem directly involving the AH8308E is shown. The memory and monitor circuits are not discussed in any detail, since system requirements vary. It is assumed that eight bits of digital data are available from some source for use by the AH8308E and that a monitor and/or sinx/x filter is being driven by the AH8308E. If fewer than eight bits are used, tie the unused LSBs to logic 0. Any AH8308E control signals not required in a particular system application should be tied to logic 1 to prevent erroneous operation. The timing relationships of the various signals are shown in Figure 5.

Timing for the overall display subsystem is derived from the system Master Clock. Through a suitable divider chain, a frequency of either 2.04 MHz is generated and applied to the clock input of the 3262A Sync Generator IC or equivalent (see Note*). From this clock signal, the 3262A generates the Sync and Blanking signals. The Composite Sync and Blanking Signals are applied to the corresponding control inputs on the AH8308E after first passing through TTL to ECL translators (all 3262A outputs are TTL). The Sync and Blanking signals are also sent to the Memory System for use by the Memory Address logic if required. The 3262A also produces a timing signal which is valid during the Vertical Interval at the start of the odd Field for interlaced systems. This signal may be used to control Memory addressing.

In most systems the "setup" level is left at one particular value such as the Standard 71 mV. In rare cases where the application requires, the setup level can be controlled digitally by means of a DAC with either a current or voltage output. If the SETUP pin is driven as a voltage point, values from −1 to −5V will produce 0 to 20 IRE units respectively. If a current is injected into the SETUP pin, approximately 11 mA is needed to produce 0 IRE units.

The composite video output from the AH8308E is connected directly to the (75Ω-terminated) video input of the monitor by a length of coax cable. The length of the cable should be limited to prevent the dc resistance of the cable run from exceeding 7.5Ω. If an amplifier is used between the AH8308E output and the monitor, longer lengths of cable can be allowed.

***PLEASE NOTE**

Comparable IC's providing similar functions to the 3262A are available from several manufacturers. The Fairchild part number 3262A is used by way of example, and no endorsement by Analogic of this part is intended or implied. Also, Analogic is not responsible for the accuracy of technical information supplied by other manufacturers.

The Video Signal

The EIA Standards RS170 and RS343 define the video signal in detail and refer to the IRE units for measuring the various components of the signal. The total peak amplitude of the standard video signal, from the maximum white level to the sync level is 140 IRE units. The standards further define the video signal as 1 Vp-p; therefore, 1 IRE unit is 7.14 mV. The maximum white level is the most positive amplitude of the video signal, and sync the most negative; this is referred to as a black-negative (as opposed to a black-positive) video signal. The illustration in Figure 7 depicts the composite video signal produced by the AH8308E.

The AH8308E provides a 10% Overbright feature which causes a negative shift in all of the various levels (i.e. Reference White, Reference Black, Blanking and Sync) by approximately 9 IRE units. The relative number of IRE units between each of these levels is compatible with the EIA Standards. As the definitions are given for the various levels in the AH8308E composite signal, it should be remembered that they differ from the standard RS170/RS343 absolute levels by 9 IRE units (0.064V).

The most positive amplitude level is the 10% Overbright. As its name implies, this level is higher than the whitest level of the picture information by 10% of the signal or 0.064V (10% of 0.643V). This level is most often used to define a cursor on a display screen. By making the cursor 10% brighter than the remainder of the picture, it can be located easily. REFERENCE WHITE is the most positive amplitude of the normal picture information, while REFERENCE BLACK is the most negative. The span of signal from REFERENCE WHITE to REFERENCE BLACK is 90 IRE units or 0.643V. This span is divided into 256 discrete levels (gray scale) because of the 8-bit resolution of the AH8308E.

The BLANKING LEVEL is 10 IRE units below REFERENCE BLACK in a standard video signal and is the voltage level that will completely cut off the display screen. The AH8308E provides a means of varying the relative distance between the REFERENCE BLACK and BLANKING LEVEL, referred to as the setup. The SETUP pin on the AH8308E can be programmed to provide a set-up of 0 mV., 71 mV or 142 mV (0 IRE, 10 IRE or 20 IRE units). Left open, the standard setup of 71 mV (10 IRE units) is produced. Tied to – 5V, 142 mV (20 IRE units) is produced; tied to ground, 0 mV (0 IRE units) is produced. The BLANKING LEVEL is also referred to as the PEDESTAL, BACK PORCH or FRONT PORCH.

(continued)

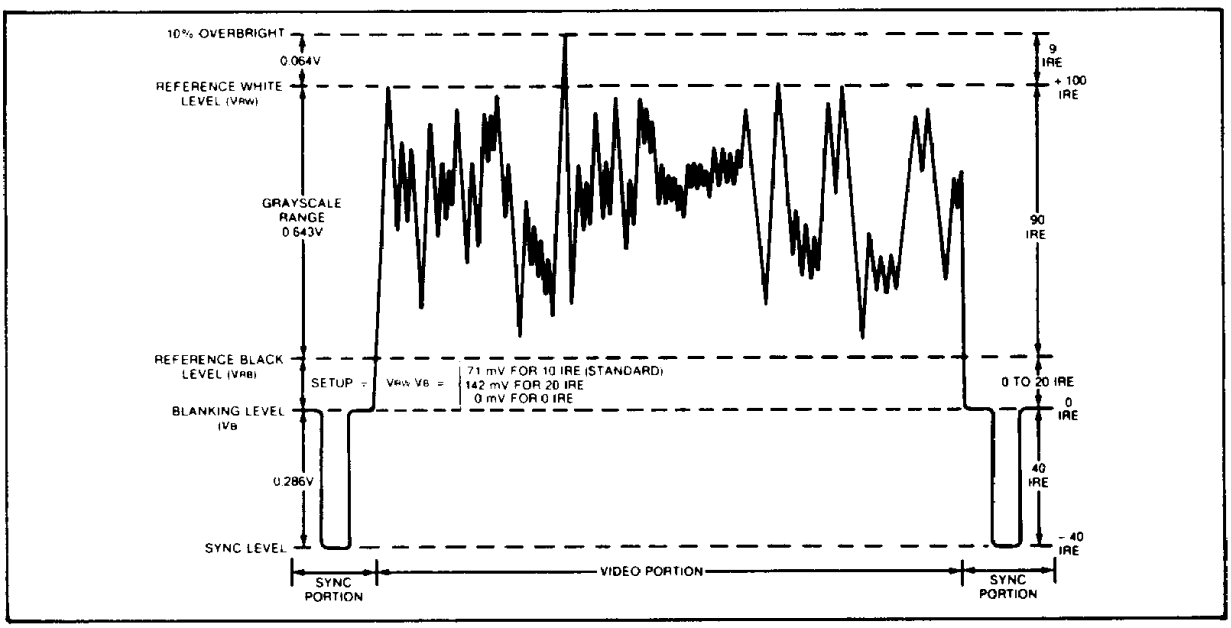


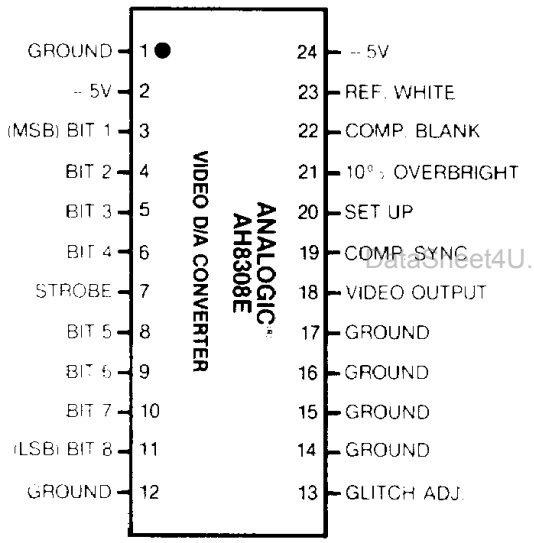
Figure 7. The Composite Video Signal (Not to Scale).

The Video Signal (cont.)

The most negative amplitude of video signal is the SYNC LEVEL at −40 IRE (0.286V) below the BLANKING LEVEL. Relative to 10% OVERBRIGHT, this level is −1.064V. The SYNC level is used to synchronize the scanning circuits in the display system. It is this sync level (along with BLANKING) produced directly by the AH8308E that provides the composite video signal.

All of the above definitions apply to both monochrome and color (RED/BLUE/GREEN) display systems. In color systems, the composite signal is produced on only one channel (usually the green). The other two DACs producing the Red and Blue video have the Sync and Blanking levels disabled by tying them to logic 1.

PINOUT

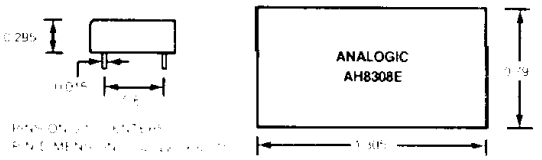


(TOP VIEW)

Available Options

The AH8308E is normally supplied with eight DATA INPUTS, STROBE, REFERENCE WHITE, 10% OVERBRIGHT, BLANKING and SYNC control inputs, capable of driving a 75 ohm terminated monitor. We invite inquiries on modifications such as dual monitor capability, REFERENCE BLACK CONTROL and other custom requirements.

MECHANICAL



CONTROL SIGNALS

SIGNAL	ACTIVE LOGIC LEVEL	RESULTANT OUTPUT
DATA, BIT 1—BIT 8	000 000 00	−0.707V (REF. BLK)
	111 111 11	−0.064V (REF. WHT)
STROBE	↓	DATA LOADED
REF. WHITE	0	−0.064V
COMP. BLANK	0	−0.778V
10% OVERBRIGHT	0	0V
COMP. SYNC	0	−1.064V
SETUP	OPEN	71 mV (10 IRE)
	−5.0V	−142 mV (20 IRE)
	GND	0 mV (0 IRE)

ORDERING GUIDE

150 MHz 8-Bit ECL Video DAC...

Specify **AH8308E**