PRODUCT BRIEF*

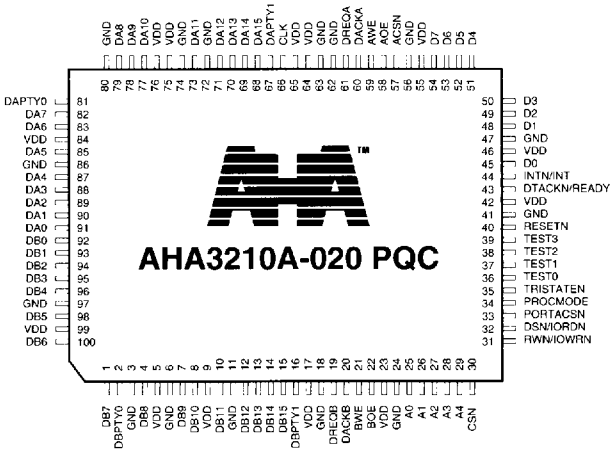
AHA3210

10 MBYTES/SEC DCLZ DATA COMPRESSION COPROCESSOR IC

The AHA3210 is a single chip lossless compression and decompression integrated circuit implementing the industry standard DCLZ algorithm. The device supports a sustained compression, decompression, or pass-through rate of 10 MBytes/sec. The high data rate and other high performance features make it suitable for many applications, such as, high performance laser printers or SCSI storage peripherals.

The Content Addressable Memory within the DCLZ engine eliminates external SRAMs typically required for dictionary storage or data buffering in a compression system. Other system features include two 24-bit counters, automatic multiple-record transfer support and compression ratio optimization.

The Data Compression Lempel Ziv (DCLZ) adaptive compression algorithm is approved by several standards organizations including QIC, DAT, ANSI, ISO and ECMA. DCLZ has been accepted by Hewlett-Packard and other system companies worldwide as their standard of choice. The algorithm exhibits an average compression ratio of 2 to 1.



FEATURES

HIGH PERFORMANCE:

- 10 MBytes/sec data compression, decompression, or pass-through rate
- 2 to 1 average compression ratio
- High compression of small records
- Automatic multiple-record transfers
- Dynamic compression ratio monitoring

FLEXIBILITY:

- In-Line and Look-Aside architectures supported
- Intelligent Dictionary control

SYSTEM INTERFACE:

- Single chip data compression solution
- No SRAM required
- 2 independent DMA ports programmable for 8 or 16-bit transfers
- Programmable interrupts
- Interfaces directly to AHA's tape controller/formatters and industry standard SCSI controllers

OTHERS:

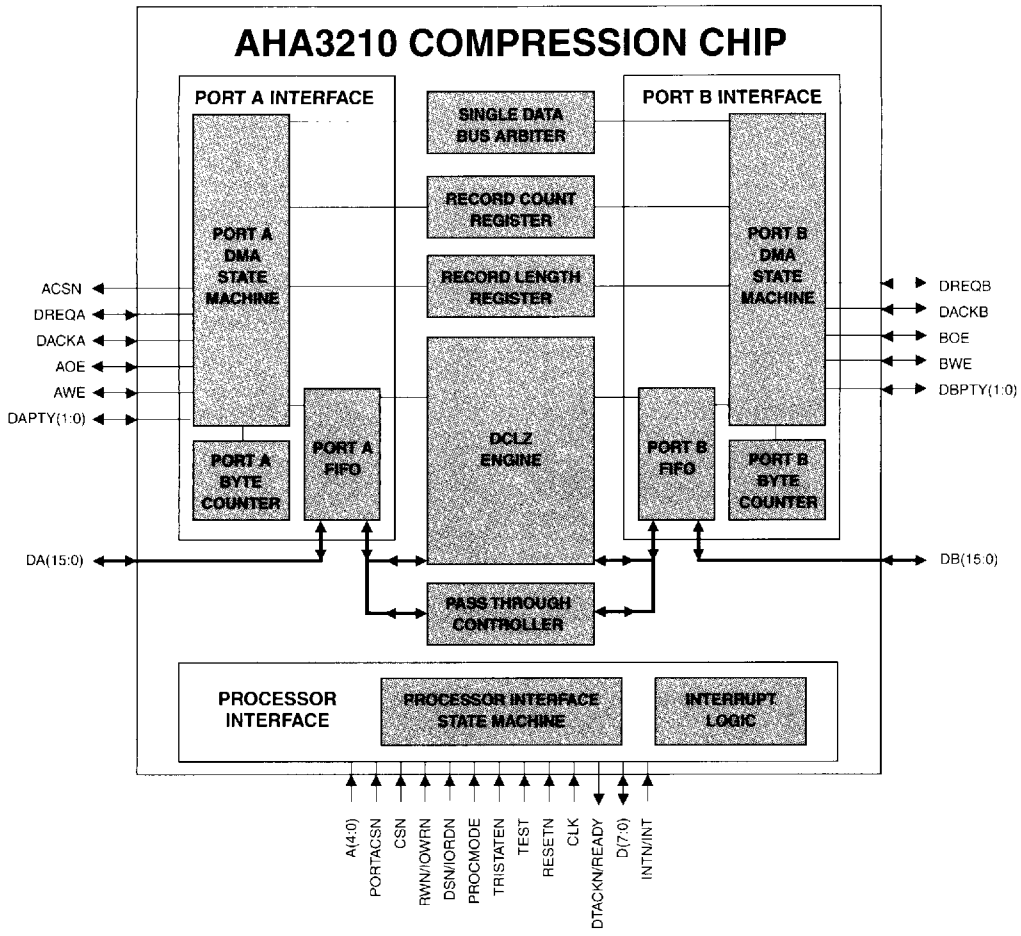
- Open standard DCLZ adaptive lossless compression algorithm
- Standards include: QIC, DDS/DAT, ANSI, ISO and ECMA
- Low power stand by operation
- EIAJ-standard 100-pin plastic quad flat package
- Higher speed, testing and packaging options available
- Software emulation of the algorithm available

APPLICATIONS

- High performance laser printers
- DDS/Data DAT helical scan tape drives
- QIC or 8mm tape drives
- High performance disk drives
- High speed data communication systems
- SCSI host-bus adapters

Advanced Hardware Architectures

*Request the *AHA3210* Product Specification for complete details



FUNCTIONAL DESCRIPTION

The AHA3210 may be used in compression, decompression or pass-through modes. These modes, along with other features, are fully described in the *AHA3210 Product Specification.*

The two bi-directional DMA ports, A and B, are used to transfer data through the AHA3210 device. In compression mode, uncompressed data flows into Port A and is compressed by the DCLZ engine. The compressed data is then transferred out of Port B. Decompression is the opposite with data flowing into Port B, being decompressed by the DCLZ engine, and then flowing out of Port A. In pass through mode, data moves from either port to the other unchanged. An optional single data bus mode allows Ports A and B DMA interfaces to transfer data on a shared data bus.

THE DCLZ DATA COMPRESSION ALGORITHM

The DCLZ algorithm removes redundancy from data by recognizing and encoding patterns of input characters. Each time a unique string of characters occurs, it is entered into a dictionary located within the DCLZ engine and is assigned a numeric value or codeword. Subsequent occurrences of dictionary entries are replaced by their associated codewords.

The dictionary contains up to 4K entries with each representing a string of up to 128 characters. One of the fundamental advantages of DCLZ is that the dictionary is embedded in the transmitted codewords, saving time and storage space.

Once the dictionary has been developed, it may be shared across file or record boundaries, thus maximizing the compression achieved on small records or files.

DCLZ is a lossless algorithm, insuring that the decompressed data output is exactly the same as the uncompressed data input.

SYSTEMS APPLICATIONS

A typical application for the AHA3210 is the implementation of data compression in a tape drive system using AHA5102 or 5122 tape controllers. An in-line architecture is employed in this system.

The in-line application inserts compression directly between the host and the system data buffer. There is no direct connection between the buffer and the host. For compression, data flows from the host, through the bus controller and into the AHA3210. The data is then compressed by the DCLZ machine and flows into the system buffer followed by the tape drive interface. This data flow is usually controlled by a local microprocessor. For decompression, the flow is reversed.

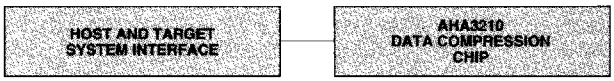
In an in-line architecture the AHA compression chip operates at the data rate of the host interface controller. The AHA3210 device supports a sustained data transfer rate of up to 10 MBytes/sec.

In a look-aside application, the system buffer is in series with the data flow. There is a direct connection between the host and the buffer memory through a DMA port. For compression, data flows from the host, through the bus interface and peripheral controllers and into the system buffer. Data then flows from the system buffer into the AHA3210 where it is compressed and sent back to the system buffer. Finally, data is transferred from the system buffer interface. During decompression, this flow is reversed.

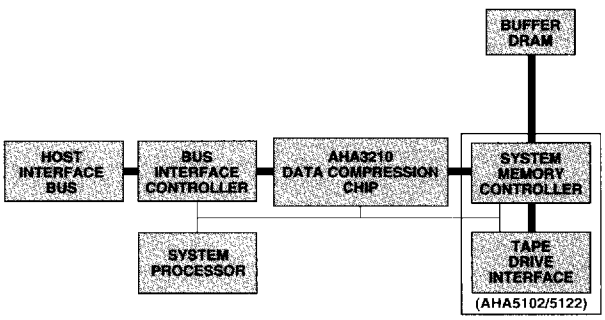
The AHA3210 is covered by one or more patents.

IN-LINE ARCHITECTURE

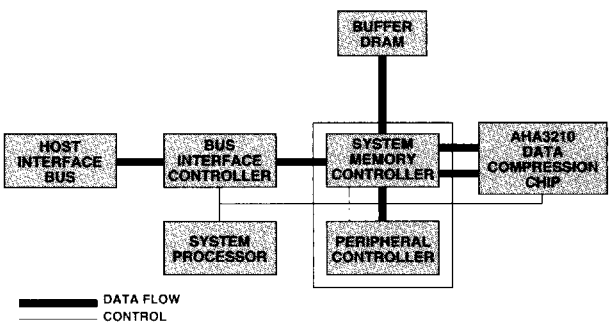
LOOK-ASIDE ARCHITECTURE



EXAMPLE IN-LINE APPLICATION



EXAMPLE LOOK-ASIDE APPLICATION



AHA3210 REGISTER ADDRESS MAP

ADDRESS	READ	WRITE
0x00	DCLZ Control Register	DCLZ Control Register
0x01	DCLZ Status Register	Reserved
0x02	Comp. Ratio Optimization Register	Comp. Ratio Optimization Register
0x03	DMA Configuration Register	DMA Configuration Register
0x04	Port A Control Register 0	Port A Control Register 0
0x05	Port A Control Register 1	Port A Control Register 1
0x06	Port A Status Register	Reserved
0x07	Port A Byte Count (7:0)	Port A Byte Count (7:0)
0x08	Port A Byte Count (15:8)	Port A Byte Count (15:8)
0x09	Port A Byte Count (23:16)	Port A Byte Count (23:16)
0x0A	Port B Control Register 0	Port B Control Register 0
0x0B	Port B Control Register 1	Port B Control Register 1
0x0C	Port B Status Register	Reserved
0x0D	Port B Byte Count (7:0)	Port B Byte Count (7:0)
0x0E	Port B Byte Count (15:8)	Port B Byte Count (15:8)
0x0F	Port B Byte Count (23:16)	Port B Byte Count (23:16)
0x10	Port B Byte Comparator (7:0)	Port B Byte Comparator (7:0)
0x11	Port B Byte Comparator (15:8)	Port B Byte Comparator (15:8)
0x12	Port B Byte Comparator (23:16)	Port B Byte Comparator (23:16)
0x13	Record Length Register (7:0)	Record Length Register (7:0)
0x14	Record Length Register (15:8)	Record Length Register (15:8)
0x15	Record Length Register (23:16)	Record Length Register (23:16)
0x16	Record Count Register (7:0)	Record Count Register (7:0)
0x17	Record Count Register (15:8)	Record Count Register (15:8)
0x18	Record Count Register (23:16)	Record Count Register (23:16)
0x19	Interrupt Status Register	Interrupt Clear Register
0x1A	Interrupt Disable Register	Interrupt Disable Register
0x1F	Identification Register	Reserved

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
AHA3210A-020 PQC	Data Compression Coprocessor IC

TECHNICAL PUBLICATIONS

DOCUMENT #	DESCRIPTION
PS3210	AHA3210 Product Specification
PS3101	AHA3101 Product Specification, DCLZ 2.5 MBytes/sec.
ANDC01	Primer: Data Compression Lempel Ziv
ANDC04	Data Management for the AHA3210 Data Compression Coprocessor
ANDC05	AHA3210 Designer's Guide
ABDC02	DCLZ Software Licensing Procedure
ABSTD1	AHA Data Compression and Reed-Solomon Standards
GLGEN1	General Glossary of Terms
RAECMA-0791	"DCLZ Emerges as an Open Data Compression Standard," article reprint *Computer Technology Review*, Summer 1991
STDEMO	DCLZ Demonstration Disk (PC Compatible)

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