AT27LV512R

T-46-13-29
T-46-13-25

Features

- Wide Power Supply Range, 3.0 VDC to 5.5 VDC
- Compatible with JEDEC Standard AT27C512R
- Low Power 3-Volt CMOS Operation
  - 100 µA max. Standby
  - 26mW max. Active at 3.3 MHz for V_{CC} = 3.3 VDC
  - 110mW max. Active at 5 MHz for V_{CC} = 5.5 VDC
- Read Access Time - 300ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP or SOIC
  - 32-Pad LCC and OTP PLCC
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

512K (64K x 8) Low Voltage UV Erasable CMOS EPROM

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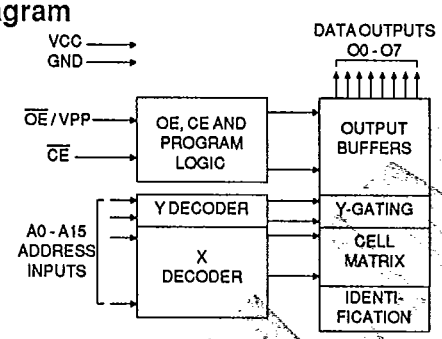
Preliminary

Block Diagram



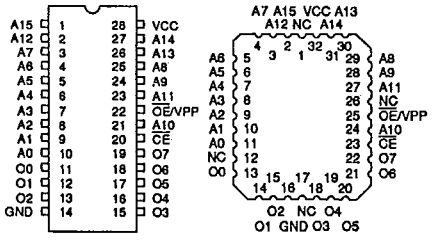
Description

The AT27LV512R chip is a low power, low voltage 524,288 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 64K x 8 bits. It requires only one supply in the range of 3.0 to 5.5 VDC in normal read mode operation, making it ideal for battery powered systems.

With a typical power draw of only 18mW at 3.3 MHz and V_{CC} at 3.3 VDC, the AT27LV512R will draw less than one fifth the power of a standard 5 volt EPROM. Standby mode supply current is typically less than 20µA.

Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$ /V_{PP}	Output Enable
NC	No Connect



Note: LCC Package Pins 1 and 17 are DON'T CONNECT.

Description (Continued)

The AT27LV512R comes in a choice of industry standard JEDEC-approved ceramic packages including; 28-pin DIP ceramic or one time programmable (OTP) plastic, 28-pin OTP plastic small outline (SOIC), and 32-pad leadless chip carrier (LCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

The AT27LV512R operating with V_{CC} at 3.0 VDC produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0 VDC.

Atmel's 27LV512R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV512R programs identically as an AT27C512R.

Erasure Characteristics

The entire memory array of the AT27LV512R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is 6.5V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	Vcc	Outputs
Read	V_{IL}	V_{IL}	Ai	Vcc	DOUT
Output Disable	V_{IL}	V_{IH}	X(1)	Vcc	High Z
Standby	V_{IH}	X	X	Vcc	High Z
Rapid Program(2)	V_{IL}	V_{PP}	Ai	Vcc (2)	DIN
PGM Verify (2)	V_{IL}	V_{IL}	Ai	Vcc (2)	DOUT
PGM Inhibit (2)	V_{IH}	V_{PP}	X	Vcc (2)	High Z
Product Identification(2),(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A15=V_{IL}	Vcc (2)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics. Programming modes require V_{CC} > 4.5 V.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

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		AT27LV512R -30
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
Vcc Power Supply		3.0V to 5.5V

D.C. and Operating Characteristics for Read Operation

(VCC = 3.0V to 5.5V unless otherwise specified)

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC}+1V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC}+0.1V				10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0V				100	µA
		I_{SB2} (TTL), $\overline{CE}$=2.0 to V_{CC}+1.0V				1	mA
I_{CC}	V_{CC} Active Current	I_{CC1}	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}, V_{CC} = 5.5V	Com.		20	mA
				Ind.		25	mA
		I_{CC2}	f = 3.33MHz, I_{OUT} = 0mA $\overline{CE}$ = V_{IL}, V_{CC} = 3.3V	Com.		8	mA
				Ind.		10	mA
V_{IL}	Input Low Voltage	V_{IL1}	4.5 ≤ V_{CC} ≤ 5.5V		-0.6	0.8	V
		V_{IL2}	3.0 ≤ V_{CC} < 4.5V		-0.6	0.6	V
V_{IH}	Input High Voltage				2.0	6.5	V
V_{OL}	Output Low Voltage	V_{OL1}	I_{OL} = 2.1mA, V_{CC} = 4.5V			.45	V
		V_{OL2}	I_{OL} = 1.0mA, V_{CC} = 3.0V			0.3	V
V_{OH}	Output High Voltage	I_{OH} = -100µA			V_{CC}-0.3		V
		I_{OH} = -400µA			2.4		V

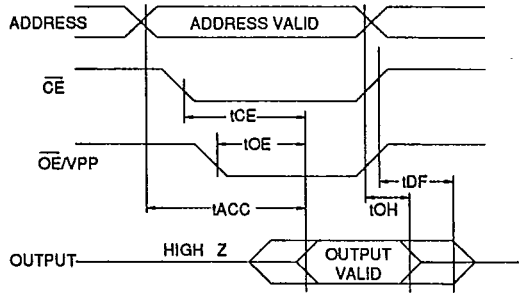
Notes: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$.

A.C. Characteristics for Read Operation (VCC = 3.0V to 5.5V)

Symbol	Parameter	Condition		AT27LV512R -30 Min	AT27LV512R -30 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$=$\overline{OE}/V_{PP}$=V_{IL}	Com.		270	ns
			Ind.		270	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}$=V_{IL}			300	ns
t_{OE} (2,3)	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}$=V_{IL}			150	ns
t_{DF} (4,5)	$\overline{OE}/V_{PP}$ High to Output Float	$\overline{CE}$=V_{IL}			100	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first	$\overline{CE}$=$\overline{OE}/V_{PP}$ =V_{IL}			0	ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

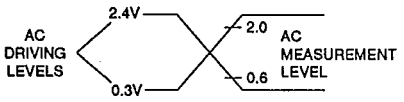
A.C. Waveforms for Read Operation (1)



Notes:
1. 3V timing measurement references are 0.6V and 2.0V. Input AC driving levels are 0.3V and 2.4V. See Input Test Waveforms and Measurement Levels.
2. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

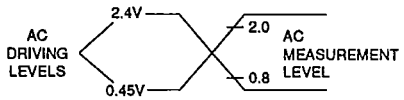
Input Test Waveforms and Measurement Levels

(VCC = 3.0V)



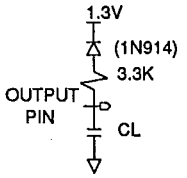
t_R, t_F < 20ns (10% to 90%)

(VCC = 5.5V)



t_R, t_F < 20ns (10% to 90%)

Output Test Load



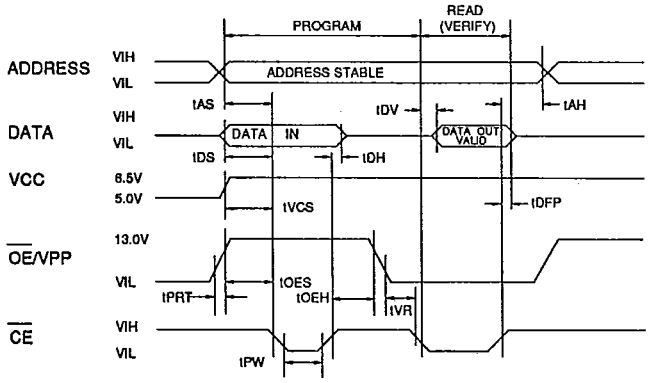
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) (1)

	Typ	Max-	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for 5V supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms (1)



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{OE}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{OE}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{DV}	Data Valid from $\overline{CE}$	(Note 2)		1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

Notes:

1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

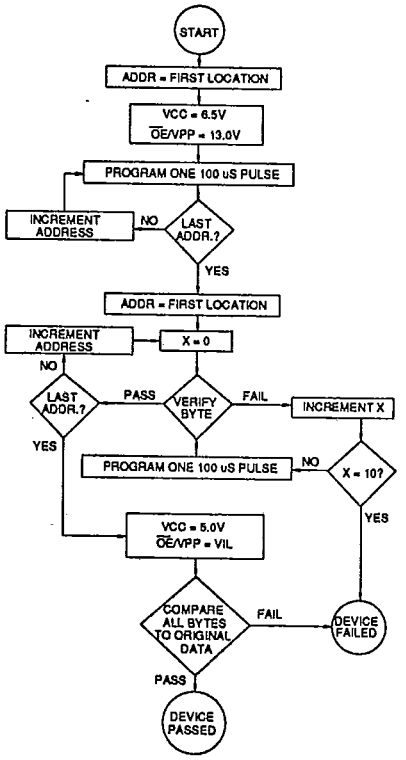
Atmel's 27LV512R Integrated Product Identification Code[1]

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	0	1	0D

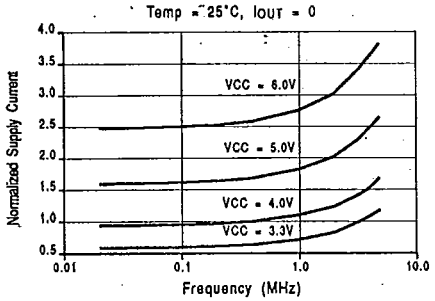
Note: 1. The AT27LV512R has the same Product Identification Code as the AT27C512R. Both are programming compatible.

Rapid Programming Algorithm

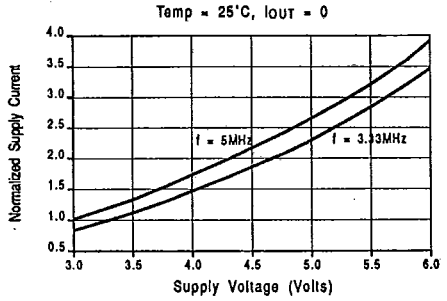
A 100µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



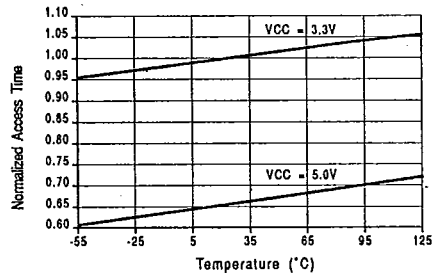
NORMALIZED SUPPLY CURRENT vs. FREQUENCY
Temp = 25°C, IOUT = 0



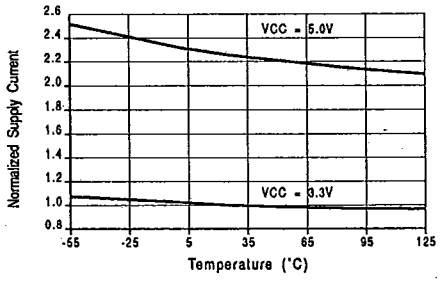
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE
Temp = 25°C, IOUT = 0



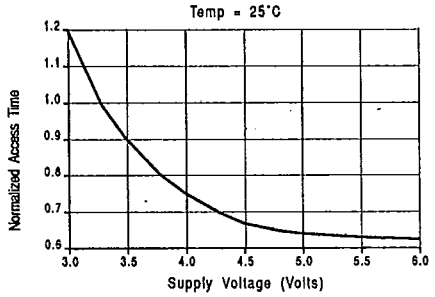
NORMALIZED ACCESS TIME vs. TEMPERATURE



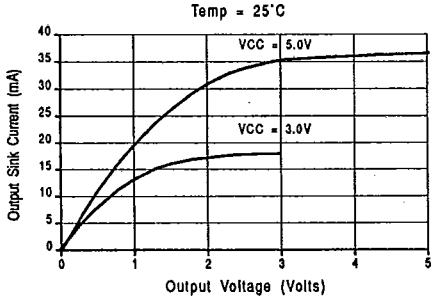
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE
Frequency = 3.33MHz, IOUT = 0



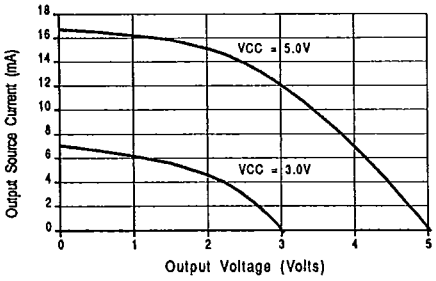
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE
Temp = 25°C



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE
Temp = 25°C



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE
Temp = 25°C



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Ordering Information

t_{ACC} (ns)	Icc (mA) Active (3.3)	Icc (mA) Standby	Ordering Code	Package	Operation Range
270	8	0.1	AT27LV512R-30DC AT27LV512R-30JC AT27LV512R-30LC AT27LV512R-30PC AT27LV512R-30RC	28DW6 32J 32LW 28P6 28R	Commercial (0°C to 70°C)
270	10	0.1	AT27LV512R-30DI AT27LV512R-30LI	28DW6 32LW	Industrial (-40°C to 85°C)

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Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)