HB526A264EN-10/12

1,048,576-word × 64-bit × 2 bank (Non Parity) Synchronous Dynamic RAM Module
168-pin JEDEC Standard Outline Unbuffered 8 byte DIMM

HITACHI

ADE-203-485B (Z)
Rev. 2.0
Apr. 29, 1996

Description

The HB526A264EN belongs to 8 Byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 8 Byte processor applications.

The HB526A264EN is a 1M × 64 × 2 bank synchronous dynamic RAM module, mounted 8 pieces of 16-Mbit SDRAM (HM5216805TT) sealed in TSOP package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). An outline of the HB526A264EN is 168-pin socket type package (dual lead out). Therefore, the HB526A264EN makes high density mounting possible without surface mount technology. The HB526A264EN provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

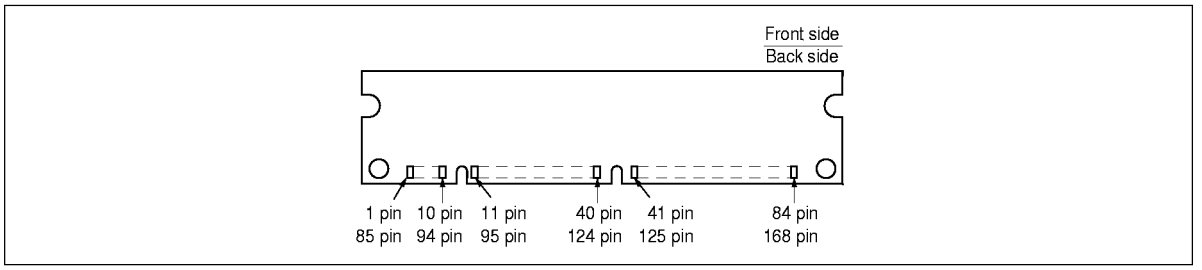
Features

- 168-pin socket type package (Dual lead out)
  — Lead pitch: 1.27 mm
- 3.3 V (+/–0.3 V) supply
- Interface: LVTTL
- Clock frequency: 100MHz/83MHz
- Data bus width: × 64 (Non Parity) bit
- Single pulsed $\overline{RAS}$
- 2 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length: 1/2/4/8/Full page
- Programmable burst sequential: Sequential/interleave
- Full page burst length capability: Sequential burst/burst stop capability
- Programmable $\overline{CAS}$ latency: 2/3
- 4,096 refresh cycles: 64 ms
- 2 variation of refresh: Auto refresh/Self refresh

Ordering Information

Type No.	Frequency	Package	Contact pad
HB526A264EN-10	100 MHz	168-pin dual lead out socket type	Gold
HB526A264EN-12	83 MHz		

Pin Arrangement



Pin Arrangement

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	13	DQ9	25	NC	37	A8
2	DQ0	14	DQ10	26	V_{CC}	38	A10
3	DQ1	15	DQ11	27	$\overline{WE}$	39	NC
4	DQ2	16	DQ12	28	DQMB0	40	V_{CC}
5	DQ3	17	DQ13	29	DQMB1	41	V_{CC}
6	V_{CC}	18	V_{CC}	30	$\overline{S0}$	42	CK0
7	DQ4	19	DQ14	31	NC	43	V_{SS}
8	DQ5	20	DQ15	32	V_{SS}	44	NC
9	DQ6	21	NC	33	A0	45	$\overline{S2}$
10	DQ7	22	NC	34	A2	46	DQMB2
11	DQ8	23	V_{SS}	35	A4	47	DQMB3
12	V_{SS}	24	NC	36	A6	48	NC

Pin Arrangement (cont)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
49	V_{CC}	79	NC	109	NC	139	DQ48
50	NC	80	NC	110	V_{CC}	140	DQ49
51	NC	81	NC	111	$\overline{CAS}$	141	DQ50
52	NC	82	SDA	112	DQMB4	142	DQ51
53	NC	83	SCL	113	DQMB5	143	V_{CC}
54	V_{SS}	84	V_{CC}	114	NC	144	DQ52
55	DQ16	85	V_{SS}	115	$\overline{RAS}$	145	NC
56	DQ17	86	DQ32	116	V_{SS}	146	NC
57	DQ18	87	DQ33	117	A1	147	NC
58	DQ19	88	DQ34	118	A3	148	V_{SS}
59	V_{CC}	89	DQ35	119	A5	149	DQ53
60	DQ20	90	V_{CC}	120	A7	150	DQ54
61	NC	91	DQ36	121	A9	151	DQ55
62	NC	92	DQ37	122	A11	152	V_{SS}
63	NC	93	DQ38	123	NC	153	DQ56
64	V_{SS}	94	DQ39	124	V_{CC}	154	DQ57
65	DQ21	95	DQ40	125	NC	155	DQ58
66	DQ22	96	V_{SS}	126	NC	156	DQ59
67	DQ23	97	DQ41	127	V_{SS}	157	V_{CC}
68	V_{SS}	98	DQ42	128	CKE	158	DQ60
69	DQ24	99	DQ43	129	NC	159	DQ61
70	DQ25	100	DQ44	130	DQMB6	160	DQ62
71	DQ26	101	DQ45	131	DQMB7	161	DQ63
72	DQ27	102	V_{CC}	132	NC	162	V_{SS}
73	V_{CC}	103	DQ46	133	V_{CC}	163	NC
74	DQ28	104	DQ47	134	NC	164	NC
75	DQ29	105	NC	135	NC	165	SA0
76	DQ30	106	NC	136	NC	166	SA1
77	DQ31	107	V_{SS}	137	NC	167	SA2
78	V_{SS}	108	NC	138	V_{SS}	168	V_{CC}

Pin Description

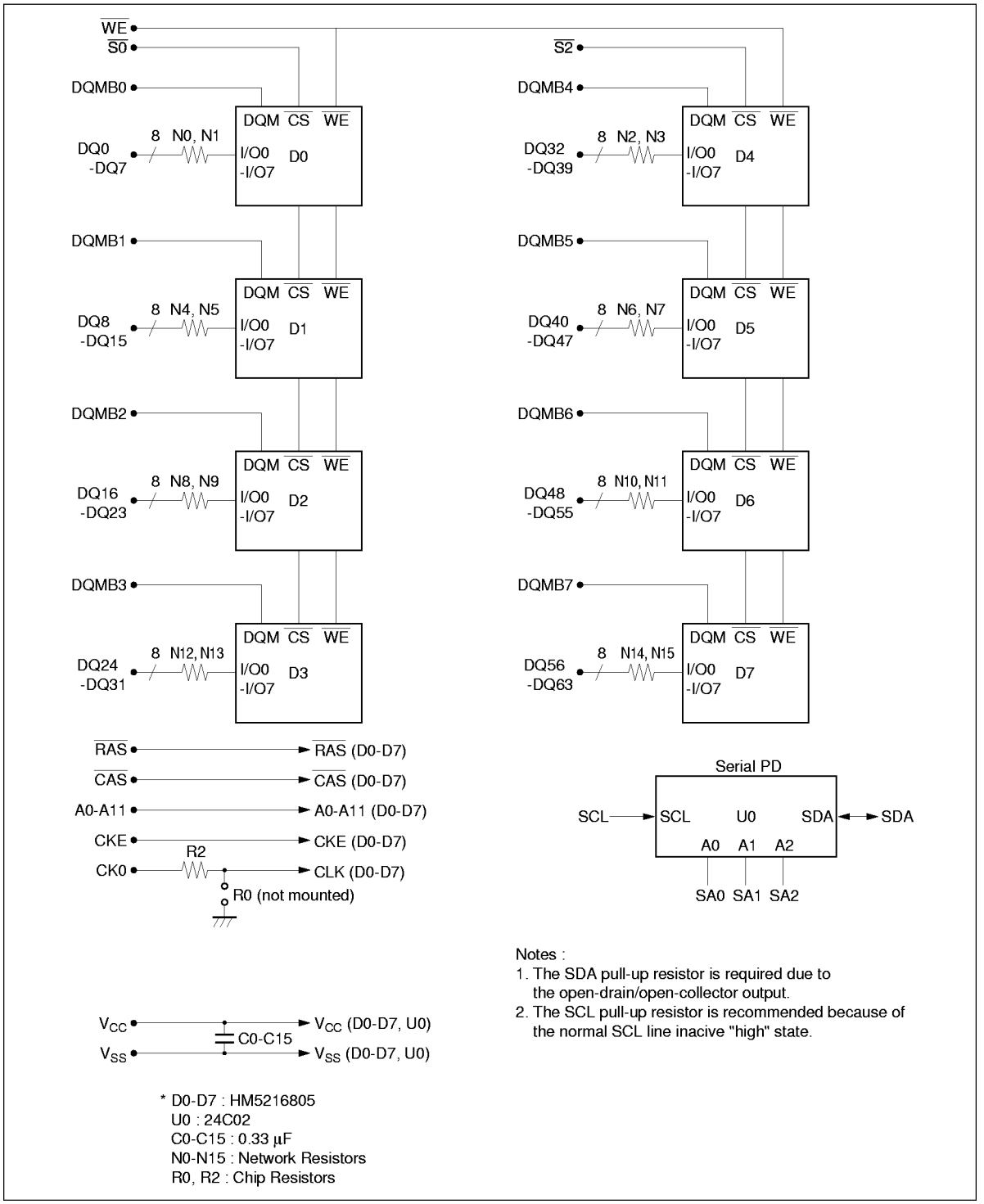
Pin name	Function
A0 to A11	Row address: A0 to A10 Column address: A0 to A8 Bank select address: A11
DQ0 to DQ63	Data in/Data-output
$\overline{S0}$, $\overline{S2}$ ($\overline{CS0}$, $\overline{CS2}$)	Chip select
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQMB0 to DQMB7 (DQM0 to DQM7)	Input/Output mask
CK0 (CLK0)	Clock input
CKE	Clock enable
SDA	Serial data-in/data-out
SCL	Serial clock
SA0 to SA2	Serial address input
V_{cc}	Power supply
V_{ss}	Ground
NC	Non connection

Serial PD Matrix

Byte Number	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Notes
0	Number of bytes utilized by module manufacturer	0	0	0	1	0	1	0	1	21
1	Total number bytes in serial PD device	0	0	0	0	1	0	0	0	256 byte
2	Memory type	0	0	0	0	0	1	0	0	SDRAM
3	Number of row addresses	0	0	0	0	1	0	1	1	11
4	Number of column addresses	0	0	0	0	1	0	0	1	9
5	Number of DIMM banks	0	0	0	0	0	0	0	1	1
6	Module data width	0	1	0	0	0	0	0	0	64
7	Module data width (continued)	0	0	0	0	0	0	0	0	0 (+)
8	Module supply voltage/interface levels	0	0	0	0	0	0	0	1	3.3 V
9	SDRAM cycle time 10 ns	1	0	1	0	0	0	0	0	CL = 3
	SDRAM cycle time 12 ns	1	1	0	0	0	0	0	0	CL = 3
10	SDRAM access from clock 8 ns	1	0	0	0	0	0	0	0	CL = 3
	SDRAM access from clock 9.5 ns	1	0	0	1	0	1	0	1	CL = 3
11	SDRAM DIMM configuration type	0	0	0	0	0	0	0	0	None
12	Refresh rate/type	1	0	0	0	0	0	0	0	Normal (15.625 µs) Self refresh
13	SDRAM module attributes	0	0	0	0	0	0	0	0	
14	SDRAM device attributes: General	0	0	0	0	1	1	1	0	
15	SDRAM device attributes: minimum clock delay, back-to-back random column addresses	0	0	0	0	0	0	0	1	1
16	SDRAM device attributes: Burst lengths supported	1	0	0	0	1	1	1	1	1, 2, 4, 8, full page
17	SDRAM device attributes: number of banks on SDRAM device	0	0	0	0	0	0	1	0	2
18	SDRAM device attributes: $\overline{CAS}$ latency	0	0	0	0	0	1	1	0	2, 3
19	SDRAM device attributes: $\overline{CS}$ latency	0	0	0	0	0	0	0	1	0
20	SDRAM device attributes: $\overline{WE}$ latency	0	0	0	0	0	0	0	1	0

Note: 1. Serial PD data are not protected.
0: Serial data, “driven to Low”
1: Serial data, “driven to High”

Block Diagram



Notes :
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacive "high" state.

* D0-D7 : HM5216805
U0 : 24C02
C0-C15 : 0.33 µF
N0-N15 : Network Resistors
R0, R2 : Chip Resistors

Command Operation, Mode Register Configuration and Operation

Refer to the HM5216805 Series data sheet.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	8	W
Operating temperature	Topr	0 to +65	°C
Storage temperature	Tstg	–55 to +125	°C

Electrical Characteristics

Recommended DC Operating Conditions (Ta = 0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	4.6	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}
2. V_{IH} (max) = 5.5 V for pulse with ≤ 5 ns
3. V_{IL} (min) = –1.0 V for pulse with ≤ 5 ns

DC Characteristics (Ta = 0 to 65°C, V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V)

		HB526A264EN						
		-10		-12				
Parameter	Symbol	Min	Max	Min	Max	Unit	Test condition	Note
Operating current	I_{CC1}	—	800	—	680	mA	Burst length = 1 t_{RC} = min	1, 2, 4
Standby current (Bank Disable)	I_{CC2}	—	24	—	24	mA	CKE = V_{IL}, t_{CK} = min	5
		—	16	—	16	mA	CKE = V_{IL} CLK = V_{IL} or V_{IH} Fixed	6
		—	240	—	200	mA	CKE = V_{IH}, NOP command t_{CK} = min	3
Active standby current (Bank active)	I_{CC3}	—	56	—	56	mA	CKE = V_{IL}, t_{CK} = min, I/O = High-Z	1, 2
		—	280	—	240	mA	CKE = V_{IH}, NOP command t_{CK} = min, I/O = High-Z	1, 2, 3
Burst operating current (CL = 2)	I_{CC4}	—	800	—	680	mA	t_{CK} = min, BL = 4	1, 2, 4
Burst operating current (CL = 3)	I_{CC4}	—	1200	—	1000	mA		
Auto refresh current	I_{CC5}	—	680	—	560	mA	t_{RC} = min	
Self refresh current	I_{CC6}	—	16	—	16	mA	$V_{IH} \geq V_{CC}$ –0.2 0V ≤ V_{IL} ≤ 0.2	7
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 ≤ Vin ≤ V_{CC}	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 ≤ Vout ≤ V_{CC} I/O = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = –2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ±0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	60	pF	1
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CLK, CKE)	C_{I2}	—	60	pF	1
Input capacitance ($\overline{CS}$)	C_{I3}	—	40	pF	1
Input capacitance (DQM)	C_{I4}	—	25	pF	1
I/O capacitance (DQ0 to 63)	$C_{I/O1}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 65°C, V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V)

		HB526A264EN					
		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
System clock cycle time (CL = 2)	t_{CK}	15	—	18	—	ns	1
System clock cycle time (CL = 3)	t_{CK}	10	—	12	—		
CLK high pulse width	t_{CKH}	3	—	4	—	ns	1
CLK low pulse width	t_{CKL}	3	—	4	—	ns	1
Access time from CLK (CL = 2)	t_{AC}	—	9.5	—	12	ns	1, 2
Access time from CLK (CL = 3)	t_{AC}	—	8	—	9.5		
Data-out hold time	t_{OH}	3	—	3	—	ns	1, 2
CLK to Data-out low impedance	t_{LZ}	0	—	0	—	ns	1, 2, 3
CLK to Data-out high impedance (CL = 2, 3)	t_{HZ}	—	7	—	9	ns	1, 4
Data in setup time	t_{DS}	2	—	3	—	ns	1
Data in hold time	t_{DH}	1	—	1	—	ns	1
Address setup time	t_{AS}	2	—	3	—	ns	1
Address hold time	t_{AH}	1	—	1	—	ns	1
CKE setup time	t_{CES}	2	—	3	—	ns	1, 5
CKE setup time for power down exit	t_{CESP}	2	—	3	—	ns	1
CKE hold time	t_{CEH}	1	—	1	—	ns	1
Command setup time	t_{CS}	2	—	3	—	ns	1
Command hold time	t_{CH}	1	—	1	—	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	—	108	—	ns	

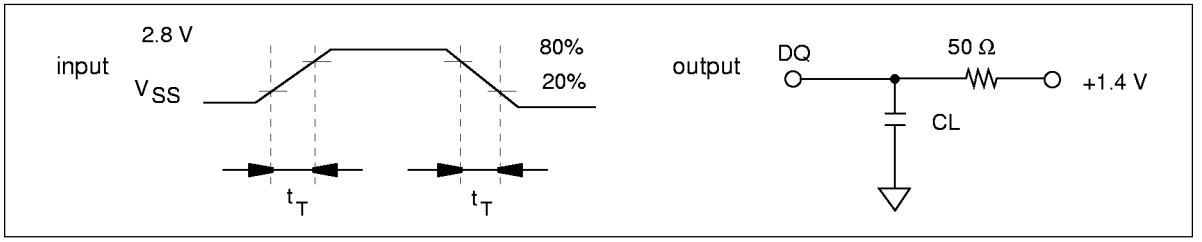
AC Characteristics (Ta = 0 to 65°C, V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V) (cont)

		HB526A264EN					
		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Active to precharge command period	t_{RAS}	60	120000	72	120000	ns	1
Active to precharge on full page mode	t_{RASC}	—	120000	—	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	—	36	—	ns	1
Precharge to active command period	t_{RP}	30	—	36	—	ns	1
The last data-in the precharge lead time	t_{RWL}	15	—	18	—	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	—	24	—	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	ns	
Refresh period	t_{REF}	—	64	—	64	ms	

Notes: 1. AC measurement assumes t_T = 1 ns. Reference level for timing of input signal is 1.40 V.
2. Access time is measured at 1.40 V. Load condition is C_L = 50 pF with current source.
3. t_{LZ} (max) defines the time at which the outputs achieves the low impedance state.
4. t_{HZ} (max) defines the time at which the outputs achieves the high impedance state.
5. t_{CES} defines CKE setup time to CKE rising edge except power down exit command.

Test condition

- Input and output timing reference levels: 1.4 V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter		HB526A264EN						
		-10			-12			
Frequency (MHz)		100	66	33	83	55	28	
t_{CK} (ns)	Symbol	10	15	30	12	18	36	Notes
Active command to column command (same bank)	t_{RCD}	3	2	1	3	2	1	
Active command to active command (same bank)	t_{RC}	9	6	3	9	6	3	= [t_{RAS} + t_{RP}]
Active command to precharge command (same bank)	t_{RAS}	6	4	2	6	4	2	
Precharge command to active command (same bank)	t_{RP}	3	2	1	3	2	1	
Last data input to precharge command (same bank)	t_{RWL}	2	1	1	2	1	1	
Active command to active command (different bank)	t_{RRD}	2	2	1	2	2	1	
Self refresh exit time	l_{SREX}	2	2	2	2	2	2	
Last data in to active command (Auto precharge, same bank)	l_{APW}	5	3	2	5	3	2	= [t_{RWL} + t_{RP}]
Self refresh exit to command input	l_{SEC}	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedance ($\overline{CAS}$ latency = 3)	l_{HZP}	3	3	3	3	3	3	
Precharge command to high impedance ($\overline{CAS}$ latency = 2)	l_{HZP}	—	2	2	—	2	2	
Last data out to precharge (auto precharge) (same bank)	l_{APR}	1	1	1	1	1	1	
Last data out to active command (early precharge) ($\overline{CAS}$ latency = 3)	l_{EP}	–2	–2	–2	–2	–2	–2	
Last data out to active command (early precharge) ($\overline{CAS}$ latency = 2)	l_{EP}	—	–1	–1	—	–1	–1	
Column command to column command	l_{CCD}	1	1	1	1	1	1	
Write command to data in latency	l_{WCD}	0	0	0	0	0	0	
DQM to data in	l_{DID}	0	0	0	0	0	0	
DQM to data out	l_{DOD}	2	2	2	2	2	2	
CKE to CKE disable	l_{CLE}	1	1	1	1	1	1	

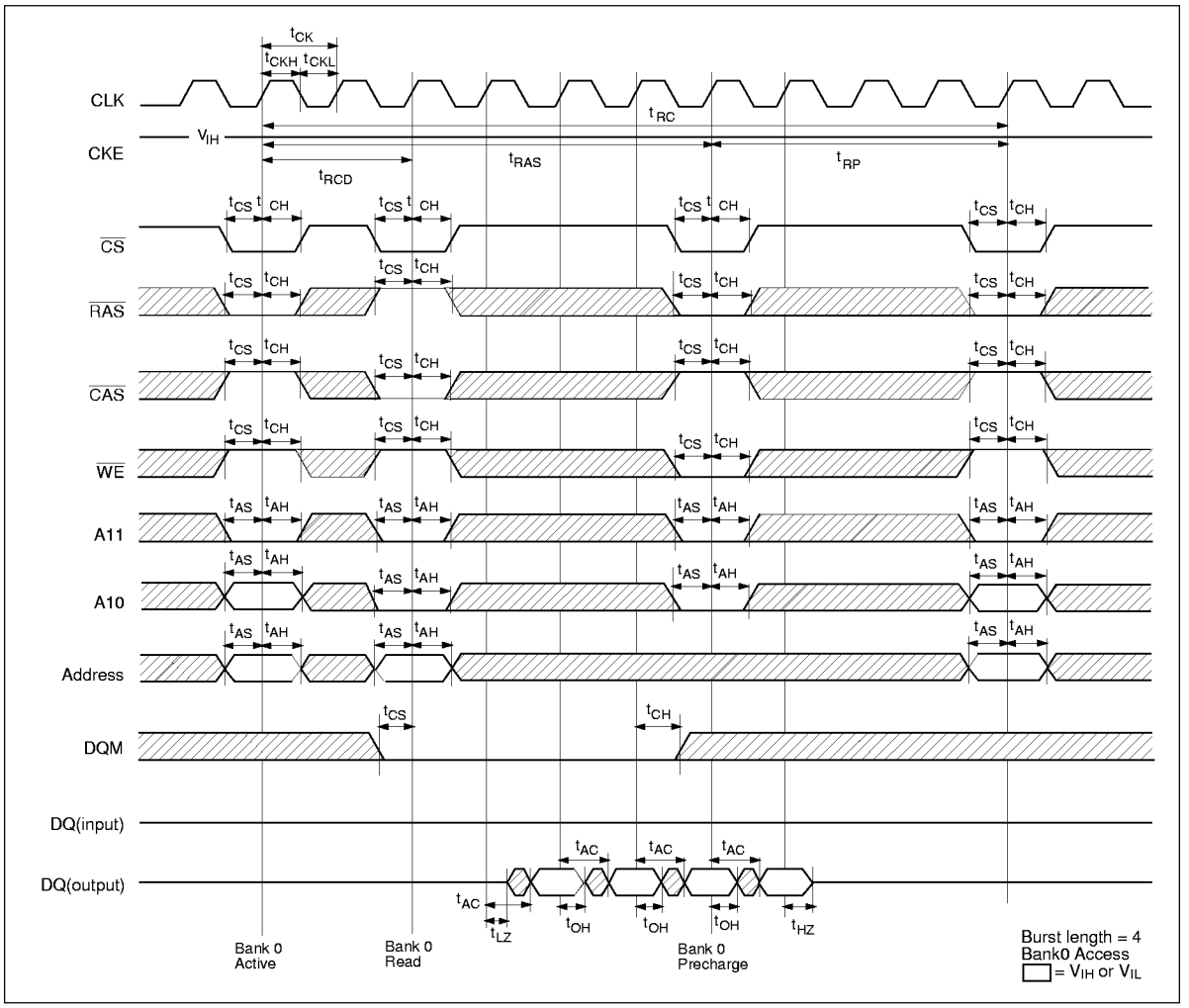
Relationship Between Frequency and Minimum Latency (cont)

Parameter		HB526A264EN						
		-10			-12			
Frequency (MHz)		**100**	**66**	**33**	**83**	**55**	**28**	
t_{CK} (ns)	**Symbol**	**10**	**15**	**30**	**12**	**18**	**36**	**Notes**
Register set to active command	t_{RSA}	1	1	1	1	1	1	
CS to command disable	t_{CDD}	0	0	0	0	0	0	
Power down exit to command input	t_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold ($\overline{CAS}$ latency = 3)	t_{BSR}	2	2	2	2	2	2	
Burst stop to output valid data hold ($\overline{CAS}$ latency = 2)	t_{BSR}	—	1	1	—	1	1	
Burst stop to output high impedance ($\overline{CAS}$ latency = 3)	t_{BSH}	3	3	3	3	3	3	
Burst stop to output high impedance ($\overline{CAS}$ latency = 2)	t_{BSH}	—	2	2	—	2	2	
Burst stop to write data ignore	t_{BSW}	0	0	0	0	0	0	

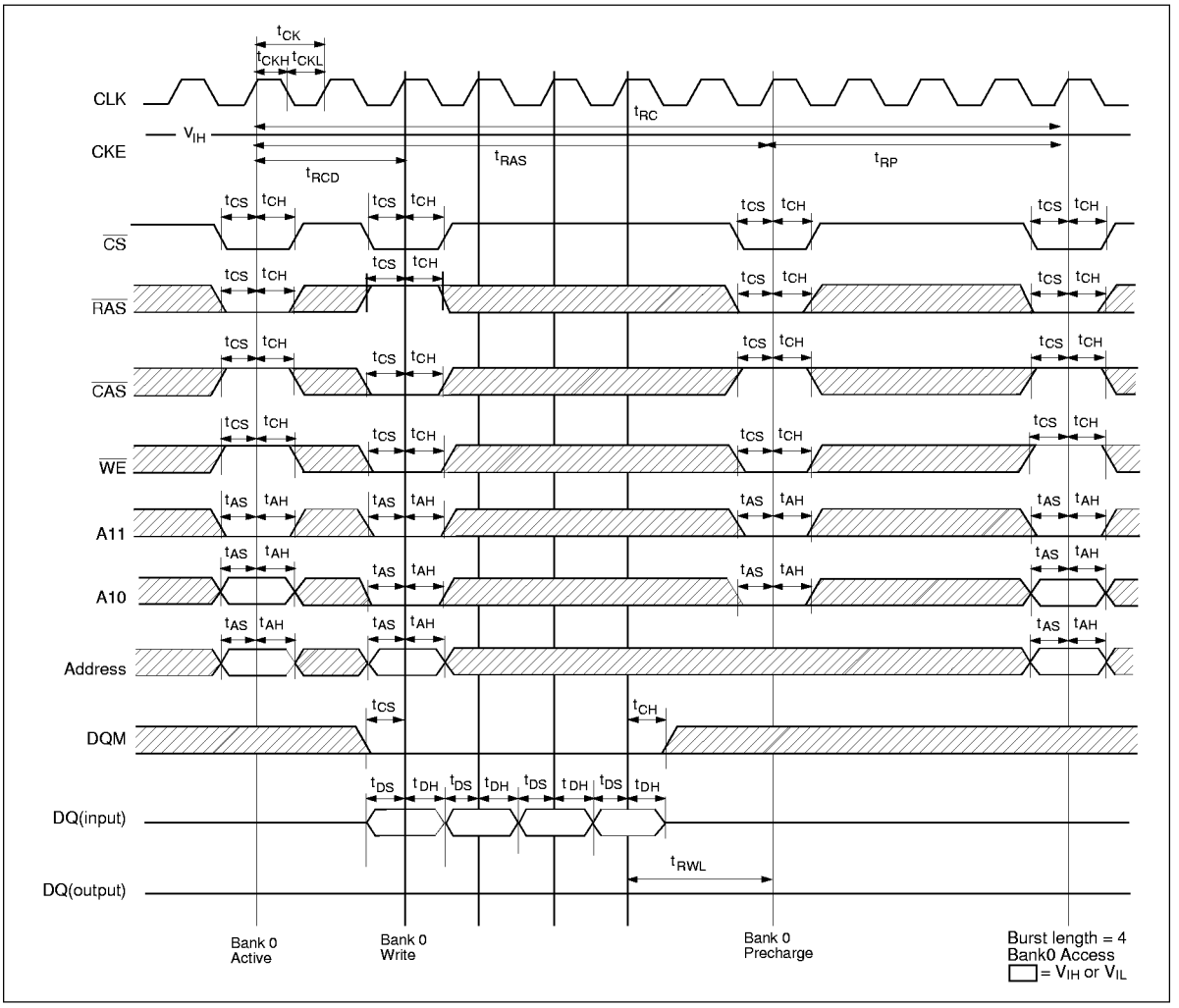
Notes: 1. t_{RCD} to t_{RRD} are recommended value.
2. CL = $\overline{CAS}$ latency.
3. 2Clock is requied between self refresh exit time and next refresh or active command.

Timing Waveforms

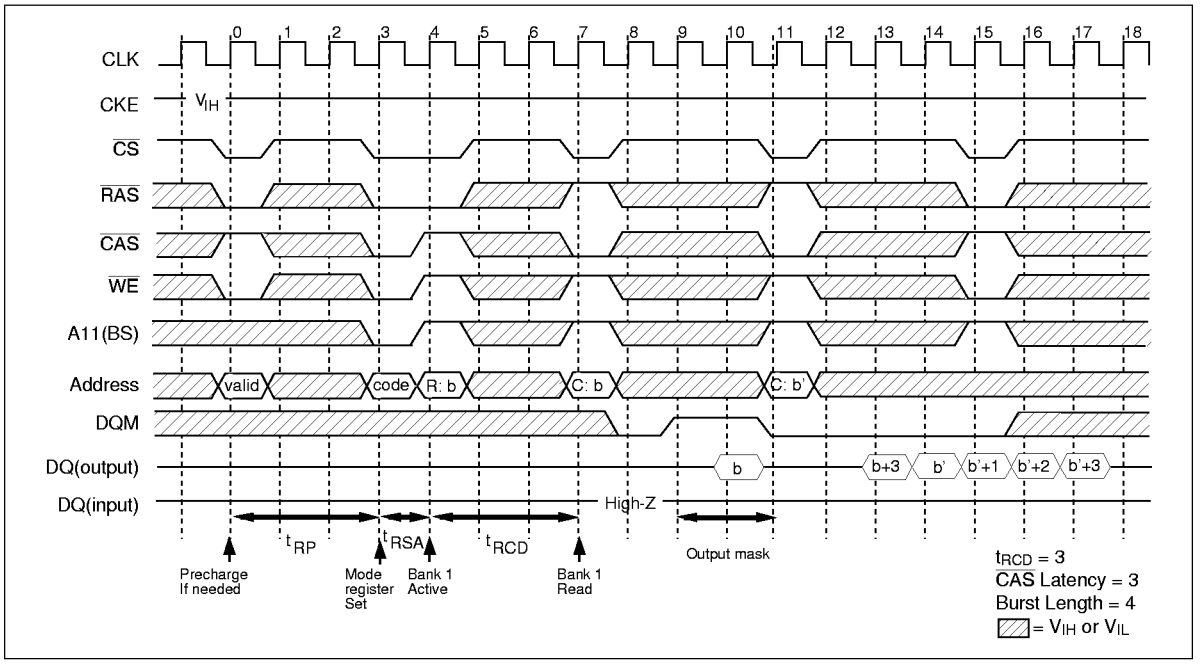
Read Cycle



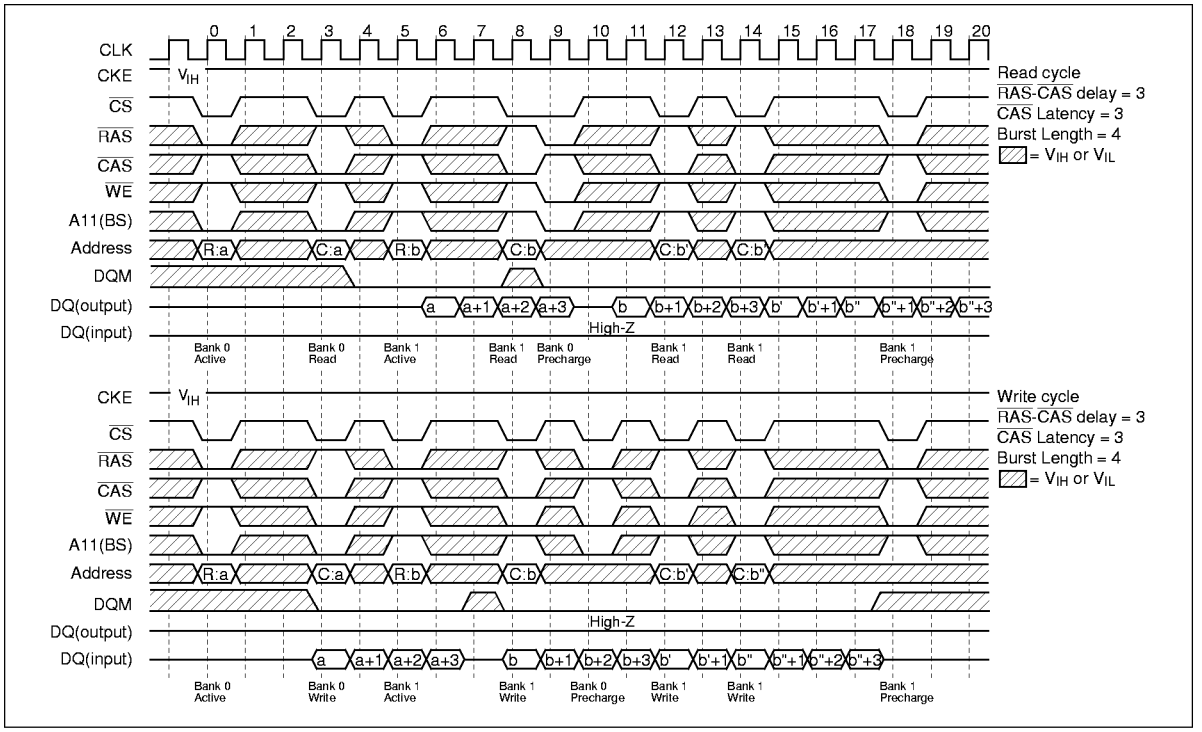
Write Cycle


tCK
tCKH tCKL
CLK
VIH
CKE
tRC
tRAS
tRP
tRCD
tCS tCH
CS
RAS
CAS
WE
tAS tAH
A11
A10
Address
DQM
tDS tDH
DQ(input)
tRWL
DQ(output)
Bank 0
Active
Bank 0
Write
Bank 0
Precharge
Burst length = 4
Bank0 Access
= VIH or VIL

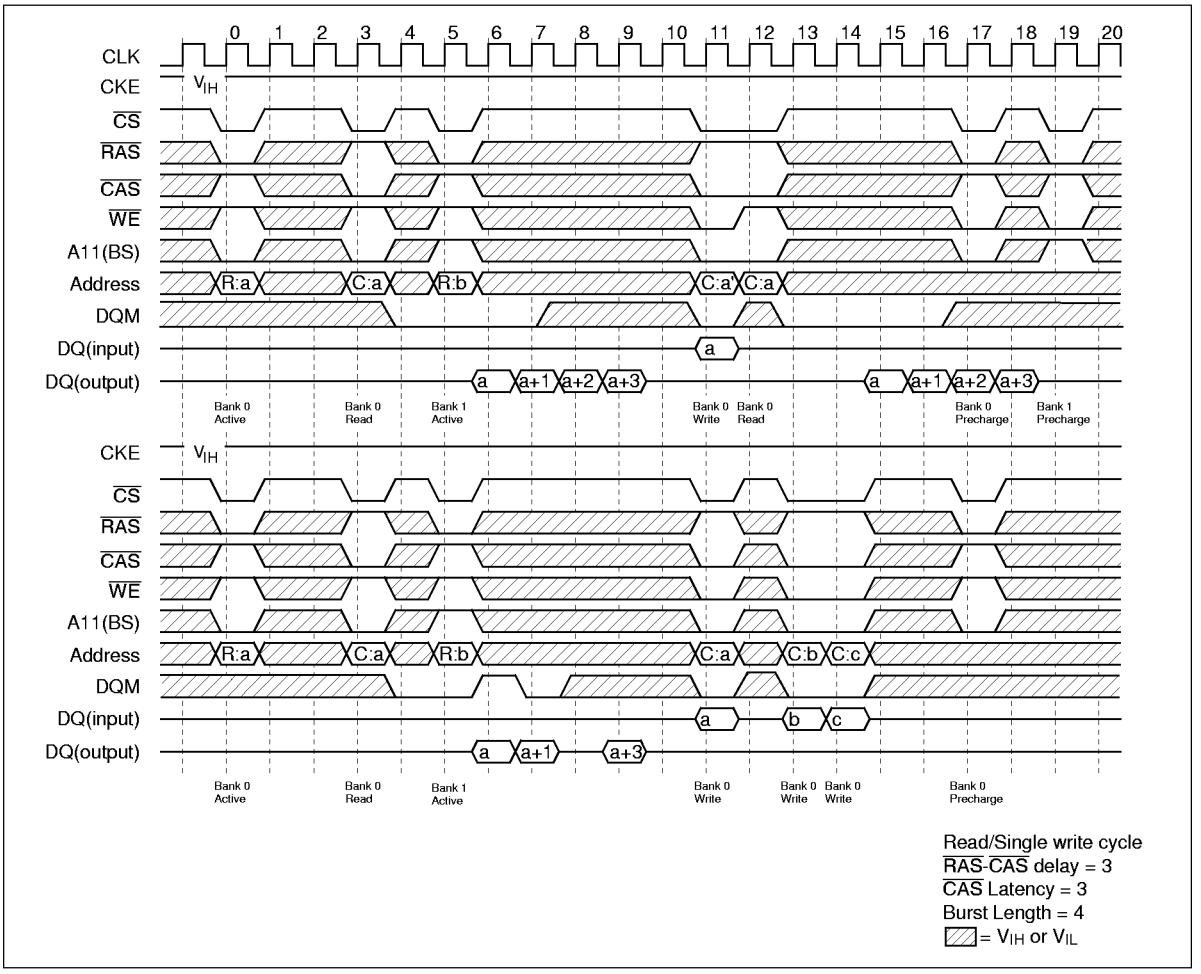
Mode Register Set Cycle



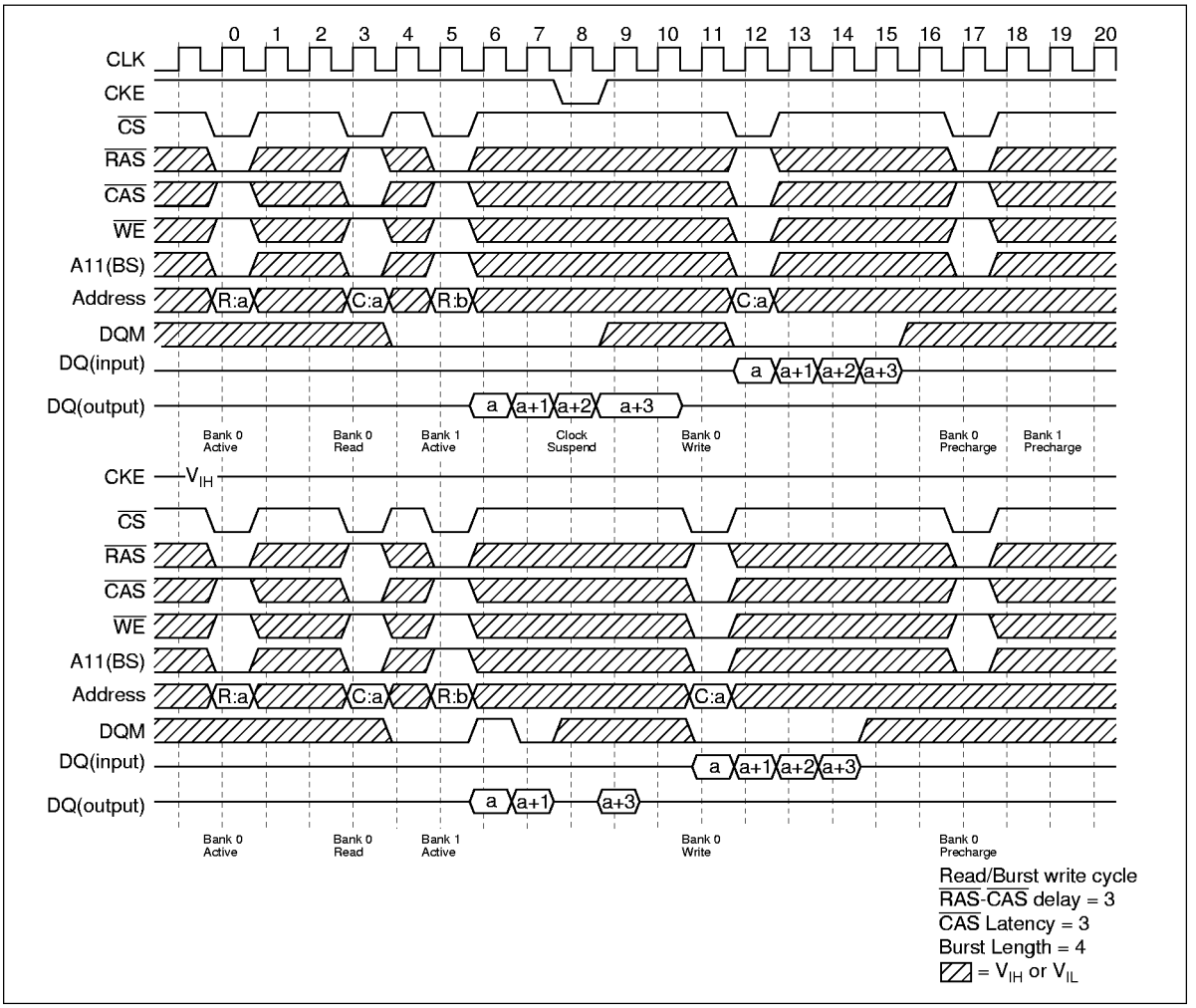
Read Cycle/Write Cycle



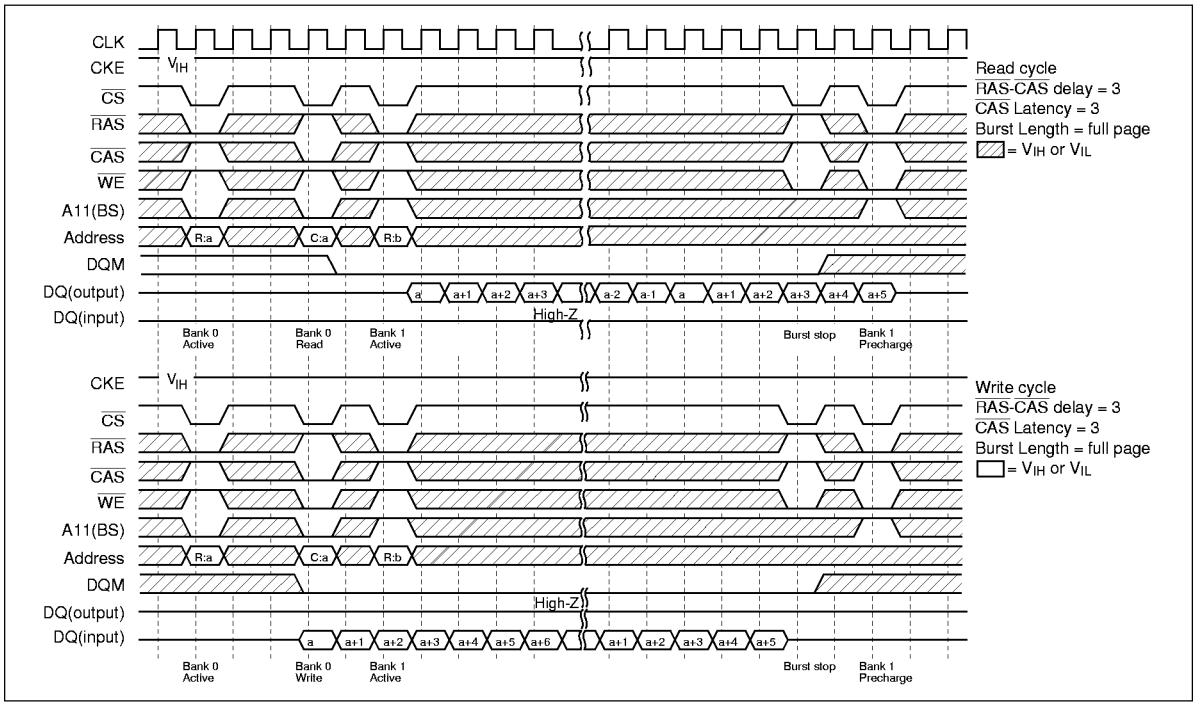
Read/Single Write Cycle



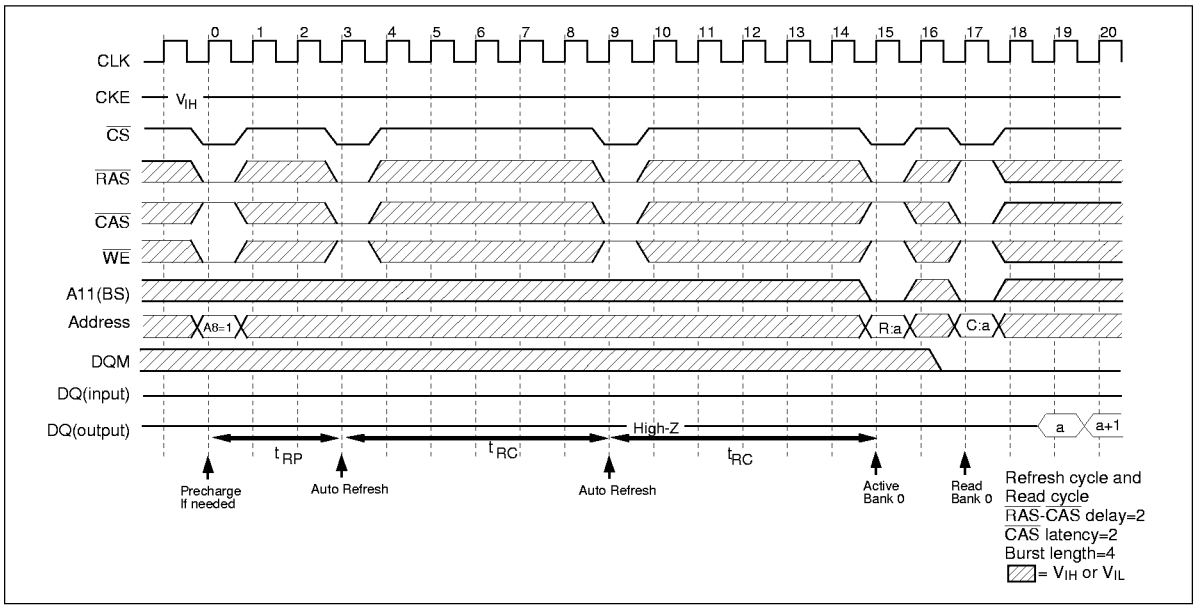
Read/Burst Write Cycle



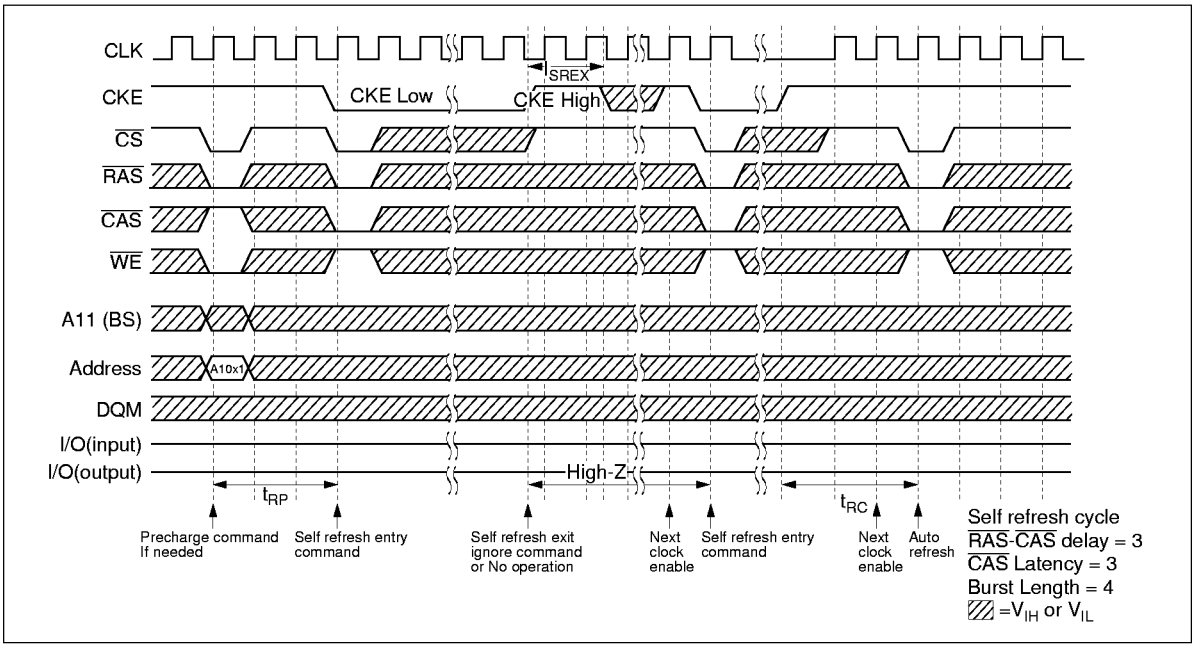
Full Page Read/Write Cycle



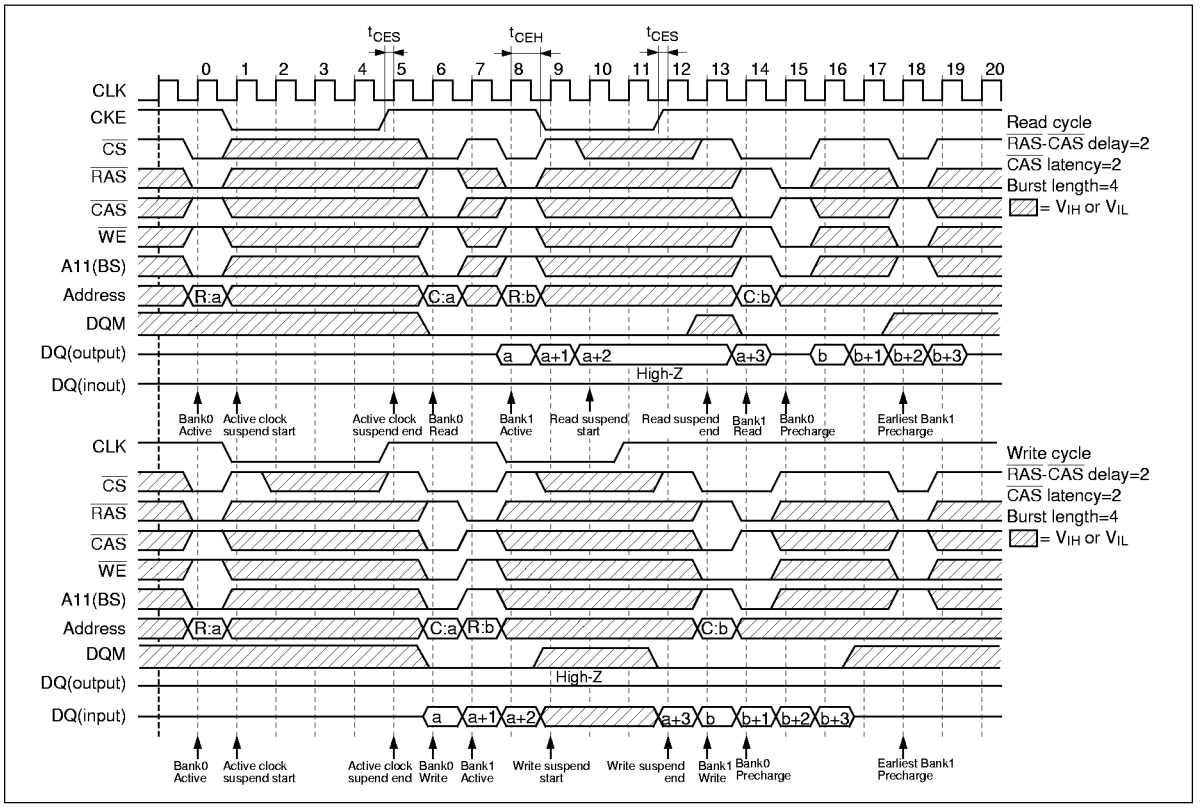
Auto Refresh Cycle



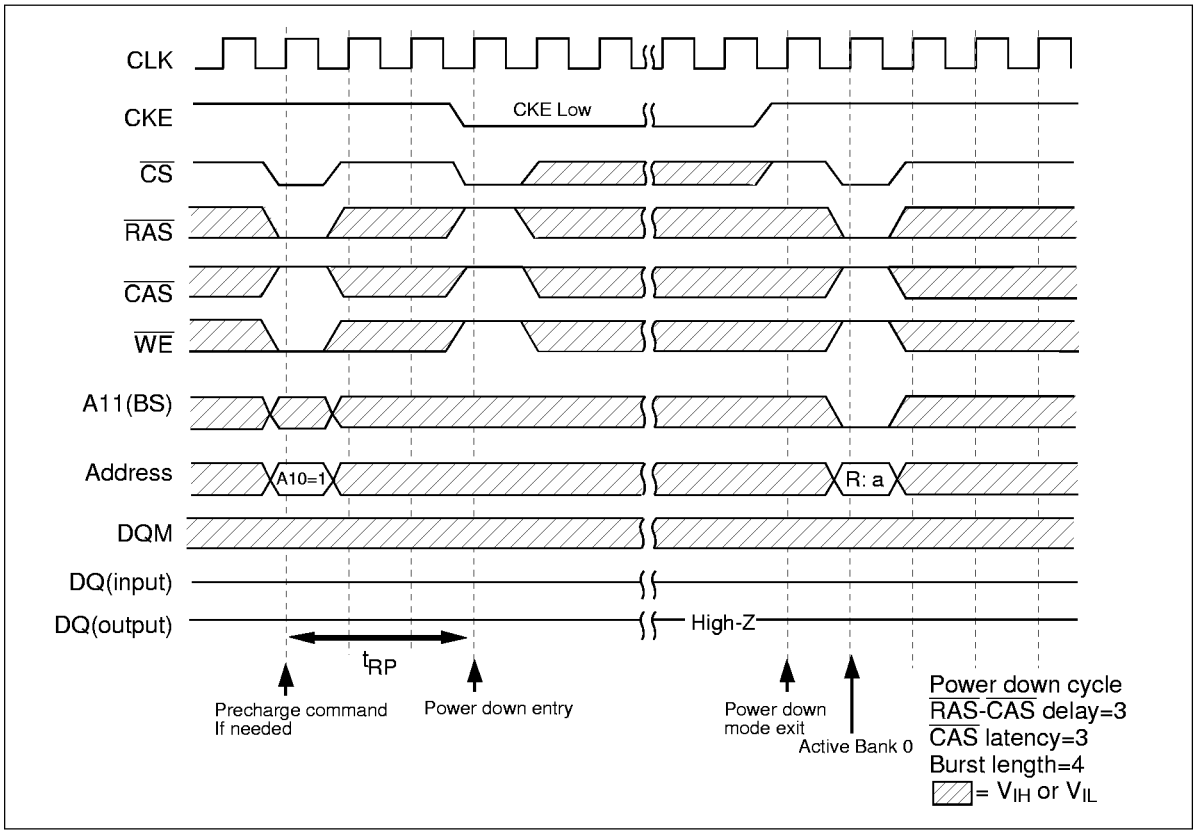
Self Refresh Cycle



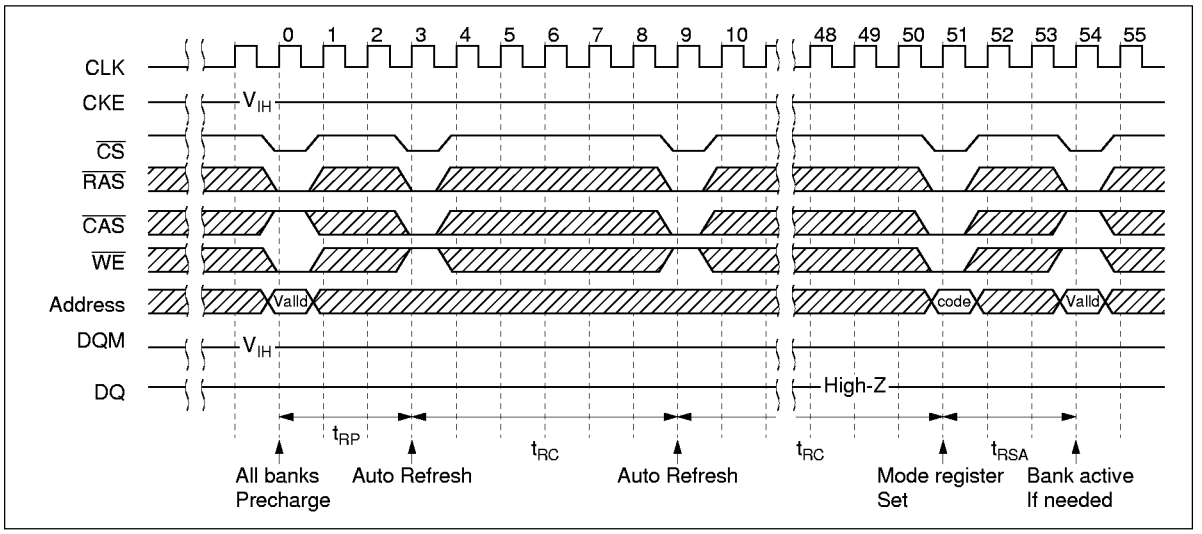
Clock Suspend Mode



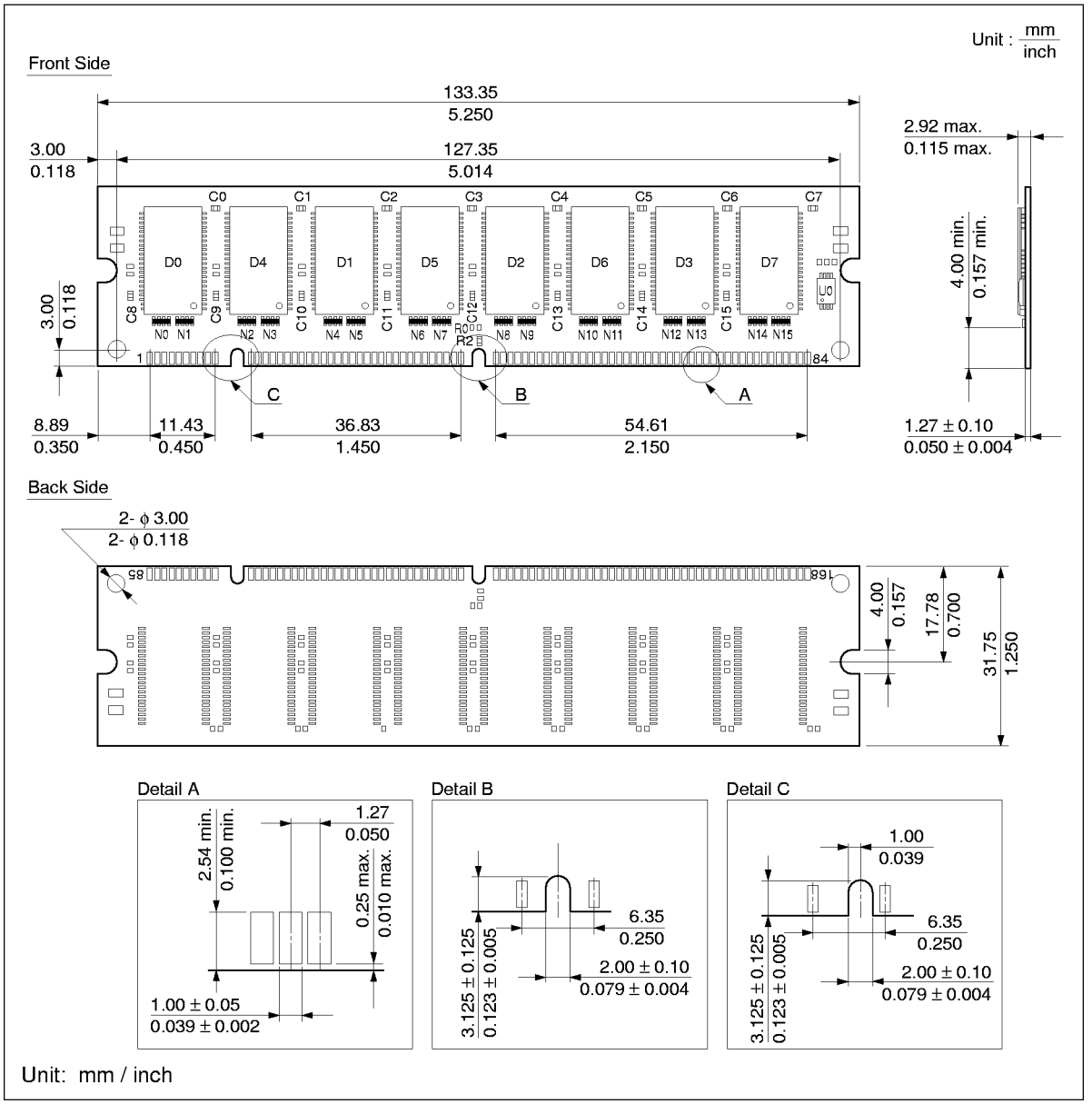
Power Down Mode



Power Up Sequence



Physical Outline



Unit: mm / inch