DATA SHEET

HC 3052/HC 3053
HC 3054/HC 3057

MONOLITHIC CMOS SERIAL INTERFACE COFIDEC FAMILY

FEATURES

COMPLETE CODEC/FILTER (COFIDEC) FAMILY
- **HC 3052 – μ-LAW WITH SHORT FRAME SIGNALING (18 PIN)**
- **HC 3053 – μ-LAW WITH BOTH SHORT AND LONG FRAME SIGNALING (20 PIN)**
- **HC 3054 – μ-LAW WITHOUT SIGNALING (16 PIN)**
- **HC 3057 – A-LAW (16 PIN)**
- **LOW OPERATION POWER (60 mW typical)**
- **LOW STANDBY POWER (1 mW typical)**
- **± 5 V POWER SUPPLIES**
- **MEETS OR EXCEED ALL D3/D4 AND CCITT SPECIFICATIONS**
- **TTL COMPATIBLE DIGITAL INTERFACES**
- **PCM DATA SERIAL INPUT/OUTPUT**
- **SYNCHRONOUS OR ASYNCHRONOUS OPERATION**

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DESCRIPTION

The MHS CODEC/FILTER (COFIDEC) family includes A-Law and μ-Law monolithic CODEC/FILTERS implemented with double-poly CMOS technology.

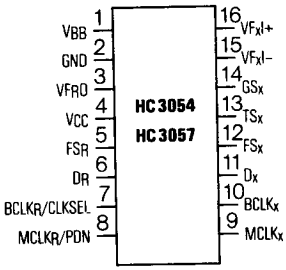
The transmit side of the device consists of:
– an amplifier with external gain adjustment
– an RC active prefilter to eliminate high frequency noise
– a switched capacitor band-pass filter including a notch filter at 55 Hz to reject signals below 200 Hz and above 3400 Hz
– a charge redistribution coder which samples and encodes filtered signal in the companded μ-Law or A-Law PCM format
– a precision voltage reference
– an internal auto-zero network to cancel the transmit offset.

The receive side of the device consists of:
– an expanding decoder (A-Law or μ-Law) to reconstruct the analog signal
– a switched-capacitor low-pass filter which corrects for the sinx/x response of the decoder output and rejects signals above 3400 Hz
– an RC active filter followed by a single ended power amplifier able to drive a 600 ohms load
– a precision voltage reference.

The PCM word is transmitted/received in a serial format compatible with industry standard.
The device is operated with two (transmit and receive) master clocks (1.536 MHz, 1.544 MHz or 2.048 MHz) which may be asynchronous.
Also required are transmit and receive bit clocks which may vary from 64 KHz to 2.048 MHz and transmit and receive frame sync pulses.

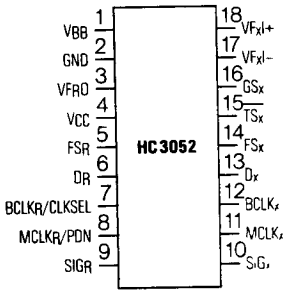
PINOUTS

Dual in-Line Package



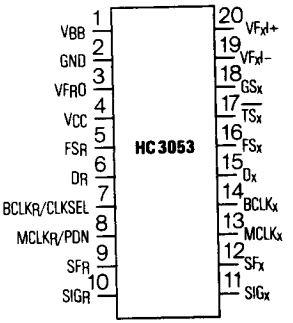
TOP VIEW

Dual in-Line Package



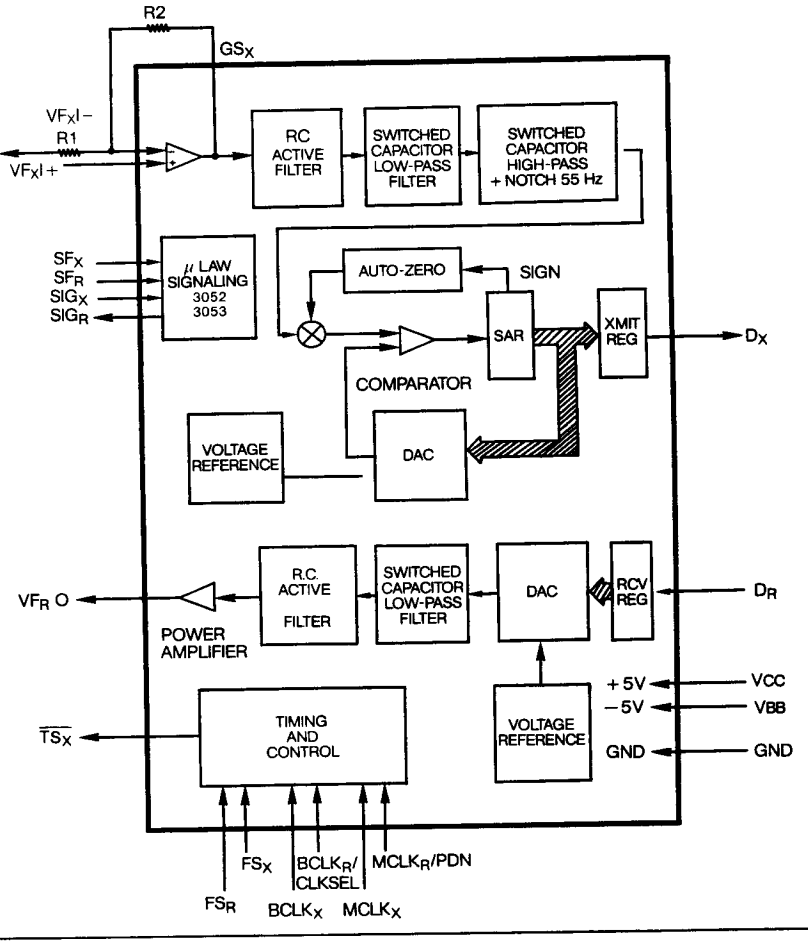
TOP VIEW

Dual in-Line Package



TOP VIEW

FUNCTIONAL DIAGRAM



PIN DESCRIPTION

HC 3052 PIN NO	HC 3053 PIN NO	HC 3054 HC 3057 PIN NO	NAME	FUNCTION
1	1	1	V_{BB}	Negative power supply $V_{BB} = -5$ V.
2	2	2	GND	Ground.
3	3	3	VFR_O	Analog output of the receive filter.
4	4	4	V_{CC}	Positive power supply $V_{CC} = +5$ V.
5	5	5	FS_R	Receive frame sync pulse.An 8 KHz pulse train which enables the PCM word to be shifted into the receive register.
6	6	6	D_R	Receive data input.The receive register clocks in D_R input with bit clock falling edge following an FS_R rising edge.
7	7	7	$BCLK_R$ & CLKSEL	Bit clock which shifts D_R input into the receive register. May vary from 64 KHz to 2.048 MHz. Alternatively may be a clock selection in synchronous mode. See table in functional description for synchronous operation.
8	8	8	$MCLK_R$ & PDN	Receive master clock must be 1.536 or 1.544 MHz. May be asynchronous with $MCLK_X$ and $BCLK_R$. If $MCLK_R$ is low, the COFIDEC operates in synchronous mode. If $MCLK_R$ is tied high, the COFIDEC is powered down.
	9		SF_R	When high during FS_R, SF_R indicates a receive signaling frame in long frame mode.
9	10		SIG_R	The signaling bit appears at this ouptut after each receive signaling frame.
10	11		SIG_X	Signaling data input.This input is inserted in place of LSB of PCM word during signaling frame.
	12		SF_X	When high during FS_X, SF_X indicates a transmit signaling frame in long frame mode.
11	13	9	$MCLK_X$	Transmit master clock. Must be 1.536, 1.544 or 2.048 MHz. May be asynchronous with $MCLK_R$. See table in functional description for synchronous operation.
12	14	10	$BCLK_X$	Bit clock. May vary from 64 KHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
13	15	11	D_X	Three-state PCM data output enabled by FS_X.
14	16	12	FS_X	Transmit frame sync pulse. An 8 KHz pulse train which enables the PCM word to be shifted out through D_X with $BCLK_X$.
15	17	13	$\overline{TS_X}$	Open drain output. Pulled down during time slot.
16	18	14	GS_X	Analog output of transmit amplifier used to set the gain.
17	19	15	VF_XI-	Inverting input of transmit amplifier.
18	20	16	VF_XI+	Non inverting input of transmit amplifier.

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FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COFIDEC and places it into a power-down state. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high ; the alternative is to hold both FS_X and FS_R inputs continuously low - the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The three state PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits.

A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.554 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. *Table 1* indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 KHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the three state D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running) : FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

ASYNCHRONOUS OPERATION

Two asynchronous modes are allowed with excellent transmission performance :

1) $MCLK_R$ is fully independent of $MCLK_X$ and must be 2.048 MH_Z for HC 3057 (A law) and 1.544 or 1.536 MH_Z for HC 3052/3053/3054 (μ law) (freq $MCLK_X$ = freq $MCLK_R \pm 50$ ppm).

2) If required, $MCLK_X$ can be used as a master clock for both transmit and receive sections by applying static logic levels to the $MCLK_R$/PDN pin.

In both modes, $BCLK_X$ and $BCLK_R$ may operate from 64 KH_Z to 2.048 MH_Z $BCLK_X$ must be synchronous with $MCLK_X$, but $BCLK_R$ may be asynchronous with $MCLK_R$ (freq $BCLK_R$ = freq $MCLK_R \pm 50$ ppm).

The degradation of the total signal to distortion ratio under all permitted asynchronous conditions does not exceed 0.5 dB as compared to the same measurement made with fully synchronous clocks.

Table 1 - Selection of Master Clock Frequencies

$BCLK_R$/ CLKSEL	Master Clock Frequency Selected	
	HC 3057	HC 3052 HC 3053 HC 3054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

SHORT FRAME SYNC OPERATION

The COFIDEC can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X, and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X three state output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_X, the COFIDEC will sense whether short or long frame sync pulses are being used. For 64 KHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X three state output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

SIGNALING

The HC 3052 and HC 3053 μ-law COFIDECs contain circuitry to insert and extract signaling information in the PCM data stream. The HC 3052 is intended for short frame sync applications, and the HC 3053 for long frame sync applications, although the HC 3053 may also be used in short frame sync applications. The HC 3054 and HC 3057 have no provision for signaling. Signaling for the HC 3052 is accomplished by applying a frame sync pulse two bit clock periods long, as shown in *Figure 2*. With FS_X two bit clock periods long, the data present at SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With FS_R two bit clock periods long, the LSB of the PCM data read into the D_R input will be latched and appear on the SIG_R output pin until updated following the next signaling frame. The decoder will then interpret the lost LSB as "1/2" to minimize noise and distortion. This short frame signaling may also be implemented using the HC 3053, providing SF_R and SF_X are left open circuit or tied low. The HC 3052 is not capable of inserting or extracting signaling information in the long frame mode.

Signaling for the HC 3053 may be accomplished in either short or long frame sync mode. The short mode signaling is the same as the HC 3052. For long frame signaling, two additional frame sync pulses are required, SF_X and SF_R, which indicate transmit and receive signaling frames, respectively. With an SF_X signaling frame sync, the data present at the SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With an SF_R signaling frame sync, the LSB of the PCM data at D_R will be latched and appear on the SIG_R output pin until the next signaling frame. The decoder will also do the "1/2" step interpretation to compensate for the loss of the LSB.

TRANSMIT SECTION

The input of the transmit section is an operational amplifier whose gain can be externally adjusted. This amplifier exhibits low noise, wide bandwith and low offset voltage (1mV typical). The input amplifier drives an antialiasing RC active filter. The switched capacitor bandpass filter is split into a 5 th order elliptic low-pass filter and a 3rd order elliptic high-pass filter which includes a 55 H_Z notch filter to guarantee excellent line (50 or 60 H_Z) rejection. The structure of each filter is fully differential so that their performance is not affected by parasitic elements. The A/D converter is of a companding type according to A (HC 3057) or μ (HC 3052/3053/3054) coding laws.

RECEIVE SECTION

The receive section includes an expanding D/A converter according to A (HC 3057) or μ (HC 3052/3053/3054) coding laws. The decoder is followed by a 5 th order switched capacitor low-pass filter and an RC active filter.

As for the transmit part, the filters are fully differential. The output amplifier has a unity gain and can drive a 600 Ω/500 pF load.

Separately trimmed voltage references are provided for transmit and receive sections respectively. Clocking circuits and internal power supplies are also fully independent. This arrangement greatly reduces crosstalk between the transmit and receive blocks and improves performance.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND −0.3V to 7V
V_{BB} to GND +0.3V to −7V
Voltage at any Digital Input or Output
V_{CC} + 0.3V to GND − 0.3V
Voltage at any Analog Input or Output
V_{CC} + 0.3V to V_{BB} − 0.3V

Operating Temperature Range −25 °C to 80 °C
Storage Temperature Range −65 °C to 150 °C
Lead Temperature (Soldering 10 seconds) 300 °C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: V_{CC} = 5.0V ± 5% V_{BB} = 5V ± 5% GND = OV
T_A = 0 °C to 70 °C: typical characteristics specified at V_{CC} = 5.0V, V_{BB} = −5.0V. T_A = 25 °C: all signals are referenced to GND

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	DX, I_L = 5.0mA $SIGR$, I_L = 1.0mA $\overline{TSX}$, I_L = 3.2mA. Open Drain			0,4 0.4 0.4	V V V
V_{OH}	Output High Voltage	DX, I_L = −5.0mA $SIGR$, I_L = −1.0mA	2.4 2,4			V V
I_{IL}	Input Low Current (Note 1)	GND ≤ V_{IN} ≤ V_{IL}. All Digital Inputs	−10		10	µA
I_{IH}	Input High Current (Note 1)	V_{IH} ≤ V_{IN} ≤ V_{CC}	−10		10	µA
I_{OZ}	Output Current in High Impedance State	DX, GND ≤ V_O ≤ V_{CC}	−10		10	µA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_{IXA}	Input Leakage Current	−2.5V ≤ V ≤ +2.5V, $VFXI+$ or $VFXI-$	−200		200	nA
R_{IXA}	Input Resistance	−2.5V ≤ V ≤ +2.5V, $VFXI+$ or $VFXI-$	10			MΩ
R_{OXA}	Output Resistance	Closed Loop. Unity Gain		1	3	Ω
R_{LXA}	Load Resistance	GSX	10			kΩ
C_{LXA}	Load Capacitance	GSX			50	pF
V_{OXA}	Output Level	GSX RL = 10k Ω	±2.8	±4.2		V
A_{VXA}	Voltage Gain	$VFXI+$ to GSX	5000			VV
F_{UXA}	Unity Gain Bandwidth		1	2		MHz
V_{OSXA}	Offset Voltage		−20	1	20	mV
V_{CMXA}	Common-Mode Voltage		−2.5		+2.5	V
CMRRXA	Common-Mode-Rejection Ratio		60	80		dB
PSRRXA	Power Supply Rejection Ratio		60	70		dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_{ORF}	Output Resistance	Pin $VFRO$		1	3	Ω
R_{LRF}	Load Resistance	$VFRO$ = ± 2.5V	600			Ω
C_{LRF}	Load Capacitance				500	pF
VOS_{RO}	Output DC Offset Voltage		−100		100	mV
POWER DISSIPATION (ALL DEVICES)						
I_{CCO}	Power-Down Current			0.15	0.5	mA
I_{BBO}	Power-Down Current			0.05	0.3	mA
I_{CC1}	Active Current			6	9	mA
I_{BB1}	Active Current			6	9	mA

Note 1: SF_X, SF_R: Internal pull down (2µ A typical) - $BCLK_R$: Internal pull up (2µ A typical)

TRANSMISSION CHARACTERISTICS (ALL DEVICES)

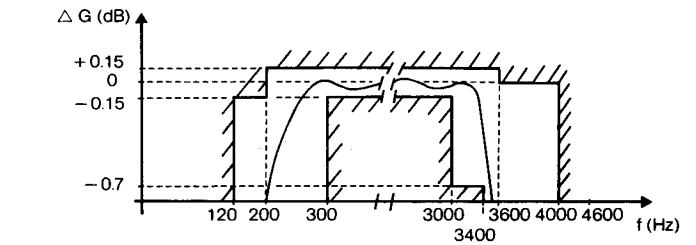
Unless otherwise specified: $T_A = 0$ °C to 70 °C, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm -5\%$, GND = OV, f = 1.02 kHz, $V_{IN.}$ = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

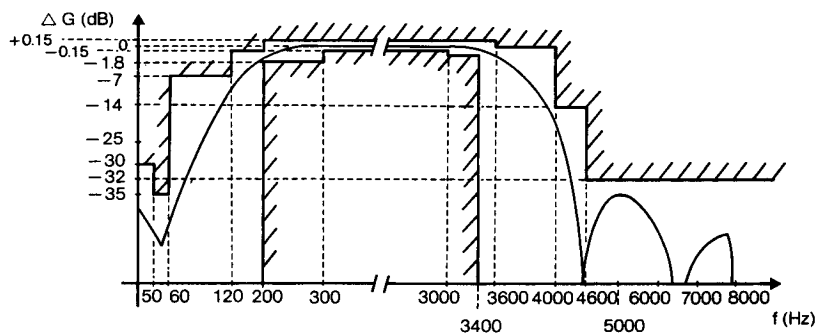
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AMPLITUDE RESPONSE						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600Ω). 0 dBm0 (all devices)		1.2277		Vrms
	Max Overload Levels	HC 3052, HC 3053, HC 3054 (3.17 dBm0) HC 3057 (3.14 dBm0)		2.501 2.492		V_{DC} V_{DC}
G_{XA}	Transmit Gain, Absolute	$T_A = 25$ °C, $V_{CC} = 5V$, $V_{BB} = -5V$ Input at GS_X = OdBm0 at 1020 Hz	−0.15		0.15	dB
G_{XATV}	Absolute Transmit Gain Variation with Temperature and Supply Voltage	$T_A = 0$ °C to 70 °C $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm -5\%$			± 0.15	dB
G_{XRL}	Transmit Gain Variations with level	Sinusoidal Test Method Reference Level 10 dBm0 VF_XI + 40 dBm0 to + 3 dBm0 VF_XI + 50 dBm0 to 40 dBm0 VF_XI + 55 dBm0 to 50 dBm0	 0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
G_{RA}	Receive Gain, Absolute	$T_A = 25$ °C, $V_{CC} = 5V$, $V_{BB} = -5V$ Input = Digital Code Sequence for OdBm0 Signal at 1020Hz	−0.15		0.15	dB
G_{RATV}	Absolue receive Gain Variation with Temperature and Supply Voltage	$T_A = 0$ °C to 70 °C $V_{CC} = 5V \pm 5\%$ $V_{BB} \pm 5V \pm 5\%$			± 0.15	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method : Reference Input PCM Code Corresponds to an ideally Encoded - 10 dBm0 Signal PCM Level = −.40 dBm0 to + 3 dBm0 PCM Level = − 50 dBm0 to − 40 dBm0 PCM Level = − 55 dBm0 to = 50 dBm0	 −0.2 −0.4 −1.2		 +0.2 +0.4 +1.2	 dB dB dB
V_{RO}	Receive Output Drive Level	$R_L = 600\ \Omega$	2.5		2.5	V
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz − 600 Hz f = 600 Hz − 800 Hz f = 800 Hz − 1000 Hz f = 1000 Hz − 1600 Hz f = 1600 Hz − 2600 Hz f = 2600 Hz − 2800 Hz f = 2800 Hz − 3000 Hz		140 100 50 20 60 80 140	220 145 75 50 100 110 200	µs µs µs µs µs µs µs
D_{RA}	Receive Delay, Absolute	f = 750 Hz		160	180	µs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz − 1600 Hz f = 1600 Hz − 2600 Hz f = 2600 Hz − 2800 Hz f = 2800 Hz − 3000 Hz		40 90 120 140	60 120 140 175	µs µs µs µs

TRANSMISSION CHARACTERISTICS (continued)

Unless otherwise specified: T_A=0 °C to 70 °C, V_{CC}=5V ± 5 %, V_{BB}=−5V ± 5 %, GND=0V, f=1.02 kHz, V_{IN}=0 dBm0, transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT SECTION TRANSFER CHARACTERISTICS						
G_{XR}	Transmit Gain Relative to Gain at 820 Hz (0dBm0)	f= 50 Hz - 60 Hz			−35	dB
		f= 60 Hz - 120 Hz			−7	dB
		f= 120 Hz - 200 Hz			−0.15	dB
		f= 200 Hz - 300 Hz	−1.8		+0.15	dB
		f= 300 Hz - 3000 Hz	−0.15		+0.15	dB
		f=3000 Hz - 3400 Hz	−0.7		+0.15	dB
		f=3400 Hz - 3600 Hz			+0.15	dB
		f=3600 Hz - 4000 Hz			0	dB
		f=4000 Hz - 4600 Hz			−14	dB
		f=4600 Hz and Up			−32	dB

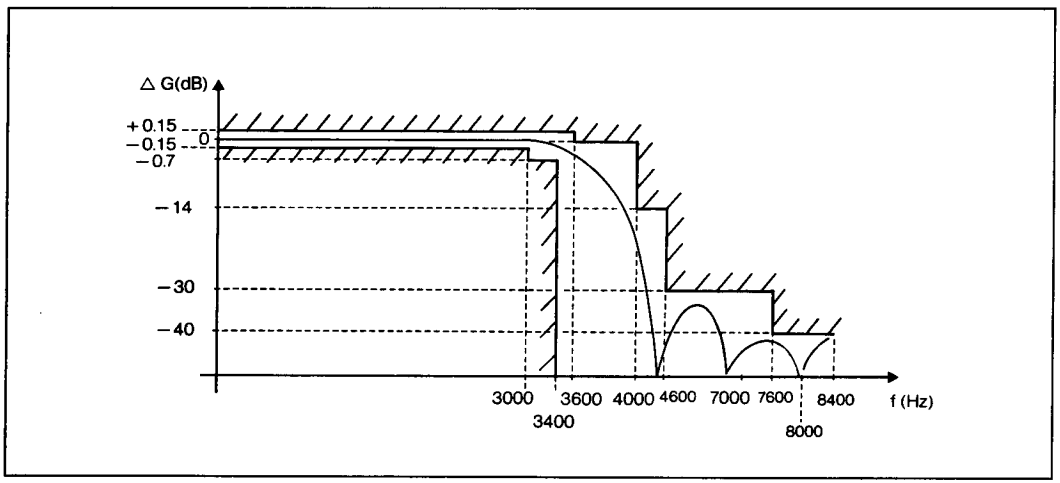




TRANSMISSION CHARACTERISTICS (continued)

Unless otherwise specified : T_A=0°C to 70°C, V_{CC}=5V±5%, V_{BB}=−5V±5%, GND=0V, f=1.02 kHz, V_{IN}=0 dBm0, transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVE SECTION TRANSFER CHARACTERISTICS						
G_{RR}	Receive Gain Relative to Gain at 820 Hz (0dBm0)	f= 0 Hz - 3000 Hz f=3000 Hz - 3400 Hz f=3400 Hz - 3600 Hz f=3600 Hz - 4000 Hz f=4000 Hz - 4600 Hz	−0.15 −0.7		+0.15 +0.15 +0.15 0 −14	dB dB dB dB dB
SOS	Spurious Out-of-Band Signals at the channel Output	Image Signals at VF_{RO}: f=4600 Hz to 7600 Hz f=7600 Hz to 8400 Hz			 −30 −40	dB dB dB



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TRANSMISSION CHARACTERISTICS (continued)

Unless otherwise specified : $T_A = 0$ °C to 70 °C, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GND = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
NOISE						
N_{XC}	Transmit Idle Channel Noise, C Message Weighted	HC 3052, HC 3053, HC 3054 $VF_XI^- = OV$		12	15	dBmC0
N_{XP}	Transmit Noise, P Message Weighted	HC 3057 Note 1 $VF_XI^- = OV$ Note 2		−74 −70	−69 −67	dBm0p dBm0p
N_{RC}	Receive Idle Channel Noise C Message Weighted	HC 3052, HC 3053, HC 3054 PCM Code equals alternating Positive and Negative Zero		8	11	dBrnC0
N_{RP}	Receive Idle Channel Noise P Message Weighted	HC 3057 PCM Code equals Positive Zero		−82	−79	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 KHz to 100 KHz, Loop Around Measurement, $VF_XI^- = 0$ Vrms			−53	dBm0
POWER SUPPLY REJECTION						
$PPSR_X$	Positive Power Supply Rejection Transmit	$VF_XI^- = 0$ Vrms $V_{CC} = 5.0\ V_{DC} + 100$ mVrms f = 0 − 50 KHz	40			dBC
$NPSR_X$	Negative Power Supply Rejection Transmit	$VF_XI^+ = 0$ Vrms $V_{BB} = -5.0\ V_{DC} + 100$ mVrms f = 0 − 50 KHz	40			dBC
$PPSR_R$	Positive Power Supply Rejection Receive	PCM Code equals Positive Zero $V_{CC} = 5.0\ V_{DC} + 100$ mVrms f = 0.4000 Hz f = 0 − 50 KHz	40 25			dBC dB
$NPSR_R$	Negative Power Supply Rejection Receive	PCM Code equals Positive Zero $V_{BB} = -5.0\ V_{DC} + 100$ mVrms f = 0 − 4000 Hz f = 0 − 50 KHz	40 25			dBC dB
DISTORTION						
$STD_{X/R}$	Signal to Total Distortion Transmit or Receive Channel	Sinusoidal Test Method Level = 3.0 dBm0 = 0dBm0 to − 30 dBM0 = − 40 dBm0 XMT RCV = − 55 dBm0 XMT RCV	33 36 29 30 14 15			dBC dBC dbc dBC dBC dBC
SFD_X	Single Frequency Distortion Transmit				−46	dB
SFD_R	Single Frequency Distortion Receive				−46	dB
IMD	Intermodulation Distortion	Loop Around Measurement. $VF_XI^- = -4$ dBm0 to − 21 dBm0, two frequencies in the range 300 Hz to 3 400 Hz			−41	dB
CROSSTALK						
CT_X-R	Transmit to Receive Crosstalk 0dBm0 Transmit Level	f = 300 Hz − 3 400 Hz D_R = Steady PCM Code		−90	−75	dB
CT_R-X	Receive to Transmit Crosstalk odBm0 Receive Level	f = 300 Hz − 3 400 Hz $VF_XI^- = OV$		−90	−70	dB

Note 1 : Quantization Noise, measured by extrapolation from the distortion result.
Note 2 : Idle Channel Noise, due to alternating sign bit of a perfectly zeroed encoder.

TIMING SPECIFICATIONS
Unless otherwise specified $T_A = 0$ °C to 70 °C, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GND = 0V

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1/t_{PM}	Frequency of Master Clocks	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	160			ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X	100			ns
t_{WBH}	Width of Bit Clock High	$V_{IH} = 2.2V$	160			ns
t_{WBL}	Width of Bit Clock Low	$V_{IL} = 0.6V$	160			ns
t_{HBF}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
t_{SBF}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t_{DBD}	Delay Time from $\overline{BCLK_X}$ High to Data Valid	Load = 150 pF plus 2 LSTTL loads	0		140	ns
t_{XDP}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL loads			140	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled	$C_L = 0$ pF to 150 pF	50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes later	$C_L = 0$ pF to 150 pF	20		165	ns
t_{SSFF}	Set-Up Time from $SF_{X/R}$ High to $FS_{X/R}$	HC 3053 Only	60			ns
t_{SSFB}	Set-Up Time from Signal Frame Sync High to $BCLK_{X/R}$ Clock	HC 3053 Only	60			ns
t_{SSGB}	Set-Up Time from SIG_X to $BCLK_X$	HC 3052 and HC 3053	100			ns
t_{HBSG}	Hold Time from $BCLK_X$ High to SIG_X	HC 3052 and HC 3053	50			ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		50			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		50			ns
t_{HBSF}	Hold Time from $BCLK_{X/R}$ Low to Signaling Frame Sync	HC 3053 Only	100			ns
t_{SF}	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	50			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	Short frame Sync Pulse (1 Bit Clock Period Long)	100			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Fram Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64K Bit/s Operating Mode	160			ns

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND −0.3V to 7V
V_{BB} to GND +0.3V to −7V
Voltage at any Digital Input or Output
V_{CC} + 0.3V to GND − 0.3V
Voltage at any Analog Input or Output
V_{CC} + 0.3V to V_{RR} − 0.3V

Operating Temperature Range −40 °C to 85 °C
Storage Temperature Range −65 °C to 150 °C
Lead Temperature (Soldering 10 seconds) 300 °C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: V_{CC} = 5.0V ± 5% V_{BB} = 5V ± 5% GND = OV
T_A = −40 °C to 85 °C: typical characteristics specified at V_{CC} = 5.0V, V_{BB} = −5.0V. T_A = 25 °C: all signals are referenced to GND

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	DX, I_L = 5.0mA $\overline{SIGR}$, I_L = 1.0mA $\overline{TSX}$, I_L = 3.2mA. Open Drain			0,4 0.4 0.4	V V V
V_{OH}	Output High Voltage	DX, I_L = −5.0mA SIG_R, I_L = −1.0mA	2.4 2,4			V V
I_{IL}	Input Low Current (Note 1)	GND ≤ V_{IN} ≤ V_{IL}. All Digital Inputs	−10		10	µA
I_{IH}	Input High Current (Note 1)	V_{IH} ≤ V_{IN} ≤ V_{CC}	−10		10	µA
I_{OZ}	Output Current in High Impedance State	DX, GND ≤ V_O ≤ V_{CC}	−10		10	µA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
$I_{I}XA$.	Input Leakage Current	−2.5V ≤ V ≤ +2.5V, VFXI+ or VFXI−	−200		200	nA
$R_I XA$	Input Resistance	−2.5V ≤ V ≤ +2.5V, VFXI+ or VFXI−	10			MΩ
$R_O XA$	Output Resistance	Closed Loop. Unity Gain		1	3	Ω
$R_L XA$	Load Resistance	GSX	10			kΩ
$C_L XA$	Load Capacitance	GSX			50	pF
$V_O XA$	Output Level	GSXRL = 10k Ω	±2.8	±4.2		V
$A_V XA$	Voltage Gain	VFXI+ to GSX	5000			VV
$F_U XA$	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		−20	1	20	mV
$V_{CM}XA$	Common-Mode Voltage		−2.5		+2.5	V
CMRRXA	Common-Mode-Rejection Ratio		60	80		dB
PSRRXA	Power Supply Rejection Ratio		60	70		dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
$R_O RF$	Output Resistance	Pin VF_RO		1	3	Ω
$R_L RF$	Load Resistance	VF_RO = ± 2.5V	600			Ω
$C_L RF$	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		−100		100	mV
POWER DISSIPATION (ALL DEVICES)						
I_{CCO}	Power-Down Current			0.15	0.5	mA
I_{BBO}	Power-Down Current			0.05	0.3	mA
I_{CC1}	Active Current			6	9	mA
I_{BB1}	Active Current			6	9	mA

Note 1: SF_X, SF_R: Internal pull down (2µ A typical) - $BCLK_R$: Internal pull up (2µ A typical)

TRANSMISSION CHARACTERISTICS (ALL DEVICES)

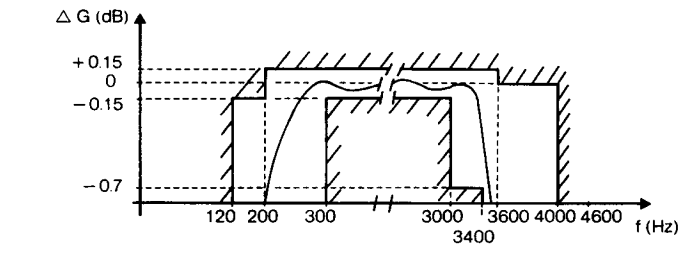
Unless otherwise specified: T_A = −40 °C to 85 °C, V_{CC} = 5V ± 5%, V_{BB} = −5V ± −5%, GND = OV, f = 1.02 kHz, $V_{IN.}$ = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

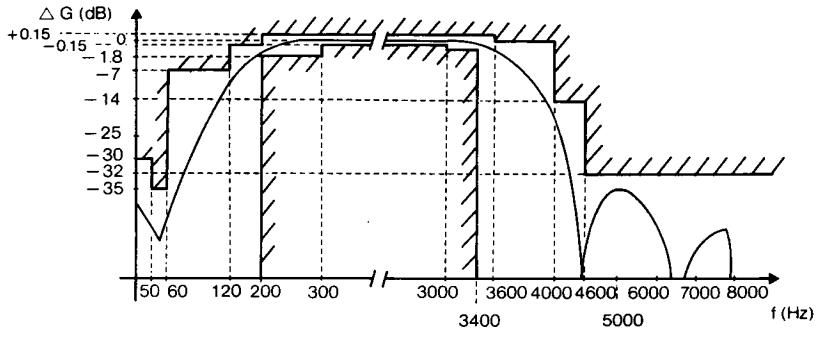
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AMPLITUDE RESPONSE						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600Ω). 0 dBm0 (all devices)		1.2277		Vrms
	Max Overload Levels	HC 5552, HC 5553, HC 5554 (3.17 dBm0) HC 5557 (3.14 dBm0)		2.501 2.492		V_{DC} V_{DC}
G_{XA}	Transmit Gain, Absolute	T_A = 25 °C, V_{CC} = 5V, V_{BB} = −5V Input at GS_X = OdBm0 at 1020 Hz	−0.15		0.15	dB
G_{XATV}	Absolute Transmit Gain Variation with Temperature and Supply Voltage	T_A = −40 °C to +85 °C V_{CC} = 5V ± 5%, V_{BB} = −5V ± −5%			± 0.15	dB
G_{XRL}	Transmit Gain Variations with level	Sinusoidal Test Method Reference Level 10 dBm0 VFXI + = −40 dBm0 to +3 dBm0 VFXI + = −50 dBm0 to 40 dBm0 VFXI + = −55 dBm0 to 50 dBm0	 0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
G_{RA}	Receive Gain, Absolute	T_A = 25 °C, V_{CC} = 5V, V_{BB} = −5V Input = Digital Code Sequence for OdBm0 Signal at 1020Hz	−0.15		0.15	dB
G_{RATV}	Absolue receive Gain Variation with Temperature and Supply Voltage	T_A = −40 °C to +85 °C V_{CC} = 5V ± 5% V_{BB} ± 5V ± 5%			± 0.15	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method : Reference Input PCM Code Corresponds to an ideally Encoded - 10 dBm0 Signal PCM Level = −40 dBm0 to +3 dBm0 PCM Level = −50 dBm0 to −40 dBm0 PCM Level = −55 dBm0 to = 50 dBm0	 0.2 −0.4 −1.2		 0.2 +0.4 +1.2	 dB dB dB
V_{RO}	Receive Output Drive Level	R_L = 600 Ω	2.5		2.5	V
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz − 600 Hz f = 600 Hz − 800 Hz f = 800 Hz − 1000 Hz f = 1000 Hz − 1600 Hz f = 1600 Hz − 2600 Hz f = 2600 Hz − 2800 Hz f = 2800 Hz − 3000 Hz		140 100 50 20 60 80 140	220 145 75 50 100 110 200	μs μs μs μs μs μs μs
D_{RA}	Receive Delay, Absolute	f = 750 Hz		160	180	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz − 1600 Hz f = 1600 Hz − 2600 Hz f = 2600 Hz − 2800 Hz f = 2800 Hz − 3000 Hz		40 90 120 140	60 120 140 175	μs μs μs μs

TRANSMISSION CHARACTERISTICS (continued)

Unless otherwise specified: $T_A = -40\,^{\circ}C$ to $85\,^{\circ}C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GND = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT SECTION TRANSFER CHARACTERISTICS						
G_{XR}	Transmit Gain Relative to Gain at 1020 Hz (0dBm0)	f = 50 Hz - 60 Hz			-35	dB
		f = 60 Hz - 120 Hz			-7	dB
		f = 120 Hz - 200 Hz			-0.15	dB
		f = 200 Hz - 300 Hz	-1.8		+0.15	dB
		f = 300 Hz - 3000 Hz	-0.15		+0.15	dB
		f = 3000 Hz - 3400 Hz	-0.7		+0.15	dB
		f = 3400 Hz - 3600 Hz			+0.15	dB
		f = 3600 Hz - 4000 Hz			0	dB
		f = 4000 Hz - 4600 Hz			-14	dB
		f = 4600 Hz and Up			-32	dB

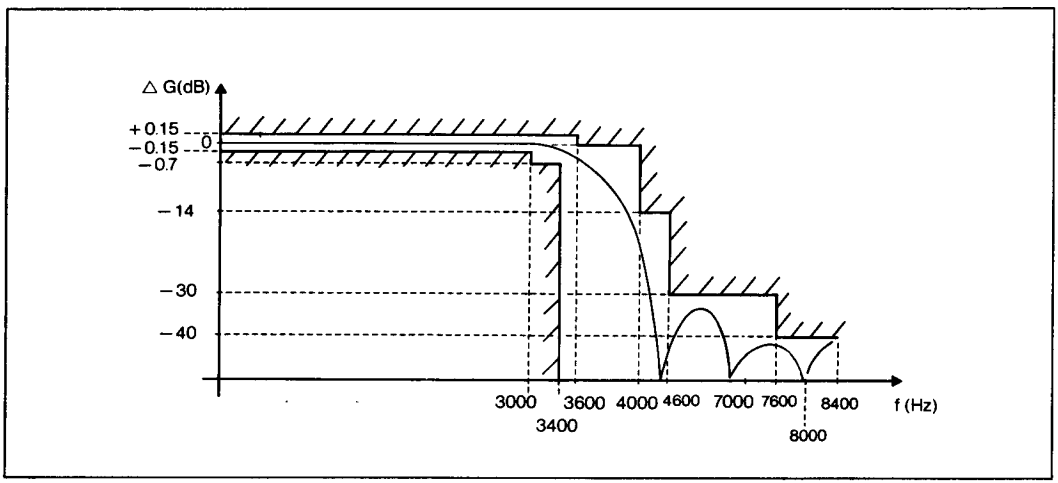




TRANSMISSION CHARACTERISTICS (continued)

Unless otherwise specified : $T_A = -40°C$ to $85°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GND = 0V, f = 1.02 kHz, $V_{IN.}$ = 0 dBm0, transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVE SECTION TRANSFER CHARACTERISTICS						
G_{RR}	Receive Gain Relative to Gain at 1020 Hz (0dBm0)	f = 0 Hz - 3000 Hz	-0,15		+0.15	dB
		f = 3000 Hz - 3400 Hz	-0,7		+0.15	dB
		f = 3400 Hz - 3600 Hz			+0.15	dB
		f = 3600 Hz - 4000 Hz			0	dB
		f = 4000 Hz - 4600 Hz			-14	dB
SOS	Spurious Out-of-Band Signals at the channel Output	Image Signals at VF_RO:				dB
		f = 4600 Hz to 7600 Hz			-30	dB
		f = 7600 Hz to 8400 Hz			-40	dB



TRANSMISSION CHARACTERISTICS (continued)

Unless otherwise specified : $T_A = -40\,°C$ to $85\,°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GND = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
NOISE						
N_{XC}	Transmit Idle Channel Noise, C Message Weighted	HC 3052, HC 3053, HC 3054 $VF_XI^- = OV$		12	15	dBmC0
N_{XP}	Transmit Noise, P Message Weighted	HC 3057 Note 1 $VF_XI^- = OV$ Note 2		−74 −70	−69 −67	dBm0p dBm0p
N_{RC}	Receive Idle Channel Noise C Message Weighted	HC 3052, HC 3053, HC 3054 PCM Code equals alternating Positive and Negative Zero		8	11	dBrnC0
N_{RP}	Receive Idle Channel Noise P Message Weighted	HC 3057 PCM Code equals Positive Zero		−82	−79	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 KHz to 100 KHz, Loop Around Measurement, $VF_XI^+ = 0$ Vrms			−53	dBm0
POWER SUPPLY REJECTION						
$PPSR_X$	Positive Power Supply Rejection Transmit	$VF_XI^+ = 0$ Vrms $V_{CC} = 5.0\,V_{DC} + 100$ mVrms f = 0 − 50 KHz	40			dBC
$NPSR_X$	Negative Power Supply Rejection Transmit	$VF_XI^- = 0$ Vrms $V_{BB} = -5.0\,V_{DC} + 100$ mVrms f = 0 − 50 KHz	40			dBC
$PPSR_R$	Positive Power Supply Rejection Receive	PCM Code equals Positive Zero $V_{CC} = 5.0\,V_{DC} + 100$ mVrms f = 0.4000 Hz f = 0 − 50 KHz	40 25			dBC dB
$NPSR_R$	Negative Power Supply Rejection Receive	PCM Code equals Positive Zero $V_{BB} = -5.0\,V_{DC} + 100$ mVrms f = 0 − 4000 Hz f = 0 − 50 KHz	40 25			dBC dB
DISTORTION						
$STD_{X/R}$	Signal to Total Distortion Transmit or Receive Channel	Sinusoidal Test Method Level = 3.0 dBm0 = 0dBm0 to − 30 dBM0 = − 40 dBm0 XMT RCV = − 55 dBm0 XMT RCV	33 36 29 30 14 15			dBC dBC dbc dBC dBC dBC
SFD_X	Single Frequency Distortion Transmit				−46	dB
SFD_R	Single Frequency Distortion Receive				−46	dB
IMD	Intermodulation Distortion	Loop Around Measurement. $VF_XI^- = -4$ dBm0 to − 21 dBm0, two frequencies in the range 300 Hz to 3 400 Hz			−41	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk 0dBm0 Transmit Level	f = 300 Hz − 3 400 Hz D_R = Steady PCM Code		−90	−75	dB
CT_{R-X}	Receive to Transmit Crosstalk odBm0 Receive Level	f = 300 Hz − 3 400 Hz $VF_XI^- = OV$		−90	−70	dB

Note 1 : Quantization Noise, measured by extrapolation from the distortion result.
Note 2 : Idle Channel Noise, due to alternating sign bit of a perfectly zeroed encoder.

TIMING SPECIFICATIONS

Unless otherwise specified $T_A = -40\,°C$ to $85\,°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GND = 0V

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	160			ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X	100			ns
t_{WBH}	Width of Bit Clock High	$V_{IH} = 2.2V$	160			ns
t_{WBL}	Width of Bit Clock Low	$V_{IL} = 0.6V$	160			ns
t_{HBF}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
t_{SBF}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL loads	0		140	ns
t_{XDP}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL loads			140	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled	$C_L = 0$ pF to 150 pF	50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes later	$C_L = 0$ pF to 150 pF	20		165	ns
t_{SSFF}	Set-Up Time from $SF_{X/R}$ High to $FS_{X/R}$	HC 3053 Only	60			ns
t_{SSFB}	Set-Up Time from Signal Frame Sync High to $BCLK_{X/R}$ Clock	HC 3053 Only	60			ns
t_{SSGB}	Set-Up Time from SIG_X to $BCLK_X$	HC 3052 and HC 3053	100			ns
t_{HBSG}	Hold Time from $BCLK_X$ High to SIG_X	HC 3052 and HC 3053	50			ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		50			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		50			ns
t_{HBSF}	Hold Time from $BCLK_{X/R}$ Low to Signaling Frame Sync	HC 3053 Only	100			ns
t_{SF}	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	50			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	Short frame Sync Pulse (1 Bit Clock Period Long)	100			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Fram Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64K Bit/s Operating Mode	160			ns

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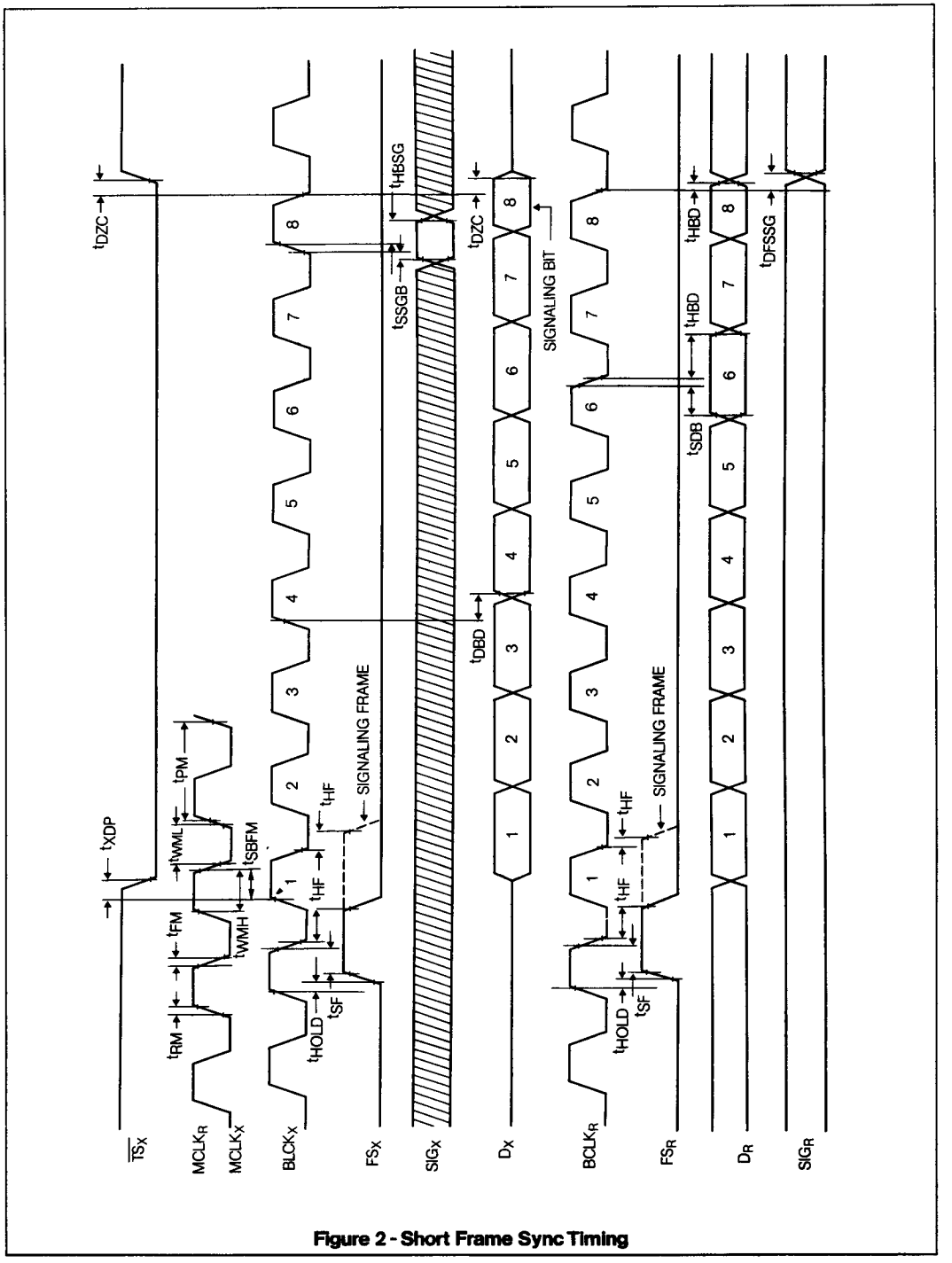


Figure 2 - Short Frame Sync Timing

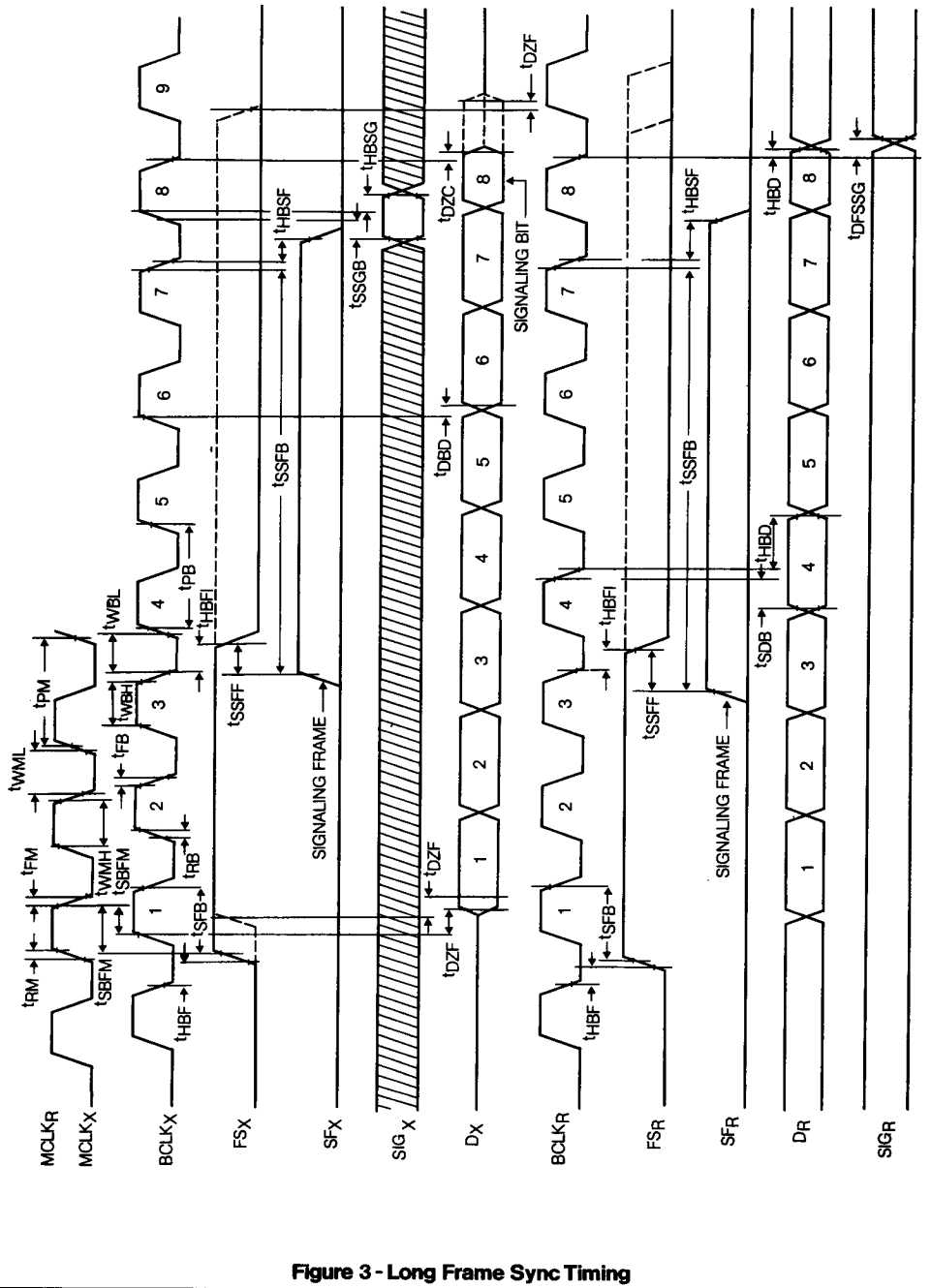


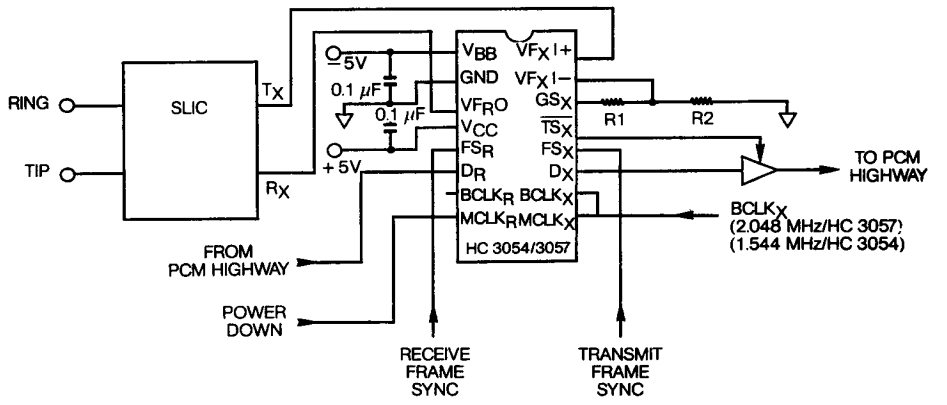
Figure 3 - Long Frame Sync Timing

OPERATING INSTRUCTIONS

Ground should be applied to the device before any other connection. Although V_{CC} and V_{BB} can be connected in any order, one should check that voltages on all inputs and on supply rails stay within absolute maximum ratings even for very short periods to avoid any latch-up. All ground connections to each device should meet at a common point as close as possible to the GND pin.

Two 0.1 µF decoupling capacitors are required from the common ground point to V_{CC} and V_{BB}.

The ground point of each COFIDEC should be tied to a common card ground in star formation, rather than via a ground bus.



Typical Synchronous Application

1