

HM6708SH/HM6709SH Series

TTL I/O**65,536-words × 4-bits High Speed Static Random Access Memory**

Features

- 65,536 words × 4 bits organization
- Fully compatible with TTL input and output
- 0.8 μm Hi-BiCMOS process
- +5 V single power supply
- Completely static memory: No clock or timing strobe required
- Low power dissipation (DC) operating: 400 mW typ
- Super fast access time: 10/12 ns max

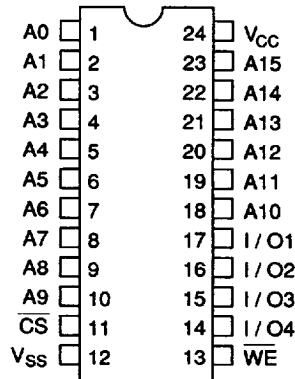
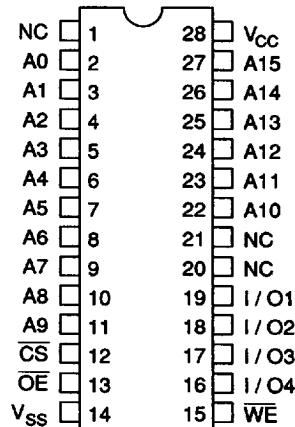
Ordering Information

Type No.	Access time	Package
HM6708SHJP-10	10 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6708SHJP-12	12 ns	
HM6709SHJP-10	10 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM6709SHJP-12	12 ns	

Pin Description

Pin name	Function
A0–A15	Address input
I/O1–I/O4	Data input/output
WE	Write enable
CS	Chip select
OE (for HM6709SH only)	Output enable
V _{SS}	Ground
V _{CC}	Power supply
NC	No connection

Pin Arrangement

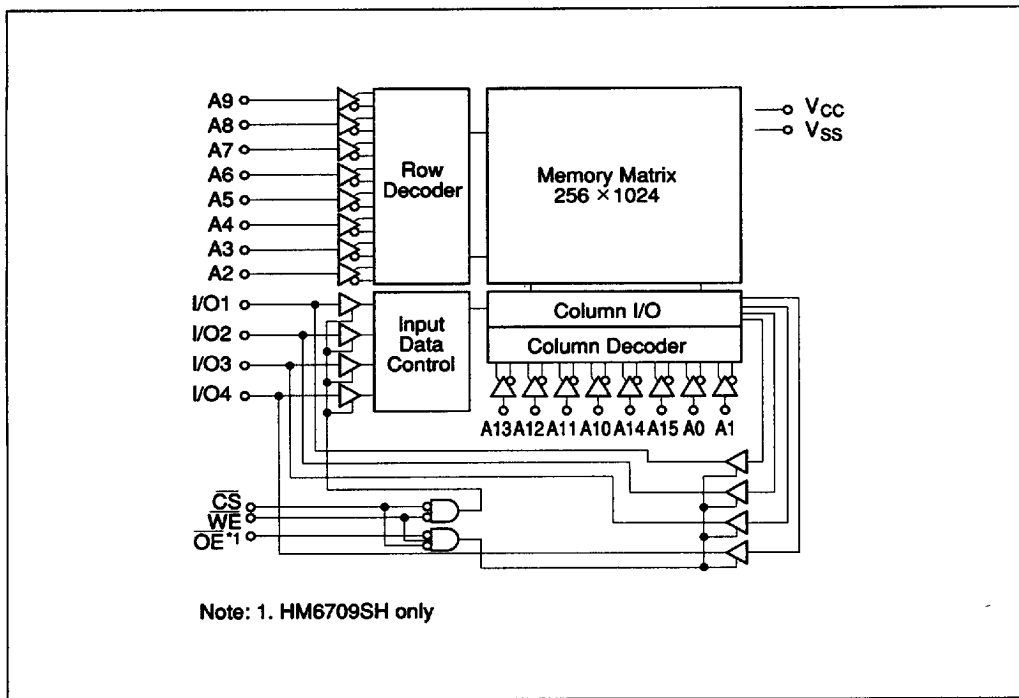
HM6708SH Series**(Top View)****HM6709SH Series****(Top View)****2****4496203 0024717 627****HITACHI**

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Block Diagram



Function Table (HM6708SH)

Input

CS	WE	Mode	I/O pin	V _{CC} current	Reference cycle
H	X	Not selected	High Z	I _{SB} , I _{SB1}	—
L	H	Read	Data out	I _{CC} , I _{CC1}	Read cycle (2), (3)
L	L	Write	Data in	I _{CC} , I _{CC1}	Write cycle (1), (2)

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Function Table (HM6709SH)

Input

CS	WE	OE	Mode	I/O pin	V _{CC} current	Reference cycle
H	X	X	Not selected	High Z	I _{SB} , I _{SB1}	—
L	H	H	Output disable	High Z	I _{CC} , I _{CC1}	—
L	H	L	Read	Data out	I _{CC} , I _{CC1}	Read cycle (1), (2), (3)
L	L	H	Write	Data in	I _{CC} , I _{CC1}	Write cycle (1), (2), (3), (4)
L	L	L	Write	Data in	I _{CC} , I _{CC1}	Write cycle (5), (6)

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage with respect to V _{SS} pin	V _{CC}	−0.5 to +7.0	V
Terminal voltage with respect to V _{SS} pin	V _T	−0.5 to V _{CC} + 0.5	V
Power dissipation	P _T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (Bias)	−10 to +85	°C
Storage temperature range	Tstg	−55 to +125	°C

For the AC and DC specifications shown in these tables, the devices were tested with a minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions (0°C ≤ Ta ≤ 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0.0	0.0	0.0	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.5	V
Input low voltage	V _{IL}	−3.0 ¹	—	0.8	V

Note: 1. Pulse width 10 ns, DC: −0.5 V

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DC Characteristics ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $T_a = 0 \text{ to } +70^\circ\text{C}$)

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Parameter	Symbol	-10			-12			Unit	Test conditions
		Min	Typ*1	Max	Min	Typ*1	Max		
Input leakage current	$ I_{LI} $	—	—	2	—	—	2	μA	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0 \text{ V}$ to V_{CC}
Output leakage current	$ I_{LO} $	—	—	10	—	—	10	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$, $\overline{WE} = V_{IL}$, $V_{I/O} = 0 \text{ V}$ to V_{CC}
Operating power supply current	I_{CC}	—	60	100	—	60	100	mA	$\overline{CS} = V_{IL}$, $I_{I/O} = 0 \text{ mA}$
Average operating current	I_{CC1}	—	130	180	—	120	175	mA	Min. cycle, $I_{I/O} = 0 \text{ mA}$
Standby power supply current	I_{SB}	—	—	40	—	—	40	mA	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL}
	I_{SB1}	—	—	30	—	—	30	mA	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CC} - 0.2 \text{ V}$
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	$I_{OL} = 8 \text{ mA}$
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	$I_{OH} = -4 \text{ mA}$

Note: 1. Typical limits are: $V_{CC} = 5.0 \text{ V}$, $T_a = 25^\circ\text{C}$, and specified loading.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameter	Symbol	Max	Unit	Test condition
Input capacitance	C_{in}^{*1}	6	pF	$V_{in} = 0 \text{ V}$
Output capacitance	$C_{I/O}^{*1}$	10	pF	$V_{I/O} = 0 \text{ V}$

Note: 1. This parameter is sampled and is not 100% tested.

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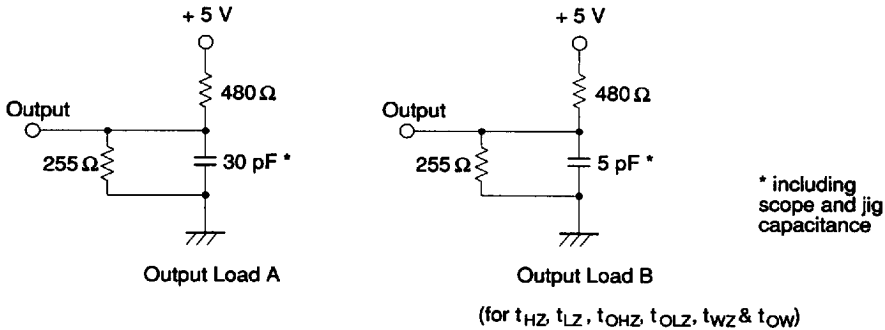
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AC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$ unless otherwise noted)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figure
- Input rise and fall times: 4 ns
- Output reference levels: 1.5 V



Read Cycle

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Parameter	Symbol	-10		-12		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	10	—	12	—	ns
Address access time	t_{AA}	—	10	—	12	ns
Chip select access time	t_{ACS}	—	10	—	12	ns
Chip selection to output in low Z	$t_{LZ}^{*1, *2}$	3	—	3	—	ns
Output enable to output valid	t_{OE}^{*3}	—	5	—	6	ns

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Read Cycle (cont)

		HM6708SH/HM6709SH				
		-10		-12		
Parameter	Symbol	Min	Max	Min	Max	Unit
Output enable to output in low Z	t _{OLZ} ^{*1, *2, *3}	0	—	0	—	ns
Chip deselection to output in high Z	t _{HZ} ^{*1, *2}	0	5	0	5	ns
Output hold from address change	t _{OH}	3	—	3	—	ns

Notes: 1. This parameter is sampled and is not 100% tested.
2. Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).
3. These parameters are for HM6709SH.

Write Cycle

		HM6708SH/HM6709SH				
		-10		-12		
Parameter	Symbol	Min	Max	Min	Max	Unit
Write cycle time	t _{WC} ^{*1}	10	—	12	—	ns
Chip selection to end of write	t _{CW}	8	—	9	—	ns
Address valid to end of write	t _{AW}	10	—	11	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write pulse width	t _{WP}	8	—	9	—	ns
Write recovery time	t _{WR}	0	—	0	—	ns
Data valid to end of write	t _{DW}	6	—	6	—	ns
Data hold time	t _{DH}	0	—	0	—	ns
Write enable to output in high Z	t _{WZ} ^{*2, *3}	0	5	0	6	ns
Output disable to output in high Z	t _{OHZ} ^{*2, *3, *4}	0	6	0	6	ns
Output active from end of write	t _{OW} ^{*2, *3}	3	—	3	—	ns

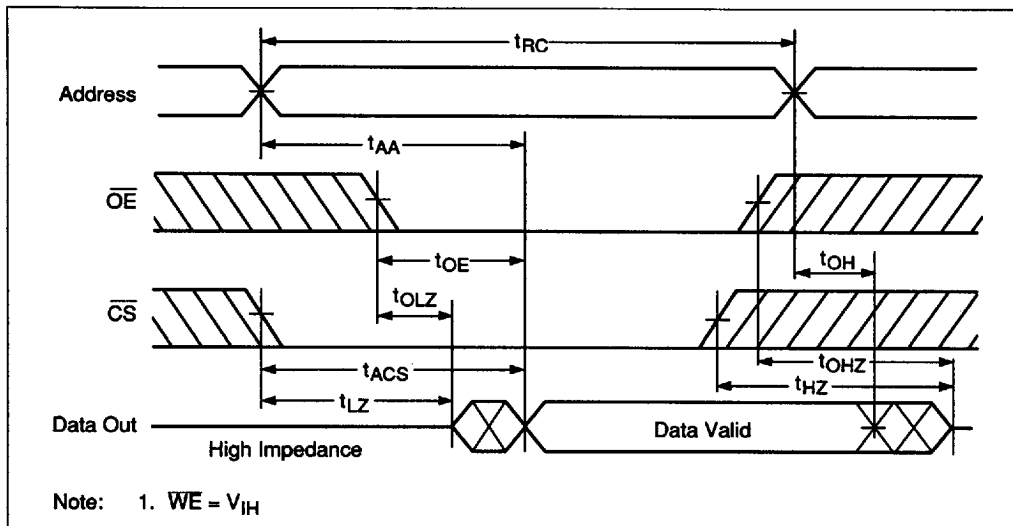
Notes: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and is not 100% tested.
3. Transition is measured ± 200 mV from steady state voltage with loading specified in Load (B).
4. These parameters are for HM6709SH.

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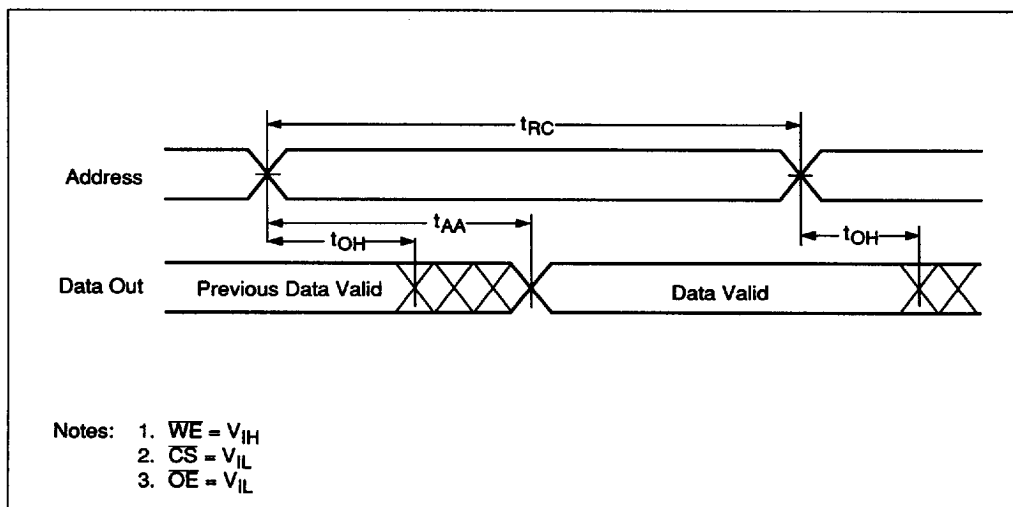
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Timing Waveforms

Read Cycle 1



Read Cycle 2



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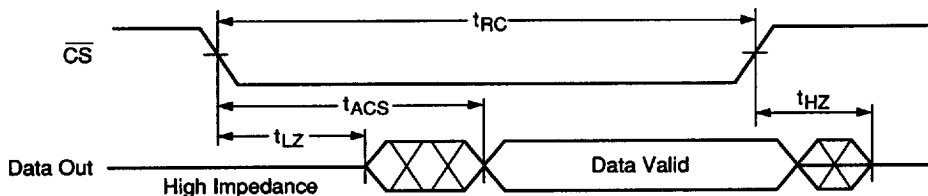
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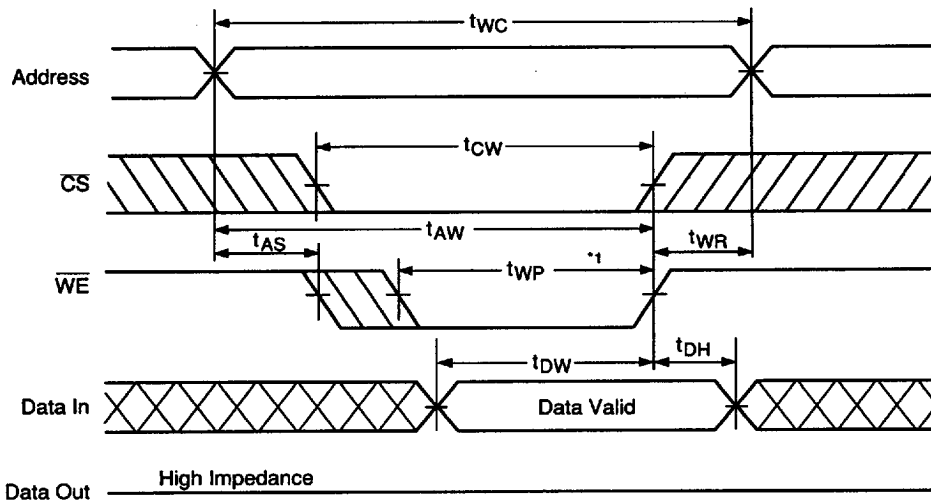
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Read Cycle 3



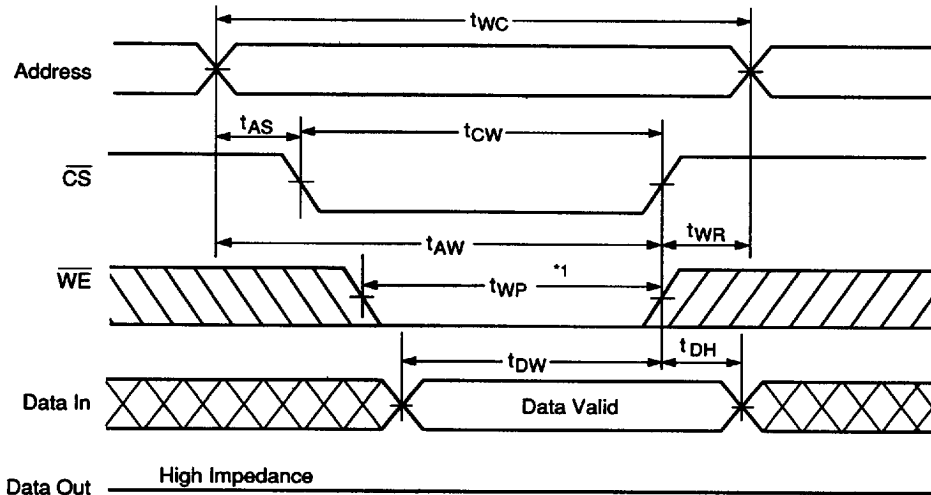
- Notes:
1. $\overline{WE} = V_{IH}$
 2. $\overline{OE} = V_{IL}$
 3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle 1 ($\overline{OE} = H$, $\overline{WE}$ controlled)



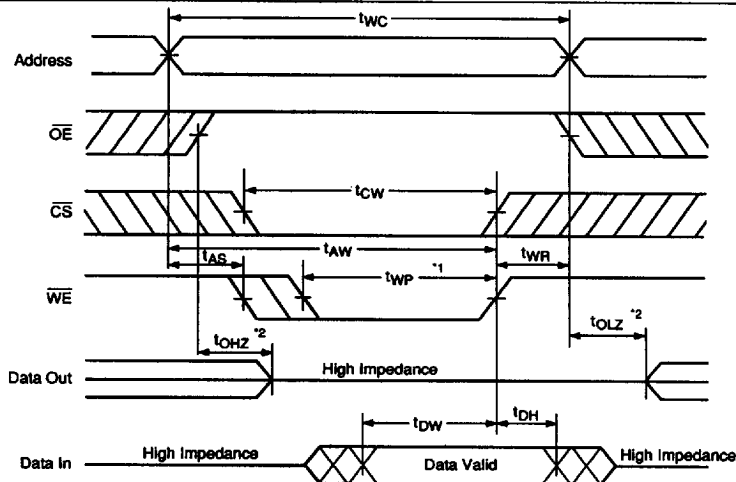
- Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 2 ($\overline{OE} = H$, $\overline{CS}$ controlled)



Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 3 ($\overline{OE}$ = clocked, $\overline{WE}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

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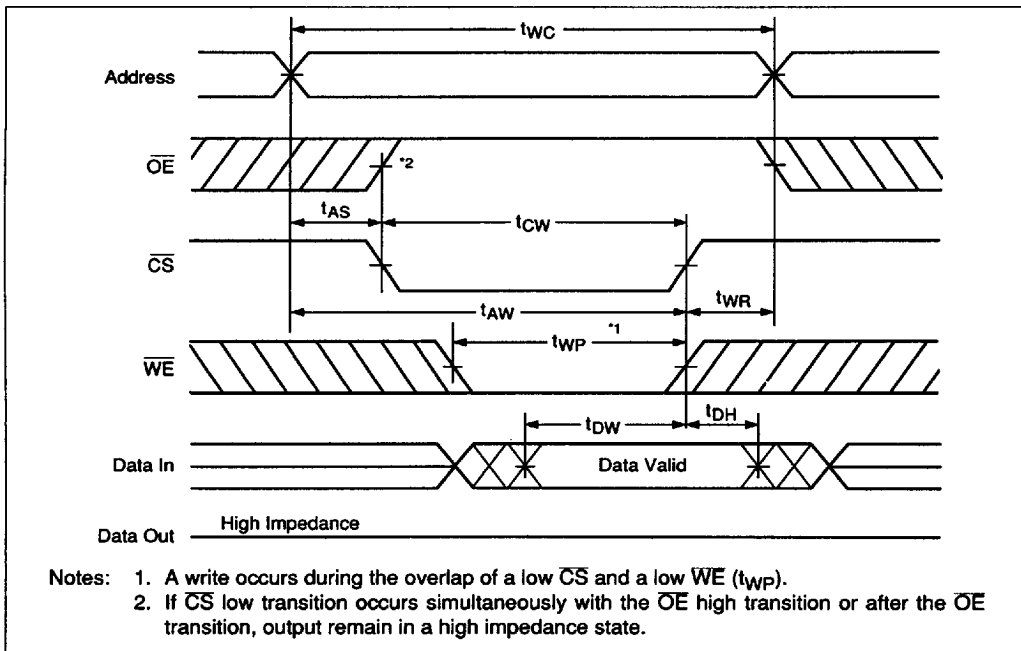
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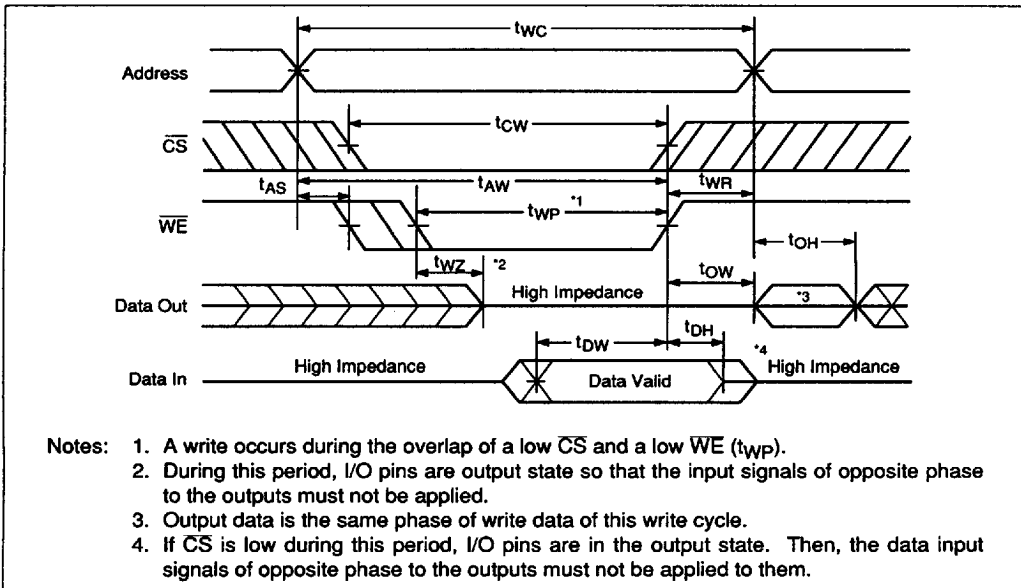
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Write Cycle 4 ($\overline{OE}$ = clocked, $\overline{CS}$ controlled)



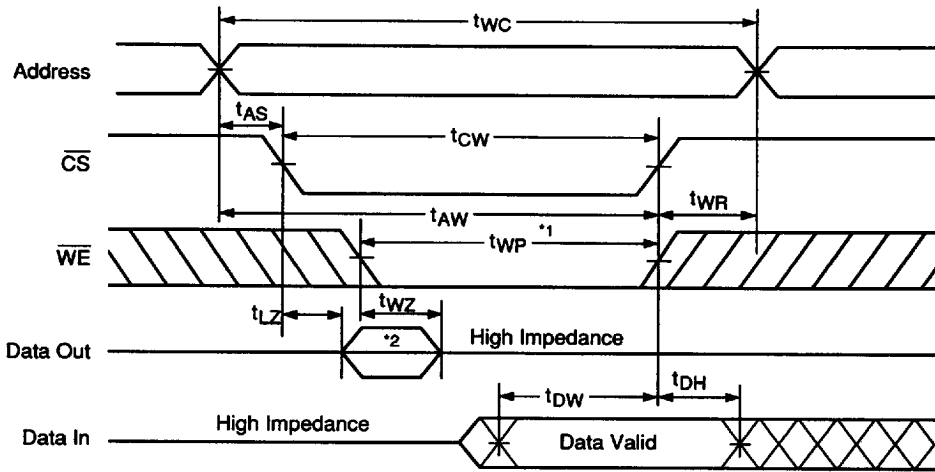
Write Cycle 5 ($\overline{OE}$ = L, $\overline{WE}$ controlled)



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Write Cycle 6 ($\overline{OE} = L$, $\overline{CS}$ controlled)



- Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
 2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.