HYM5V72A804A H-Series

Buffered 8Mx72 bit CMOS DRAM MODULE
based on 8Mx8 DRAM, EDO, ECC, 3.3V, 4K/8K-Refresh

DESCRIPTION

The HYM5V72A804A H-Series is a 8Mx72-bit EDO mode CMOS DRAM module consisting of nine 8Mx8 TSOP and 16-bit BiCMOS line driver in TSSOP on a 168 pin glass-epoxy printed circuit board. 0.1µF and 0.01µF decoupling capacitors are mounted for each DRAM. The HYM5V72A804AH G-series is gold plated socket type Dual In-line Memory Module suitable for easy interchange and addition of 64M byte memory.

FEATURES

- Max. Active Power Dissipation

Speed	8K	4K
50	3.60W	4.57W
60	2.95W	3.92W

- Fast access time and cycle time

Speed	tRAC	tCAC	tHPC
50	50ns	18ns	25ns
60	60ns	20ns	30ns

- 168-Pin Buffered DIMM
- Buffered inputs (except /RAS and DQ)
- Parallel Presence Detect with PD/ID pin Matrix
- Extended Data Out Operation
- Single power supply of 3.3V ± 10%
- Read-Modify-Write Capability
- LVTTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self refresh capability
- Refresh cycles

Part No.	Ref.
HYM5V72A804A H-Series	4K
HYM5V72A834A H-Series	8K£ [a]

£ ÆCAS-before-/RAS refresh, Hidden refresh mode : 4K cycles / 64ms

PIN DISCRIPTION

/RAS0, /RAS2	Row Address Strobe
/CAS0, /CAS4,	Column Address Strobe
/WE0, /WE2	Write Enable
/OE0, /OE2	Output Enable
A0, B0, A1-A12	Address Input(8K Product)
A0, B0, A1-A11	Address Input(4K Product)
DQ0-DQ71	Data Input / Output
PD1-PD8	Presence Detect
/PDE	Presence Detect Enable
ID0, ID1	ID Bit
VCC	Power (+3.3V)
VSS	Ground

PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	/OE2	86	DQ36	128	NC
3	DQ1	45	/RAS2	87	DQ37	129	NC
4	DQ2	46	/CAS4	88	DQ38	130	NC
5	DQ3	47	NC	89	DQ39	131	NC
6	Vcc	48	/WE2	90	Vcc	132	/PDE
7	DQ4	49	Vcc	91	DQ40	133	Vcc
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	Vcc	101	DQ49	143	Vcc
18	Vcc	60	DQ24	102	Vcc	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	NC	106	DQ53	148	NC
23	Vss	65	DQ25	107	Vss	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE0	69	DQ28	111	NC	153	DQ64
28	/CAS0	70	DQ29	112	NC	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ66
30	/RAS0	72	DQ31	114	NC	156	DQ67
31	/OE0	73	Vcc	115	NC	157	Vcc
32	Vss	74	DQ32	116	Vss	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	*A12	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	NC	83	ID0	125	NC	167	ID1
42	NC	84	Vcc	126	B0	168	Vcc

NOTE :
1.A12 is used for 8K-Refresh Product (HYM5V72A834A H-Series)

PRESENCE DETECT PINS

PIN	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8	ID0	ID1
-50	NC	Vss	NC	NC	NC	Vss	Vss	Vss	Vss	Vss/NC
-60	NC	Vss	NC	NC	NC	NC	NC	Vss	Vss	Vss/NC

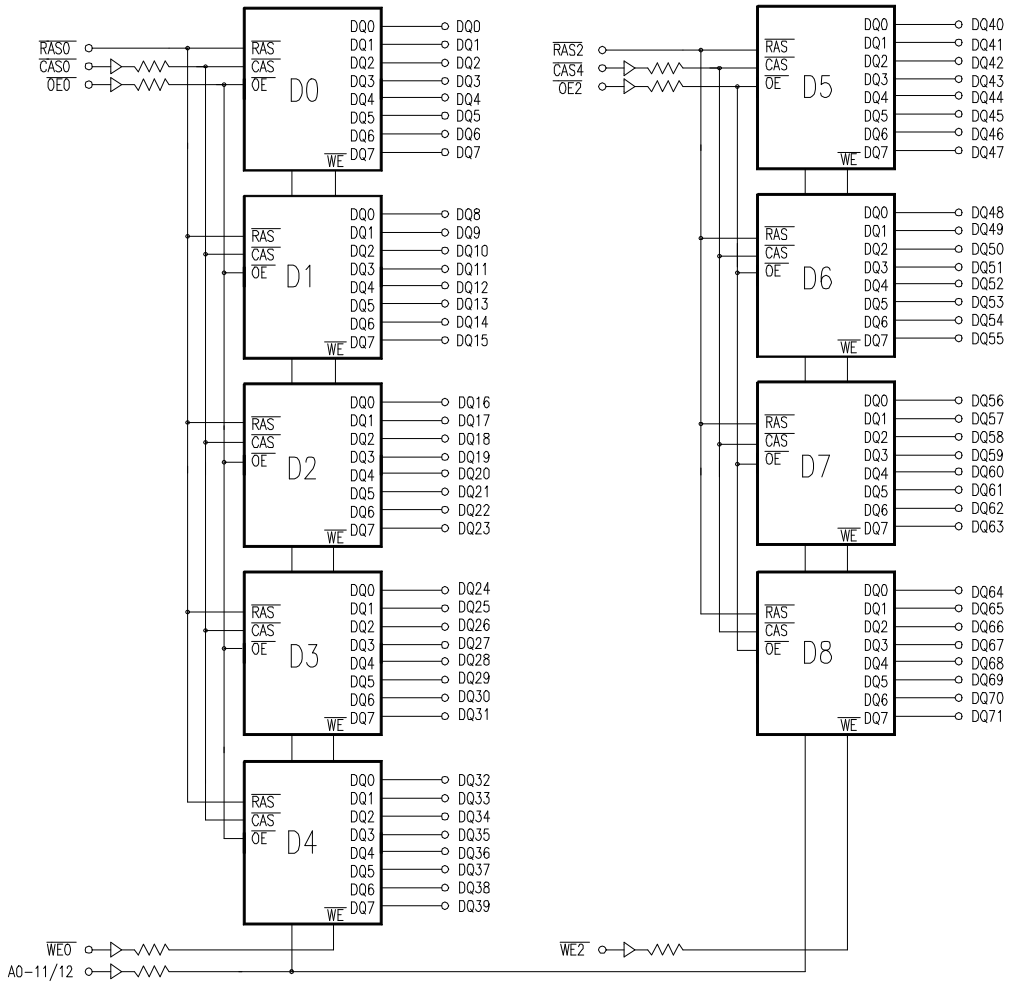
NOTE :

1.PDs are either open NC or driven to Vss via on-board buffer circuit.

2.IDs are connected directly to NC or Vss without a buffer.

3.ID1 will be either open NC for Self-Refresh or driven to Vss for standard.

BLOCK DIAGRAM



NOTE : 1.A12 is used for 8K-Refresh Product (HYM5V72A834A H-Series)

2. All resistors are 25Ohm±5%

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin relative to V_{SS}	-0.5 to 4.6	V
V_{CC}	Voltage on V_{CC} relative to V_{SS}	-0.5 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	11.4	W
T_{SOLDER}	Soldering Temperature•Time	260•10	°C•sec

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

Note: All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C , V_{CC}=3.3V ± 10%, V_{SS}=0V, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Speed	Max. Current		Unit
				8K Product	4K Product	
I_{CC1}	Operating Current	/RAS, /CAS Cycling tRC=tRC (min.)	50 60	1000 820	1270 1090	mA
I_{CC2}	LVTTL Standby Current	/RAS = /CAS ≥ V_{IH} other inputs ≥ V_{SS}		9.18	9.18	mA
I_{CC3}	/RAS-only Refresh Current	/RAS cycling /CAS = V_{IH} tRC = tRC (min.)	50 60	1000 820	1270 1090	mA
I_{CC4}	EDO Mode Current	/CAS cycling /RAS = V_{IL} tHPC = tHPC (min.)	50 60	1090 910	1180 1000	mA
I_{CC5}	CMOS Standby Current	/RAS = /CAS ≥ V_{CC} - 0.2V	SL-part	4.68 2.88	4.68 2.88	mA
I_{CC6}	/CAS-before-/RAS Refresh Current	tRC=tRC (min.)	50 60	1000 820	1270 1090	mA
I_{CC7}	Battery Back-up Current (SL-part)	V_{IH} = V_{CC} - 0.2V, V_{IL} = 0.2V /CAS = CBR cycling or 0.2V /OE & /WE = V_{IH} = V_{CC} - 0.2V Address = Don`t care DQ0-DQ71 = Open		5.13	5.13	mA
I_{CC8}	Self Refresh Current (SL-part)	/RAS & /CAS = 0.2V Other pins are same as I_{CC7}		4.23	4.23	mA

Symbol	Parameter	Test Condition		Min.	Max	Unit
I_{LI}	Input Leakage current(Any Input)	V_{SS} ≤ V_{IN} ≤ V_{CC} + 0.3, All other pins not under test=V_{SS}	All but /RAS /RAS	-10 -22.5	10 22.5	µA
I_{LO}	Output Leakage current(Any Input)	V_{SS} ≤ V_{OUT} ≤ V_{CC} /RAS & /CAS at V_{IH}		-5	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA		-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.0mA		2.4	-	V

NOTE

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} dependent on output loading and cycle rates(tRC and tHPC).
2. Specified values are obtained with outputs unloaded.
3. I_{CC} is specified as an average current. In I_{CC}1, I_{CC}3, I_{CC}6, address can be changed only once while /RAS=VIL. In I_{CC}4, address can be changed maximum once while /CAS=V_{IH} within one EDO mode cycle time tHPC.
4. Only /RAS(max.) = 1µs is applied to refresh of battery backup but tRAS(max.) = 10µs is applied to normal functional operation.
5. I_{CC}5(max.) = 2.88mA, I_{CC}7 and I_{CC}8 are applied to SL-part only.
6. V_{OH} = 2.0V, V_{OL} = 0.8V at AC Functional Test.

AC CHARACTERISTICS

(T_A=0°C to 70°C , Vcc=3.3V ± 10%, Vss=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	-50		-60		-70		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	90	-	110	-			ns	
2	tRWC	Read-Modify-Write Cycle Time	128	-	153	-			ns	14
3	tHPC	EDO Mode Cycle Time	25	-	30	-			ns	
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	70	-	77	-			ns	14
5	tRAC	Access Time from /RAS	-	50	-	60			ns	4,5,10,11
6	tCAC	Access Time from /CAS	-	18	-	20			ns	4,5,10,14
7	tAA	Access Time from Column Address	-	30	-	35			ns	4,5,11,14
8	tCPA	Access Time from /CAS Precharge	-	35	-	40			ns	4,14
9	tCLZ	/CAS to Output Low Impedance	8	-	8	-			ns	3,14
10	tCEZ	Out Buffer Turn-off delay from /CAS	8	18	8	18			ns	14
11	tT	Transition Time (Rise and Fall)	2	50	2	50			ns	4
12	tRP	/RAS Precharge Time	30	-	40	-			ns	
13	tRAS	/RAS Pulse Width	50	10K	60	10K			ns	
14	tRASP	/RAS Pulse Width (EDO Mode)	50	100K	60	100K			ns	
15	tRSH	/RAS Hold Time	18	-	20	-			ns	14
16	tCSH	/CAS Hold Time	38	-	43	-			ns	14
17	tCAS	/CAS Pulse Width	8	10K	10	10K			ns	
18	tRCD	/RAS to /CAS Delay	15	32	18	40			ns	10,14
19	tRAD	/RAS to Column Address Delay Time	11	20	13	25			ns	11,14
20	tCRP	/CAS to /RAS Precharge Time	10	-	10	-			ns	14
21	tCP	/CAS Precharge Time	8	-	10	-			ns	
22	tASR	Row Address Set-up Time	5	-	5	-			ns	14
23	tRAH	Row Address Hold Time	6	-	8	-			ns	14
24	tASC	Column Address Set-up Time	0	-	0	-			ns	
25	tCAH	Column Address Hold Time	8	-	10	-			ns	
26	tAR	Column Address Hold Time from /RAS	43	-	48	-			ns	14
27	tRAL	Column Address to /RAS Lead Time	30	-	35	-			ns	14
28	tRCS	Read Command Set-up Time	0	-	0	-			ns	
29	tRCH	Read Command Hold Time Referenced to /CAS	0	-	0	-			ns	7
30	tRRH	Read Command Hold Time Referenced to /RAS	-2	-	-2	-			ns	14
31	tWCH	Write Command Hold Time	10	-	10	-			ns	
32	tWCR	Write Command Hold Time from /RAS	38	-	43	-			ns	14
33	tWP	Write Command Pulse Width	8	-	10	-			ns	
34	tRWL	Write Command to /RAS Lead Time	20	-	20	-			ns	14
35	tCWL	Write Command to /CAS Lead Time	8	-	10	-			ns	

AC CHARACTERISTICS

#	SYMBOL	PARAMETER	-50		-60		-70		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	tDS	Data-In Set-up Time	-2	-	-2	-			ns	8,14
37	tDH	Data-In Hold Time	15	-	15	-			ns	8,14
38	tDHR	Data-In Hold Time Referenced to /RAS	40	-	45	-			ns	
39	tREF	Refresh Period (8192 cycles)	-	64	-	64			ms	12,13
		Refresh Period (4096 cycles)	-	64	-	64			ms	12
		Refresh Period (SL-part)	-	128	-	128			ms	12,13
40	tWCS	Write Command Set-up Time	0	-	0	-			ns	9
41	tCWD	/CAS to /WE Delay Time	33	-	38	-			ns	9
42	tRWD	/RAS to /WE Delay Time	68	-	82	-			ns	9,14
43	tAWD	Column Address to /WE Delay Time	45	-	53	-			ns	9
44	tCSR	/CAS Set-up Time (CBR Cycle)	10	-	10	-			ns	14
45	tCHR	/CAS Hold Time (CBR Cycle)	8	-	8	-			ns	14
46	tRPC	/RAS to /CAS Precharge Time	3	-	3	-			ns	14
47	tCPT	/CAS Precharge Time (CBR Counter Test)	25	-	30	-			ns	
48	tROH	/RAS Hold Time Reference to /OE	10	-	10	-			ns	14
49	tOEA	/OE Access Time	-	18	-	20			ns	14
50	tOED	/OE to Data Delay	18	-	20	-			ns	14
51	tOEZ	Output Buffer Turn Off Delay Time from /OE	8	18	8	18			ns	6,14
52	tOEH	/OE Command Hold Time	13	-	15	-			ns	
53	tCPWD	/WE Delay Time from /CAS Precharge	47	-	58	-			ns	9
54	tRHCP	/RAS Hold Time from /CAS Precharge	35	-	40	-			ns	14
55	tWRP	/WE to /RAS Precharge Time(CBR cycle)	12	-	12	-			ns	14
56	tWRH	/WE to /RAS Hold Time (CBR cycle)	8	-	8	-			ns	14
57	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-			ns	
58	tWTH	Write Command Hold Time (Test Mode In)	10	-	10	-			ns	
59	tRASS	/RAS Pulse Width (Self Refresh)	100K	-	100K	-			us	
60	tRPS	/RAS Precharge Time (Self Refresh)	100	-	110	-			ns	
61	tCHS	/CAS Hold Time (Self Refresh)	-50	-	-50	-			ns	
62	tDOH	Output Data Hold Time	10	-	10	-			ns	14
63	tREZ	Output Buffer Turn- off Delay from /RAS	0	10	0	15			ns	6
64	tWEZ	Output Buffer Turn- off Delay from /WE	0	15	0	20			ns	6,14
65	tWED	/WE to Data Delay Time	20	-	20	-			ns	
66	tOEP	/OE Precharge Time	5	-	5	-			ns	
67	tWPE	/WE Pulse Width (EDO cycle)	5	-	5	-			ns	
68	tOCH	/OE to /CAS Hold Time	5	-	5	-			ns	
69	tCHO	/CAS Hold Time to /OE	5	-	5	-			ns	
70	tPD	/PDE to Valid Presence Detect Data	-	10	-	10			ns	
71	tPDOFF	/PDE Inactive to Presence Detect Inactive	2	7	2	7			ns	

NOTE

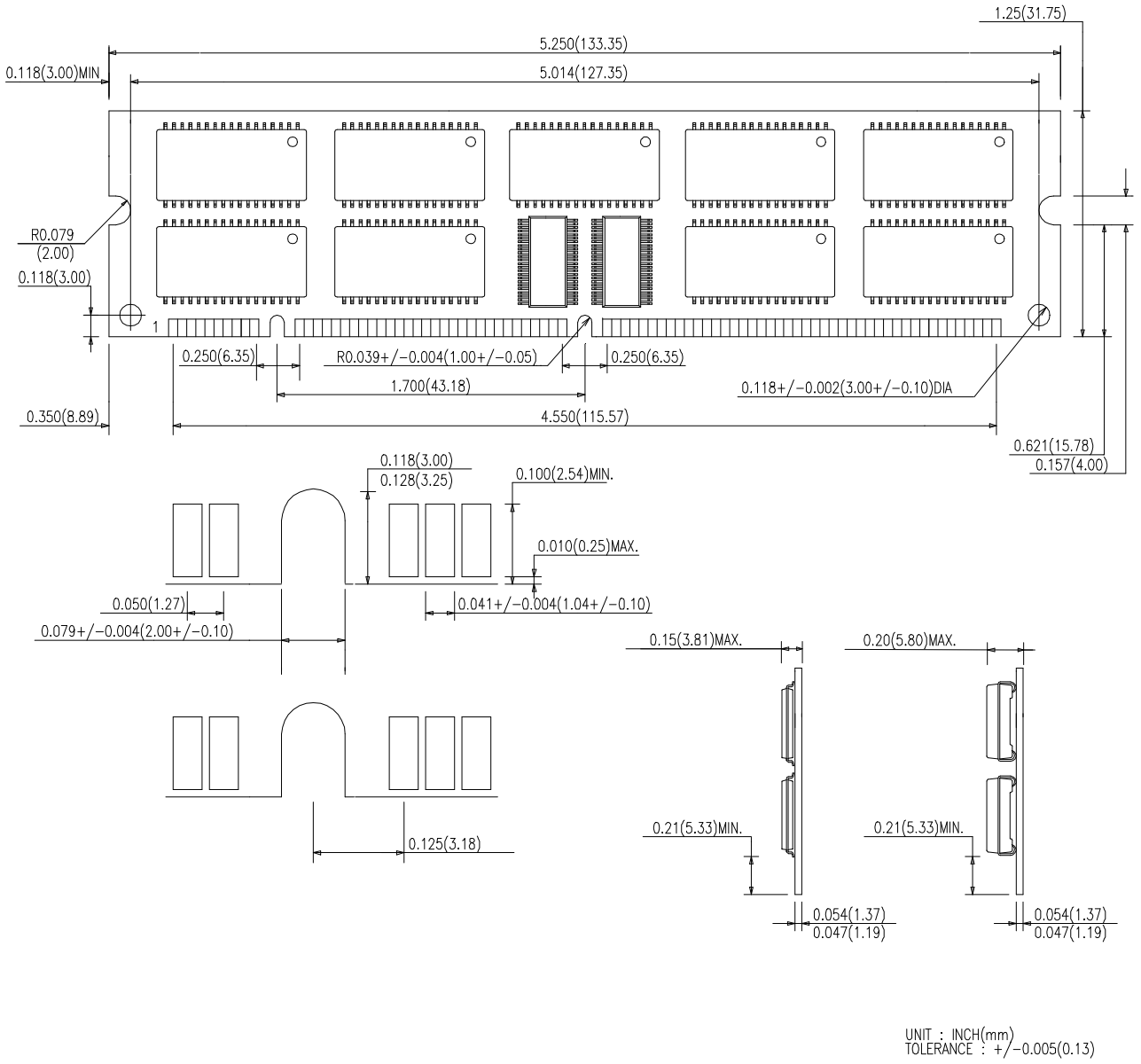
1. An initial pause of 200μs is required after power-up followed by 8 /RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 /CAS-before-/RAS initialization cycles instead of 8 /RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode during initialization.
2. If /RAS=Vss during power-up, the HYM5V72A804A / HYM5V72A834A could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up.
3. It is recommended that /RAS and /CAS track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
4. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min.) and V_{IL}(max.), and are assumed to be 5ns for all inputs.
5. Measured at V_{OH}=2.0V and V_{OL}=0.8V with a load equivalent to 1 TTL loads and 100pF.
6. tWEZ, tREZ, tCEZ and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles and late Write cycle.
9. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS ≥ tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tRWD ≥ tRWD(min.), tCWD ≥ tCWD(min.), tAWD ≥ tAWD(min.), and tCPWD ≥ tCPWD(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
10. Operation within the tRCD(max.) limit ensures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
11. Operation within the tRAD(max.) limit ensures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
12. tREF(max.)=256ms is applied to SL-parts.
13. A burst of 8192 /CAS-before-/RAS refresh cycles must be executed within 64ms (256ms for SL-parts) after exiting self refresh. (CBR refresh & Hidden refresh : 4K cycle/64ms)
14. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

CAPACITANCE

(T_A=0°C to 70°C , Vcc=3.3V ± 10%, Vss=0V, f = 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0 - A12)	-	18	pF
C_{IN2}	Input Capacitance (/WE0, /WE2, /OE0, /OE2)	-	18	pF
C_{IN3}	Input Capacitance (/RAS0, /RAS2)	-	45	pF
C_{IN4}	Input Capacitance (/CAS0, /CAS4)	-	18	pF
C_{DQ}	Data Input /Output Capacitance (DQ0 - DQ71)	-	14	pF

PACKAGE INFORMATION



UNIT : INCH(mm)
TOLERANCE : +/-0.005(0.13)

ORDERING INFORMATION

Part Number	Ref.	Power	Package
HYM5V72A804ATHG	4K	Normal	TSOP
HYM5V72A804ASLTHG	4K	SL-part	TSOP
HYM5V72A834ATHG	8K	Normal	TSOP
HYM5V72A834ASLTHG	8K	SL-part	TSOP