

Integrated Device Technology, Inc.

CMOS PARALLEL-TO-SERIAL FIFO
 256 x 16, 512 x 16, 1024 x 16

IDT72105
 IDT72115
 IDT72125

T-46-35

FEATURES:

- 25ns parallel port access time, 35ns cycle time
- 45MHz serial output shift rate
- Wide x16 organization offering easy expansion
- Low power consumption (50mA typical)
- Least/Most Significant Bit first read selected by asserting the FL/DIR pin
- Four memory status flags: Empty, Full, Half-Full, and Almost-Empty/Almost-Full
- Dual-port zero fall-through architecture
- Available in 28-pin 300 mil plastic and ceramic DIP, 28-pin SOIC, 32-pin LCC and 32-pin PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72105/72115/72125s are very high speed, low power dedicated parallel-to-serial FIFOs. These FIFOs possess a 16-bit parallel input port and a serial output port with 256, 512 and 1K word depths, respectively.

The ability to buffer wide word widths (x16) make these FIFOs ideal for laser printers, FAX machines, local area networks (LANs), video storage and disk/tape controller applications.

Expansion in width and depth can be achieved using multiple chips. IDT's unique serial expansion logic makes this possible using a minimum of pins.

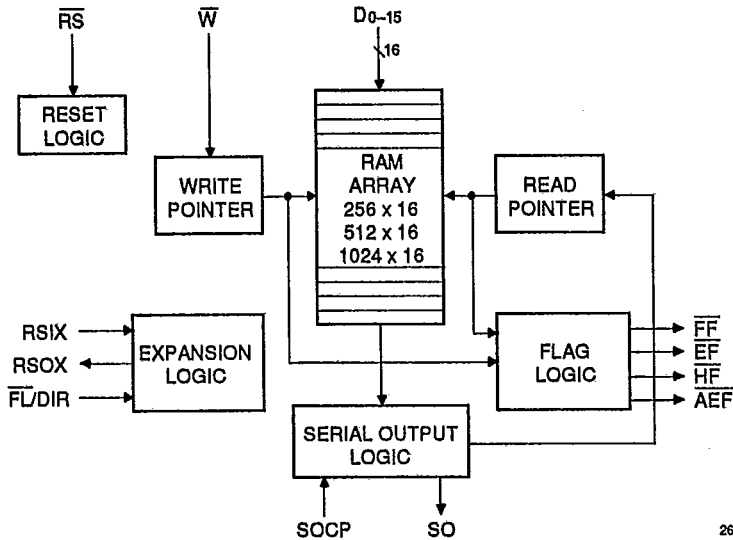
The unique serial output port is driven by one data pin (SO) and one clock pin (SOCP). The Least Significant or Most Significant Bit can be read first by programming the DIR pin after a reset.

Monitoring the FIFO is eased by the availability of four status flags: Empty, Full, Half-Full and Almost-Empty/Almost-Full. The Full and Empty flags prevent any FIFO data overflow or underflow conditions. The Half-Full Flag is available in both single and expansion mode configurations. The Almost-Empty/Almost-Full Flag is available only in a single device mode.

The IDT72105/15/25 are fabricated using IDT's leading edge, submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.



FUNCTIONAL BLOCK DIAGRAM



2685 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

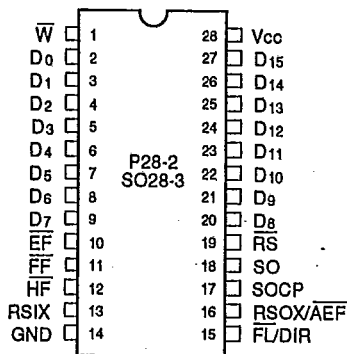
MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1992

©1992 Integrated Device Technology, Inc.

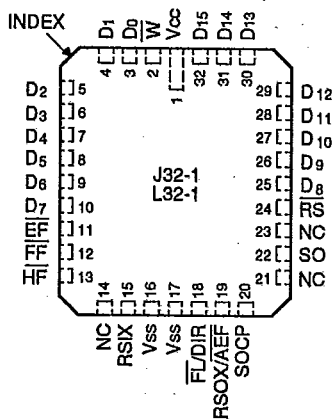
PIN CONFIGURATIONS

T-46-35



DIP/SOIC
TOP VIEW

2665 drw 02a



LCC/PLCC
TOP VIEW

2665 drw 02b

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0-D15	Inputs	I	Data inputs for 16-bit wide data.
RS	Reset	I	When RS is set low, internal READ and WRITE pointers are set to the first location of the RAM array. FF and HF go HIGH. EF and AEF go LOW. A reset is required before an initial WRITE after power-up. W must be high during the RS cycle. Also the First Load pin (FL) is programmed only during Reset.
W	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag (FF) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag (EF) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
FL/DIR	First Load/Direction	I	This is a dual purpose input used in the width and depth expansion configurations. The First Load (FL) function is programmed only during Reset (RS) and a LOW on FL indicates the first device to be loaded with a byte of data. All other devices should be programmed HIGH. The Direction (DIR) pin controls shift direction after Reset and tells the device whether to read out the Least Significant or Most Significant bit first.
RSIX	Read Serial In Expansion	I	In the single device configuration, RSIX is set HIGH. In depth expansion or daisy chain expansion, RSIX is connected to RSOX (expansion out) of the previous device.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out LSB or MSB depending on the Direction pin programming. During Expansion the SO pins are tied together.
FF	Full Flag	O	When FF goes LOW, the device is full and further WRITE operations are inhibited. When FF is HIGH, the device is not full.
EF	Empty Flag	O	When EF goes LOW, the device is empty and further READ operations are inhibited. When EF is HIGH, the device is not empty.
HF	Half-Full Flag	O	When HF is LOW, the device is more than half-full. When HF is HIGH, the device is empty to half-full.
RSOX/AEF	Read Serial Out Expansion Almost-Empty, Almost-Full Flag	O	This is a dual purpose output. In the single device configuration (RSIX HIGH), this is an AEF output pin. When AEF is LOW, the device is empty-to-(1/8 full -1) or (7/8 full +1)-to-full. When AEF is HIGH, the device is 1/8-full up to 7/8-full. In the Expansion configuration (RSOX connected to RSIX of the next device) a pulse is sent from RSOX to RSIX to coordinate the width, depth or daisy chain expansion.
Vcc	Power Supply		Single power supply of 5V.
GND	Ground		Single ground of 0V.

2665 tbl 01

T-46-35

STATUS FLAGS

Number of Words in FIFO			FF	AEF	HF	EF
IDT72105	IDT72115	IDT72125				
0	0	0	H	L	H	L
1-31	1-63	1-127	H	L	H	H
32-128	64-256	128-512	H	H	H	H
129-224	257-448	513-896	H	H	L	H
225-255	449-511	897-1023	H	L	L	H
256	512	1024	L	L	L	H

2665 tbi 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I _{OUT}	DC Output Current	50	50	mA

2665 tbi 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
V _{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage Commercial	2.0	—	—	V
V _{IH}	Input High Voltage Military	2.2	—	—	V
V _{IL} ⁽¹⁾	Input Low Voltage Commercial & Military	—	—	0.8	V

2665 tbi 04

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.



DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72105/IDT72115/ IDT72125 Commercial			IDT72105/IDT72115/ IDT72125 Military			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I _{IL} ⁽¹⁾	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	μA
I _{OL} ⁽²⁾	Output Leakage Current	-10	—	10	-10	—	10	μA
V _{OH}	Output Logic "1" Voltage I _{OUT} = -2mA ⁽⁵⁾	2.4	—	—	2.4	—	—	V
V _{OL}	Output Logic "0" Voltage I _{OUT} = 8mA ⁽⁶⁾	—	—	0.4	—	—	0.4	V
I _{CC1} ⁽³⁾	Power Supply Current	—	50	100	—	75	125	mA
I _{CC2} ⁽³⁾	Average Standby Current ($\bar{W} = \overline{RS} = \overline{FL}/DIR = V_{IH}$)(SOCP = V _{IL})	—	4	8	—	4	12	mA
I _{CC3} ^(3,4,7)	Power Down Current	—	1	6	—	1	8	mA

2665 tbi 05

- NOTES:
 1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}.
 2. SOCP = V_{IL}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
 3. I_{CC} measurements are made with outputs open.
 4. $\overline{RS} = \overline{FL}/DIR = \bar{W} = V_{CC} - 0.2V$; SOCP = 0.2V; all other inputs ≥ V_{CC} - 0.2 or ≤ 0.2V.
 5. For SO, I_{OUT} = -4mA.
 6. For SO, I_{OUT} = 16mA.
 7. Measurements are made after reset.

AC ELECTRICAL CHARACTERISTICS

T-46-35

(Commercial: Vcc = 5V±10%, TA = 0°C to +70°C; Military: Vcc = 5V ± 10%, TA = -55°C to +125°C)

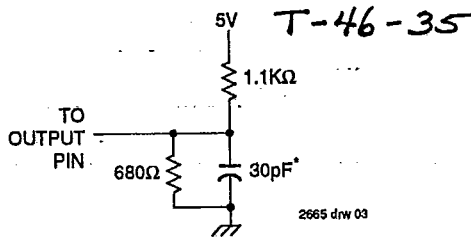
Symbol	Parameter	Figure	COM'L		MILITARY		COM'L AND MILITARY				Unit
			72105L25 72115L25 72125L25		72105L30 72115L30 72125L30		72105L50 72115L50 72125L50		72105L80 72115L80 72125L80		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
ts	Parallel Shift Frequency	—	—	28.5	—	25	—	15	—	10	MHz
tsocp	Serial Shift Frequency	—	—	50	—	45	—	40	—	28	MHz
PARALLEL INPUT TIMINGS											
tWC	Write Cycle Time	2	35	—	40	—	65	—	100	—	ns
tWPW	Write Pulse Width	2	25	—	30	—	50	—	80	—	ns
tWR	Write Recovery Time	2	10	—	10	—	15	—	20	—	ns
tDS	Data Set-up Time	2	12	—	13	—	15	—	15	—	ns
tDH	Data Hold Time	2	0	—	1	—	2	—	5	—	ns
tWEF	Write High to EF High	5, 6	—	35	—	40	—	45	—	50	ns
tWFF	Write Low to FF Low	4, 7	—	35	—	40	—	45	—	50	ns
tWF	Write Low to Transitioning HF, AEF	8	—	35	—	40	—	45	—	50	ns
tWPF	Write Pulse Width After FF High	7	25	—	30	—	50	—	80	—	ns
SERIAL OUTPUT TIMINGS											
tsocp	Serial Clock Cycle Time	3	20	—	22	—	25	—	35	—	ns
tsocw	Serial Clock Width High/Low	3	8	—	9	—	10	—	15	—	ns
tsopd	SOCp Rising Edge to SO Valid Data	3	—	14	—	15	—	15	—	17	ns
tsohz	SOCp Rising Edge to SO at High Z ⁽¹⁾	3	3	14	3	14	3	15	3	17	ns
tsolz	SOCp Rising Edge to SO at Low Z ⁽¹⁾	3	3	14	3	14	3	15	3	17	ns
tsocef	SOCp Rising Edge to EF Low	5, 6	—	35	—	40	—	45	—	50	ns
tsocff	SOCp Rising Edge to FF High	4, 7	—	35	—	40	—	45	—	50	ns
tsocf	SOCp Rising Edge to Transitioning HF, AEF	8	—	35	—	40	—	45	—	50	ns
trefso	SOCp Delay After EF High	6	35	—	40	—	65	—	100	—	ns
RESET TIMINGS											
trsc	Reset Cycle Time	1	35	—	45	—	65	—	100	—	ns
trsp	Reset Pulse Width	1	25	—	30	—	50	—	80	—	ns
trss	Reset Set-up Time	1	25	—	30	—	50	—	80	—	ns
trsr	Reset Recovery Time	1	10	—	15	—	15	—	20	—	ns
EXPANSION MODE TIMINGS											
tfls	FL Set-up Time to RS Rising Edge	9	7	—	7	—	8	—	10	—	ns
tflh	FL Hold Time to RS Rising Edge	9	0	—	1	—	2	—	5	—	ns
tDIRS	DIR Set-up Time to SOCP Rising Edge	9	10	—	11	—	12	—	12	—	ns
tDIRH	DIR Hold Time from SOCP Rising Edge	9	5	—	5	—	5	—	5	—	ns
tsOXD1	SOCp Rising Edge to RSOX Rising Edge	9	—	15	—	17	—	17	—	20	ns
tsOXD2	SOCp Rising Edge to RSOX Falling Edge	9	—	15	—	17	—	17	—	20	ns
tsIXS	RSIX Set-up Time to SOCP Rising Edge	9	5	—	5	—	8	—	15	—	ns
tsIXPW	RSIX Pulse Width	9	10	—	10	—	15	—	20	—	ns

NOTE:
1. Values guaranteed by design.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2665 tbl 07



2665 drw 03

or equivalent circuit

Figure A. Output Load

*Includes jig and scope capacitances.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	12	pF

NOTE: 2665 tbl 08

1. This parameter is sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

Parallel Data Input

The device must be reset before beginning operation so that all flags are set to their initial state. In width or depth expansion the First Load pin (FL) must be programmed to indicate the first device.

The data is written into the FIFO in parallel through the Do-16 input data lines. A write cycle is initiated on the falling edge of the Write (W) signal provided the Full Flag (FF) is not asserted. If the W signal changes from HIGH-to-LOW and the Full Flag (FF) is already set, the write line is internally inhibited from incrementing the write pointer and no write operation occurs.

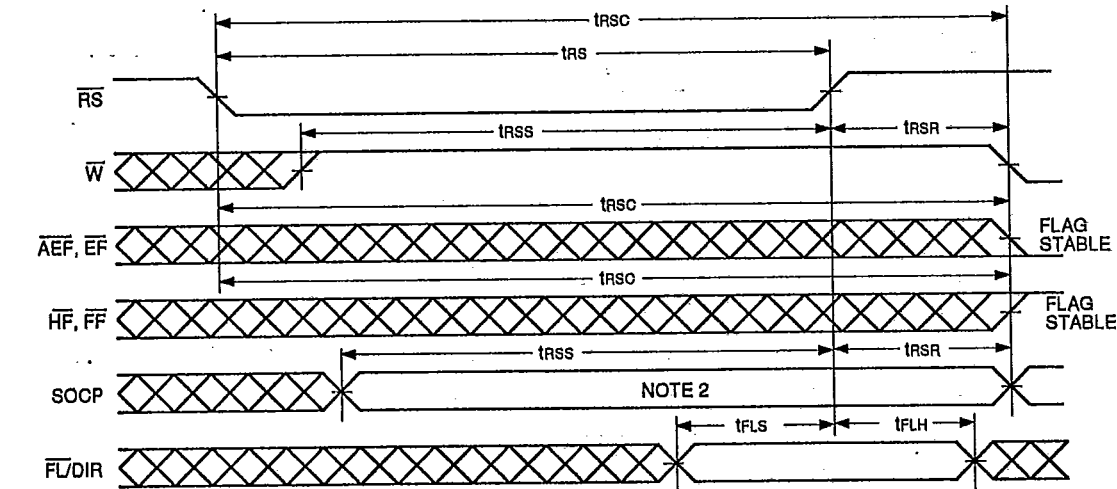
Data set-up and hold times must be met with respect to the rising edge of Write. On the rising edge of W, the write pointer

is incremented. Write operations can occur simultaneously or asynchronously with read operations.

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag (EF) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP.

The serial word is shifted out Least Significant Bit or Most Significant Bit first, depending on the FL/DIR level during operation. A LOW on DIR will cause the Least Significant Bit to be read out first. A HIGH on DIR will cause the Most Significant Bit to be read out first.



2665 drw 04

- NOTES:
1. EF, FF, HF and AEF may change status during Reset, but flags will be valid at trsc.
 2. SOCP should be in the steady low or high during trss. The first low-high (or high-low) transition can begin after trsr.

Figure 1. Reset

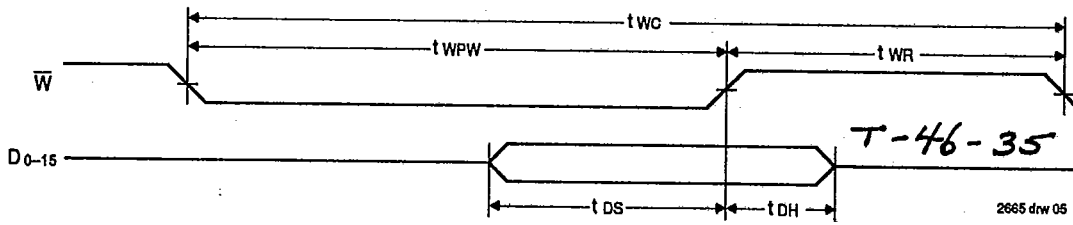
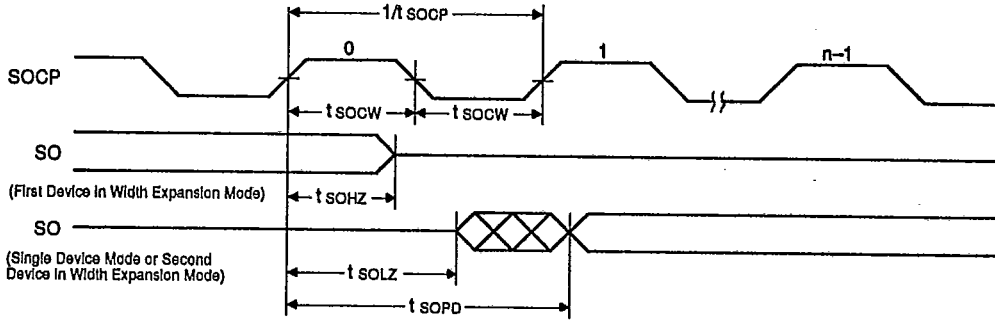


Figure 2. Write Operation



NOTE:

1. In Single Device Mode, \overline{SO} will not tri-state except after reset.

2665 drw 06

Figure 3. Read Operation

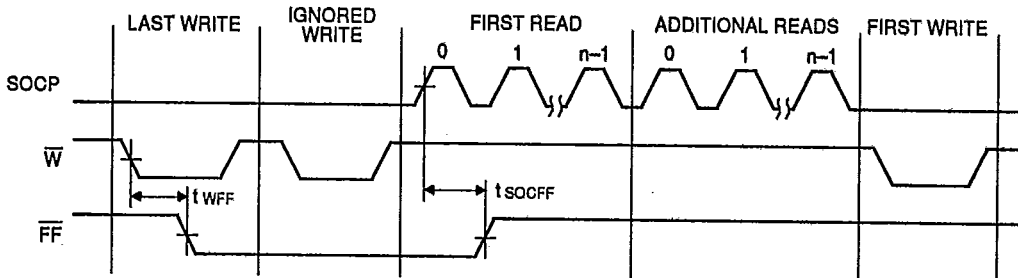
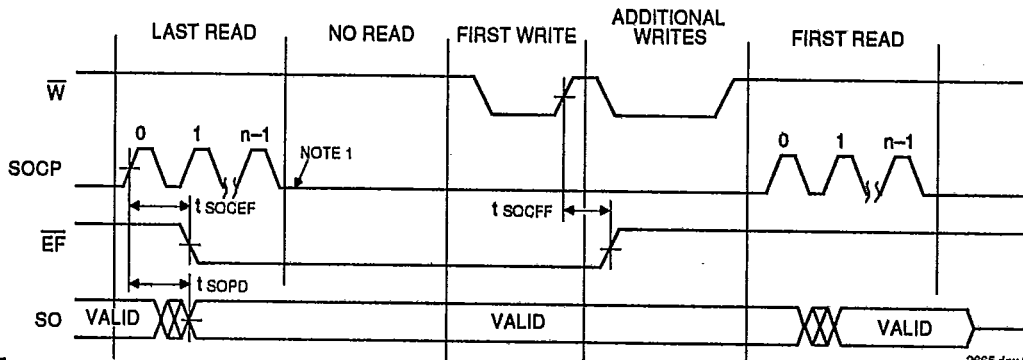


Figure 4. Full Flag from Last Write to First Read

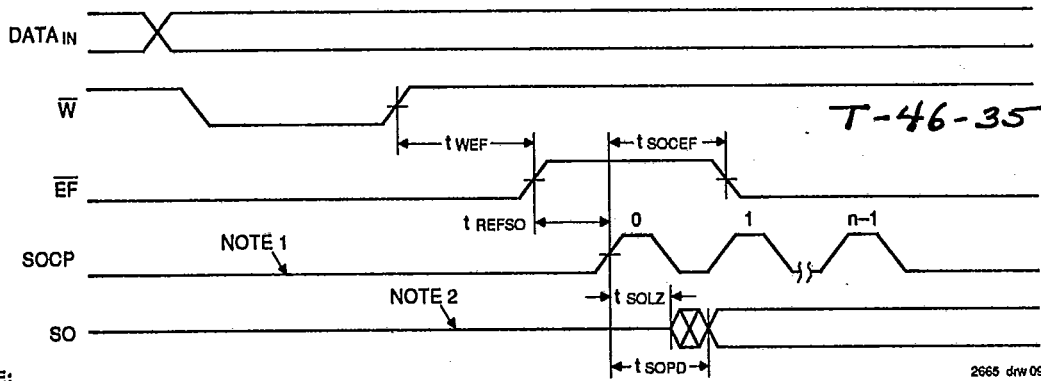


NOTE:

1. \overline{SOCP} should not be clocked until \overline{EF} goes high.

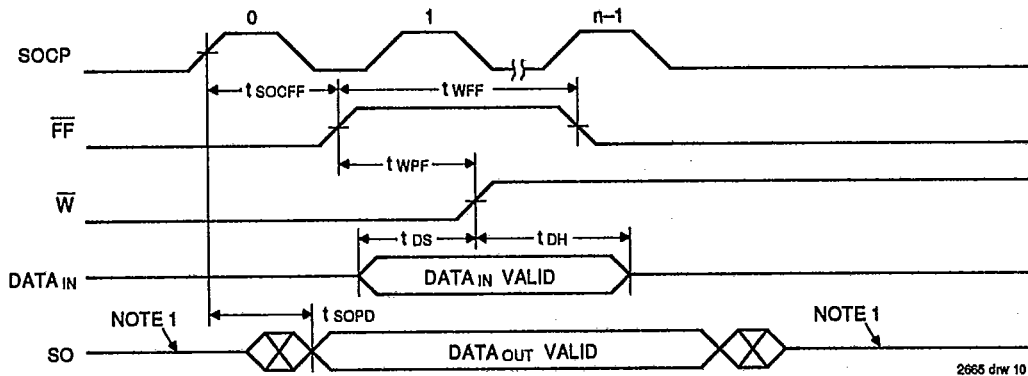
2665 drw 08

Figure 5. Empty Flag from Last Read to First Write



- NOTE:**
1. SOCP should not be clocked until \overline{EF} goes high.
 2. In Single Device Mode, SO will not tri-state except after Reset. It will retain the last valid data.

Figure 6. Empty Boundary Condition Timing



- NOTE:**
1. Single Device Mode will not tri-state but will retain the last valid data.

Figure 7. Full Boundary Condition Timing

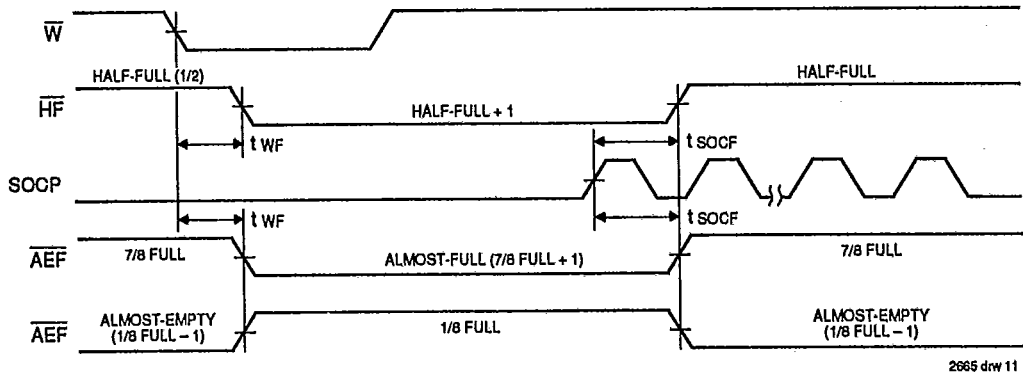


Figure 8. Half-Full, Almost-Full and Almost-Empty Timings



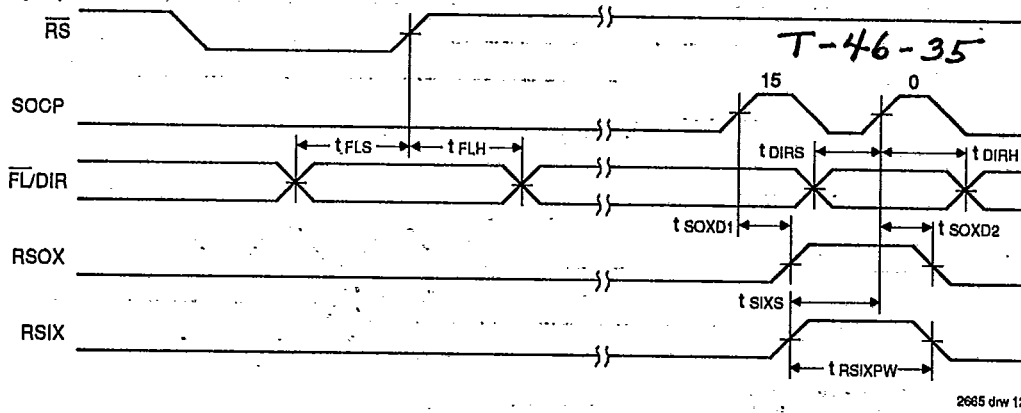


Figure 9. Serial Read Expansion

OPERATING CONFIGURATIONS

Single Device Mode

The device must be reset before beginning operation so that all flags are set to location zero. In the standalone case, the RSIX line is tied HIGH and indicates single device operation to the device. The RSOX/AEF pin defaults to AEF and outputs the Almost-Empty and Almost-Full Flag.

Width Expansion Mode

In the cascaded case, word widths of more than 16 bits can be achieved by using more than one device. By tying the RSOX and RSIX pins together, as shown in Figure 11, and programming which is the Least Significant Device, a cascaded serial word is achieved. The Least Significant Device is programmed by a LOW on the FL/DIR pin during reset. All other devices should be programmed HIGH on the FL/DIR pin at reset.

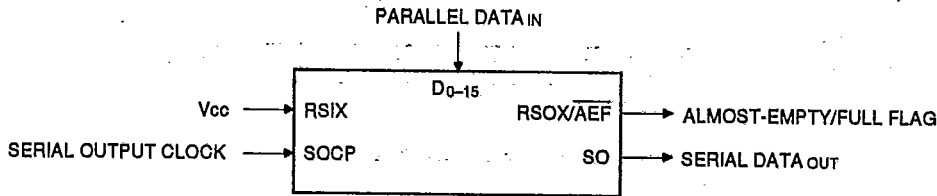


Figure 10. Single Device Configuration

Mode	Inputs			Internal Status		Outputs		
	RS	FL	DIR	Read Pointer	Write Pointer	AEF, EF	FF	HF
Reset	0	X	X	Location Zero	Location Zero	0	1	1
Read/Write	1	X	0,1	Increment ⁽¹⁾	Increment ⁽¹⁾	X	X	X

NOTE:

1. Pointer will increment if appropriate flag is HIGH.

2665 tbl 09

Table 1. Reset and First Load Truth Table—Single Device Configuration

T-46-35

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit bus. NOTE: After reset, the level on the FL/DIR pin decides if the Least Significant or Most Significant Bit is read first out of each device.

The three flag outputs, Empty (EF), Half-Full (HF) and Full (FF), should be taken from the Most Significant Device (in the example, FIFO #2). The Almost-Empty/Almost-Full flag is not available. The RSOX pin is used for expansion.

Depth Expansion (Daisy Chain) Mode

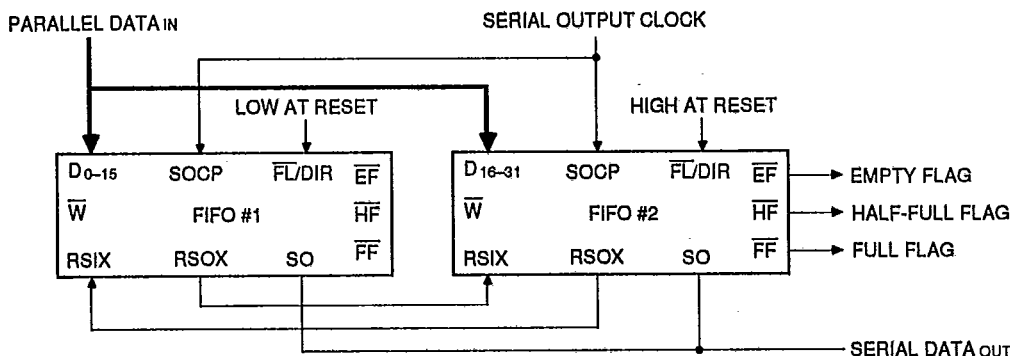


Figure 11. Width Expansion for 32-bit Parallel Data In

2665 drw 14

The IDT72105/15/25 can easily be adapted to applications requiring greater than 1024 words. Figure 12 demonstrates Depth Expansion using three IDT72105/15/25s and an IDT74FCT138 Address Decoder. Any depth can be attained by adding additional devices. The Address Decoder is necessary to determine which FIFO is being written. A word of data must be written sequentially into each FIFO so that the data will be read in the correct sequence. The IDT72105/15/25 operates in the Depth Expansion Mode when the following conditions are met:

1. The first device must be programmed by holding FL LOW at Reset. All other devices must be programmed by holding FL high at reset.
2. The Read Serial Out Expansion pin (RSOX) of each device must be tied to the Read Serial In Expansion pin (RSIX) of the next device (see Figure 12).
3. External logic is needed to generate composite Empty,

Half-Full and Full Flags. This requires the OR-ing of all EF, HF and FF Flags.

4. The Almost-Empty and Almost-Full Flag is not available due to using the RSOX pin for expansion.

Compound Expansion (Daisy Chain) Mode

The IDT72105/15/25 can be expanded in both depth and width as Figure 13 indicates:

1. The RSOX-to-RSIX expansion signals are wrapped around sequentially.
2. The write (W) signal is expanded in width.
3. Flag signals are only taken from the Most Significant Devices.
4. The Least Significant Device in the array must be programmed with a LOW on FL/DIR during reset.



T-46-35

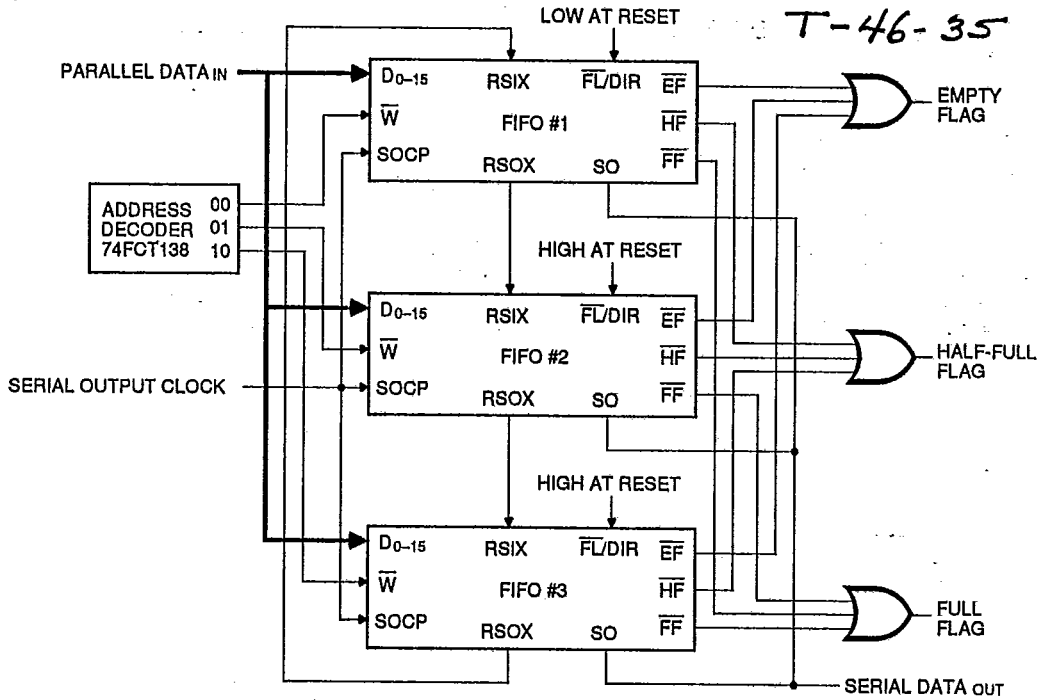


Figure 12. A 3K x 16 Parallel-to-Serial FIFO using the IDT72125

2665 drw 15

Mode	Inputs			Internal Status		Outputs	
	RS	FL	DIR	Read Pointer	Write Pointer	EF	HF, FF
Reset-First Device	0	0	X	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	X	Location Zero	Location Zero	0	1
Read/Write	1	X	0,1	X	X	X	X

NOTE:
1. RS = Reset Input, FL/DIR = First Load/Direction, EF = Empty Flag Output, HF = Half-Full Flag Output, FF = Full Flag Output.

2665 tbl 10

Table 2. Reset and First Load Truth Table-Width/Depth Compound Expansion Mode

T-46-35

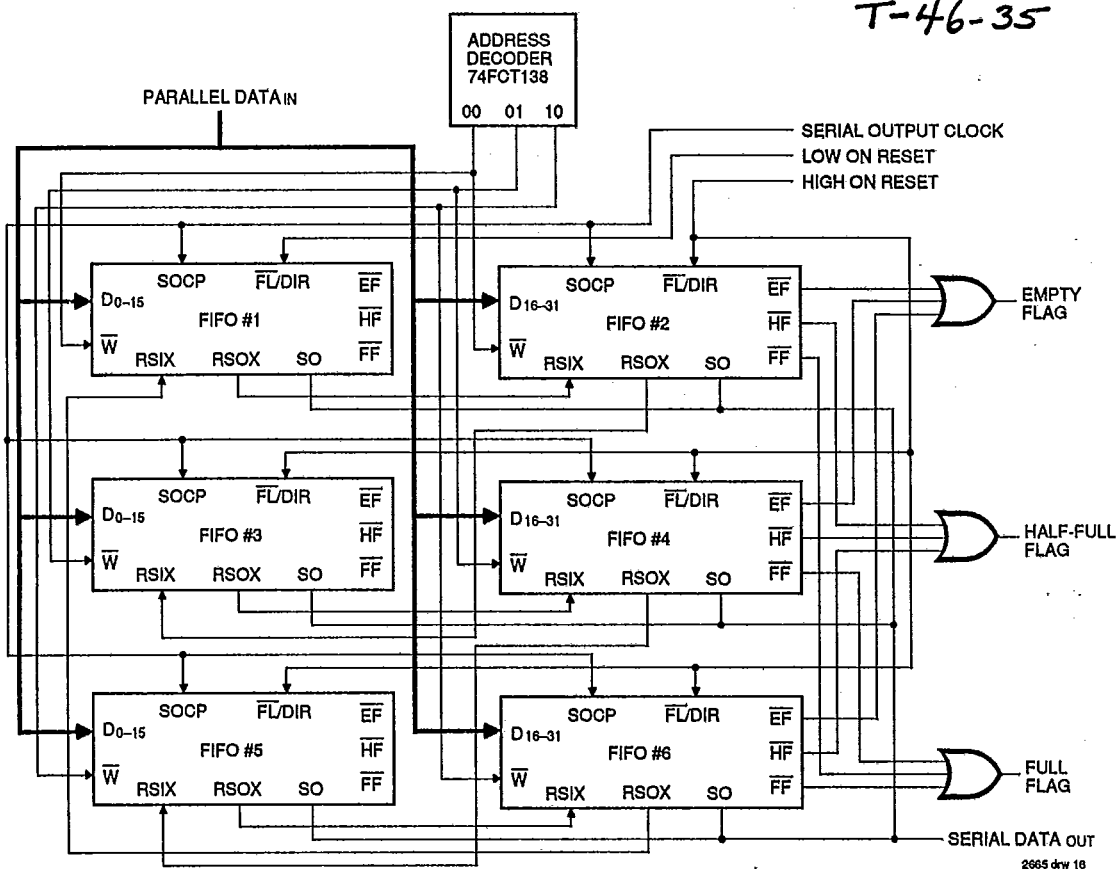


Figure 13. A 3K x 32 Parallel-to-Serial FIFO using the IDT72125

5