

MCM5101•MCM51L01

MAXIMUM RATINGS (Voltages referenced to V_{SS} Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{CC}	-0.5 to +7.0	V
Voltage on Any Pin	V _{in}	-0.3 to V _{CC} +0.3	V
Operating Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC} V _{SS}	4.75 0	5.0 0	5.25 0	V
Logic 1 Voltage, All Inputs	V _{IH}	2.2	—	V _{CC} +0.3	V
Logic 0 Voltage, All Inputs	V _{IL}	-0.3	—	0.65	V

DC CHARACTERISTICS

Characteristic	Symbol	MCM51L01-45 MCM51L01-65			MCM5101-65			MCM5101-80			Unit
		Min	Typ ⁽¹⁾	Max	Min	Typ ⁽¹⁾	Max	Min	Typ ⁽¹⁾	Max	
Input Current	I _{in} ⁽²⁾	—	5.0	—	—	5.0	—	—	5.0	—	nA
Input High Voltage	V _{IH}	2.2	—	V _{CC} +0.3	2.2	—	V _{CC} +0.3	2.2	—	V _{CC} +0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.65	-0.3	—	0.65	-0.3	—	0.65	V
Output High Voltage (I _{OH} = -1.0 mA)	V _{OH}	2.4	—	—	2.4	—	—	2.4	—	—	V
Output Low Voltage (I _{OL} = 2.0 mA)	V _{OL}	—	—	0.4	—	—	0.4	—	—	0.4	V
Output Leakage Current (CE1 = 2.2 V, V _{OL} = 0 V to V _{CC})	I _{LO} ⁽²⁾	—	—	±1.0	—	—	±1.0	—	—	±2.0	μA
Operating Current (V _{in} = V _{CC} , except CE1 ≤ 0.65 V, outputs open)	I _{CC1}	—	9.0	22	—	9.0	22	—	11	25	mA
Operating Current (V _{in} = 2.2 V, Except CE1 ≤ 0.65 V, outputs open)	I _{CC2}	—	13	27	—	13	27	—	15	30	mA
Standby Current (CE2 ≤ 0.2 V, V _{in} = 0 V or V _{CC})	I _{CCL} ⁽²⁾⁽⁴⁾	—	—	10	—	—	200	—	—	500	μA

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V _{in} = 0 V)	C _{in}	4.0	8.0	pF
Output Capacitance (V _{out} = 0 V)	C _{out}	8.0	12.0	pF

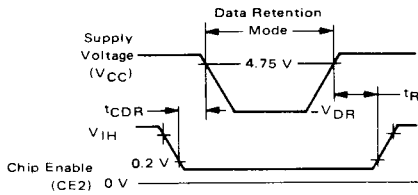
LOW V_{CC} DATA RETENTION CHARACTERISTICS (Excluding MCM5101-80)

Parameter	Test Conditions	Symbol	Min	Typ ⁽¹⁾	Max	Unit	
V _{CC} for Data Retention		V _{DR}	2.0	—	—	V	
MCM51L01-45, -65 Data Retention Current	CE2 ≤ 0.2 V	V _{DR} = 2.0 V	I _{CCDR1}	—	0.14	10	μA
MCM5101-65 Data Retention Current		V _{DR} = 2.0 V	I _{CCDR2}	—	0.70	200	μA
Chip Deselect to Data Retention Time		t _{CDR}	0	—	—	ns	
Operation Recover Time		t _R	t _{RC} ⁽³⁾	—	—	ns	

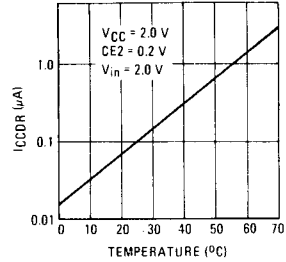
Notes:

- Typical values are T_A = 25°C and nominal supply voltage
- Current through all inputs and outputs included in I_{CCL} measurement
- t_{RC} = Read Cycle Time
- Low current state is for CE2 = 0 only

LOW V_{CC} DATA RETENTION WAVEFORM



TYPICAL ICCDR vs TEMPERATURE



AC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature unless otherwise noted)

Input Pulse Levels..... +0.65 V to 2.2 V Output Load..... 1 TTL Gate and C_L = 100 pF
 Input Rise and Fall Times..... 20 ns Timing Measurement Reference Level..... 1.5 V

READ CYCLE

Parameter	Symbol	MCM51L01-45		MCM51L01-65 MCM5101-65		MCM5101-80		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle	t _{RC}	450	—	650	—	800	—	ns
Access Time	t _A	—	450	—	650	—	800	ns
Chip Enable (CE1) to Output	t _{CO1}	—	400	—	600	—	800	ns
Chip Enable (CE2) to Output	t _{CO2}	—	500	—	700	—	850	ns
Output Disable to Output	t _{OD}	—	250	—	350	—	450	ns
Data Output to High-Z State	t _{DF}	0	130	0	150	0	200	ns
Previous Read Data Valid with Respect to Address Change	t _{OH1}	0	—	0	—	0	—	ns
Previous Read Data Valid with Respect to Chip Enable	t _{OH2}	0	—	0	—	0	—	ns

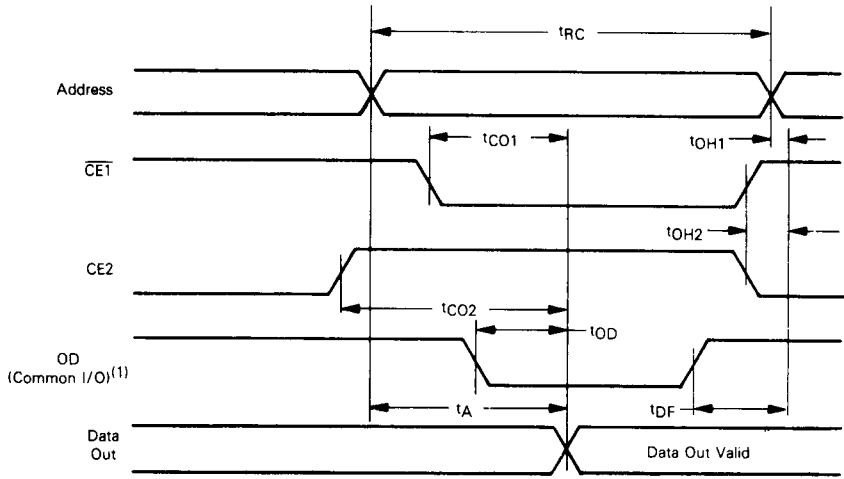
WRITE CYCLE

Parameter	Symbol	MCM51L01-45		MCM51L01-65 MCM5101-65		MCM5101-80		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle	t _{WC}	450	—	650	—	800	—	ns
Write Delay	t _{AW}	130	—	150	—	200	—	ns
Chip Enable (CE1) to Write	t _{CW1}	350	—	550	—	650	—	ns
Chip Enable (CE2) to Write	t _{CW2}	350	—	550	—	650	—	ns
Data Setup	t _{DW}	250	—	400	—	450	—	ns
Data Hold	t _{DH}	50	—	100	—	100	—	ns
Write Pulse	t _{WP}	250	—	400	—	450	—	ns
Write Recovery	t _{WR}	50	—	50	—	100	—	ns
Output Disable Setup	t _{DS}	130	—	150	—	200	—	ns

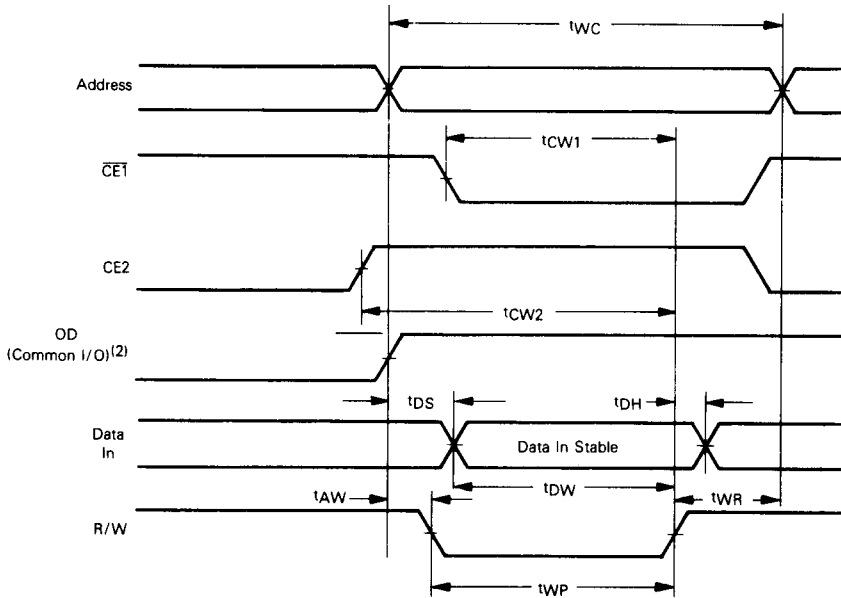
SPAM

SRAM

READ CYCLE TIMING



WRITE CYCLE TIMING



Notes:

1. \overline{OD} may be tied low for separate I/O operation
2. During the write cycle, \overline{OD} is "high" for common I/O and "don't care" for separate I/O operation