P3C218
LATCHED HIGH-SPEED 16Kx16 STATIC RAM

ADVANCE INFORMATION

FEATURES

- Full CMOS Design
- Supports Processor Speeds to 60MHz
- On-Chip Address and Chip Enable Latch
- On-Chip Input Data Latch
- Byte Write Strobe Controls
- Dual Chip Enable for Depth Expansion
- Single 3.3V ±0.3V Power Supply
- Power Down Mode When Deselected
- Output Enable Control
- TTL-Compatible I/O
- Outputs Drive up to 85pF
- 52-Pin PLCC Package

DESCRIPTION

The P3C218 is a 262,144-bit CMOS static RAM organized as 16K words, each 16 bits wide, for cache applications. The SCRAM contains on-chip address and chip enable latches controlled by ALE. A separate control, DL, latches the input data. All latches are transparent when the latch enable controls are HIGH, so the P3C218 can be used as a general-purpose asynchronous 16Kx16 SRAM by connecting ALE and DL to Vcc.

The address and chip enable latches make the P3C218 ideally suited for R3000 cache applications. Four units make up a 64KByte i- (or d-) cache; the two chip enable controls facilitate easy expansion to 128KByte. Individuals byte write operations are possible using $\overline{BWL}$ and $\overline{BWH}$ strobes to qualify the $\overline{WE}$ control, a useful feature for ix86 cache applications.

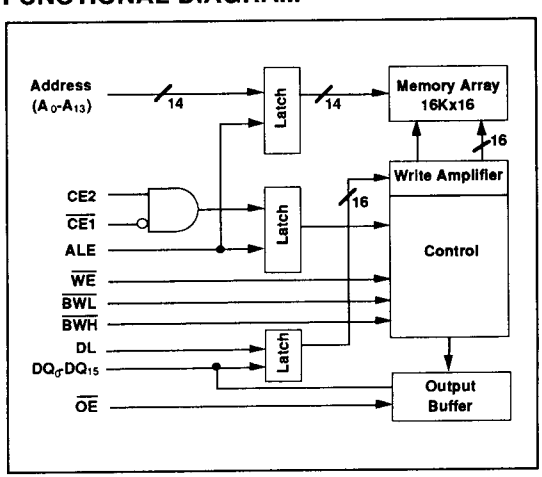
The P3C218 operates from a 3.3V ±0.3V tolerance power supply. Power dissipation is 1.0W (max.) when active, and only 100mW in standby mode. The P3C218 can be used as the secondary cache for low-cost R4000S workstations; 11 units form a 256KByte cache, expandable to 512KBytes with 22 units.

With access times of 15ns, the P3C218 can support all popular microprocessors to 60MHz while keeping chip count and power dissipation low. Outputs can drive up to 85pF loads, so no external buffers are required.

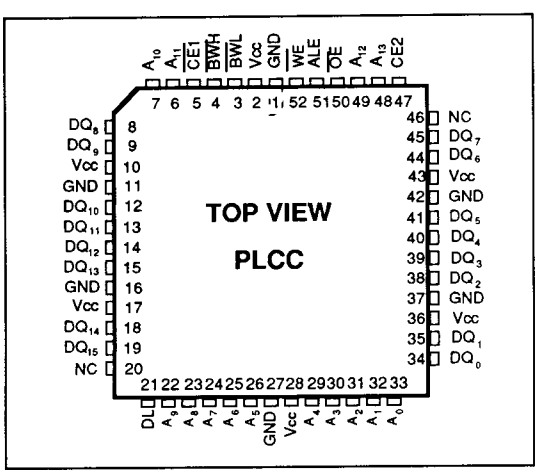
The P3C218 is manufactured using PACE III Technology, and is available in a 52-pin PLCC package, providing excellent board density.

6

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

$\overline{CE}_1$	CE_2	$\overline{BWH}$	$\overline{BWL}$	$\overline{WE}$	$\overline{OE}$	MODE	INPUT/OUTPUT	
							Bits 15–8	Bits 7–0
H	X	X	X	X	X	Deselected	High Z	High Z
X	L	X	X	X	X			
L	H	X	X	H	H	Output Disabled	High Z	High Z
L	H	X	X	H	L	Read Word	Data Out	Data Out
L	H	L	H	L	X	Write High Byte	Data In	High Z
L	H	H	L	L	X	Write Low Byte	High Z	Data In
L	H	L	L	L	X	Write Word	Data In	Data In

APPLICATION EXAMPLE: 3.3V PR4000 Secondary Cache

(256KByte cache in joint instruction-data configuration)