P4C219
HIGH-SPEED SYNCHRONOUS 16Kx16 STATIC RAM

ADVANCE INFORMATION

FEATURES

- Supports Pipelined Systems up to 50 MHz
- Access time of 15ns (max) from Clock to Data Output
- Synchronous Read and Write Operation
- Asynchronous Late Write Abort and Upper and Lower Byte Write Strobes
- Asynchronous Input Data Latch
- Single 5V ±10% Power Supply
- Outputs drive 85pF loads
- TTL Compatible I/O
- 52-pin PLCC Package

DESCRIPTION

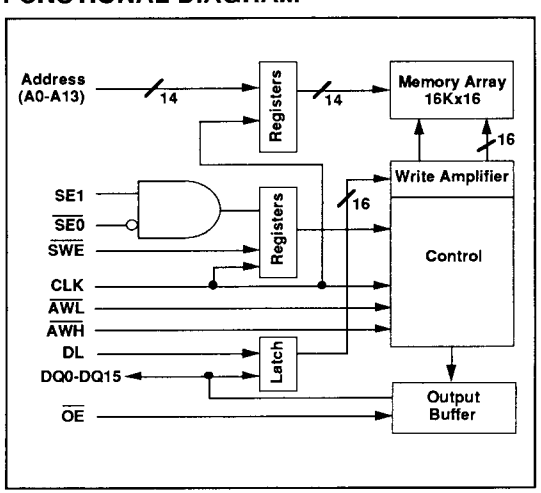
The P4C219 is a 262,144-bit synchronous CMOS static RAM organized as 16,384 words of 16 bits, with address and control input registers, and input data latches, for use in high-performance pipelined systems with wide data paths.

Address (A_{0-13}), chip enables ($\overline{SE0}$, $\overline{SE1}$) and the synchronous write enable ($\overline{SWE}$) inputs are clocked into registers by the upward transition of clock CLK. The asynchronous data latch enable latches input data on its falling edge to guarantee data hold time during write cycles. The synchronous write enable eliminates the need for complex write pulse generation. Byte write strobes ($\overline{AWL}$ and $\overline{AWH}$), which are asynchronous, control writing to the upper and lower bytes individually. The write operation can also be aborted late in the write cycle by raising $\overline{AWL}$ and $\overline{AWH}$ to the HIGH level. The asynchronous output enable $\overline{OE}$ tristates the outputs when HIGH.

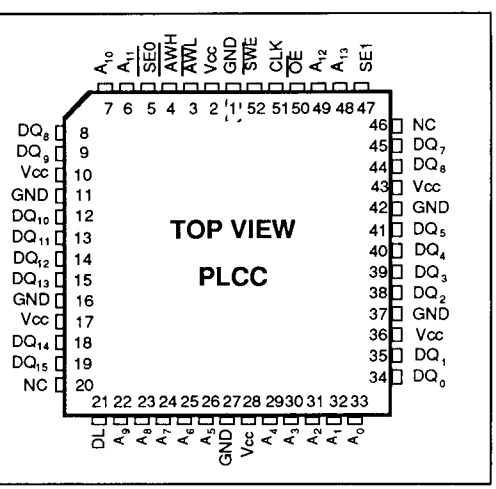
Access times from clock to data output of 15ns are available permitting use of the P4C219 at frequencies as high as 50 MHz. The outputs drive up to 85pF loads without external buffering, and the dual complementary chip enables permit easy depth expansion. Power dissipation is low because of the CMOS design.

The P4C219 is manufactured using PACE III Technology and is available in a 52-pin PLCC package providing excellent board densities.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

$\overline{SE0}$	SE1	$\overline{SWE}$	$\overline{AWL}$	$\overline{AWH}$	$\overline{OE}$	Mode	Data I/O
H	X	X	X	X	X	Deselected Cycle	High Z
X	L	X	X	X	X		High Z
L	H	H	X	X	H	Read Cycle	High Z
L	H	H	X	X	L		Data Out
L	H	L	L	L	X	16-bit Write Cycle	Data In
L	H	L	L	H	X	Low Byte Write Cycle	Data In
L	H	L	H	L	X	High Byte Write Cycle	Data In

Notes:
1. During the write cycle,DL = L latches the input data, DL = H keeps the latch transparent.
2 All appropriate set up and hold time requirements must be met with respect to Clk and DL.