

# BGB203

Bluetooth System-in-a-Package radio with baseband controller

Rev. 1.0 — 2005 July 28

Product Shortform Datasheet

## I. General description

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The BGB203 combines the Bluetooth RF part, protocol stack, Link Controller (LC), Link Manager (LM), and Host Controller Interface (HCI) firmware of the Bluetooth system specification in one SiP with embedded software. Together with an antenna and a reference clock this device forms a complete Bluetooth solution. In most cases this SiP will be attached to a host, for example a GSM baseband controller or a PC processor.

The BGB203 is designed to be used for wireless links operating in the globally available ISM band, between 2402 and 2480 MHz. The radio part is composed of a fully integrated, state-of-the-art near-zero-IF transceiver chip, an antenna filter for out-of-band blocking, a TX/RX switch, TX and RX baluns, and a basic amount of supply decoupling. The device is a “Plug-and-Play” package that needs only 3 additional decoupling components next to an antenna and reference clock for proper operation. Robust design allows for untrimmed components, giving a cost-optimized solution. Demodulation is done in open-loop mode to reduce the effects of reference frequency breakthrough on reception quality. An advanced offset compensation circuit compensates for VCO drift and RF frequency errors during open-loop demodulation, under control by the baseband processor. The circuit is integrated on a laminate substrate. It is connected to the main PCB through a HVQFN48 compatible footprint. The RF port has a normalized 50  $\Omega$  impedance and can be connected directly to an external antenna with a 50  $\Omega$  transmission line. A high-dynamic range RSSI allows near-instantaneous assessment of radio link quality, and is used for output power-control purposes.

The Baseband part and the RF interface of the SiP is designed to operate at 1.8V. The RF part of the SiP is designed to operate from 2.75 V nominal supplies. Separate ground connections are provided for reduced parasitic coupling between different stages of the circuit. There is a basic amount of RF supply decoupling incorporated into the circuit.

The industry standard ARM7TDMI microcontroller with low power consumption is integrated together with a flash memory and a SRAM. There are no provisions for external controllers to directly access on-chip data memory. Communication with an external host, for example a PC, GSM or PDA, is handled via the Host Controller Interface.

Industry standard interfaces such as PCM, UART, USB, and I<sup>2</sup>C are supported by on-chip hardware.



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## 2. Features

### 2.1 General

- Plug-and-play Bluetooth class I System-in-a-Package (SiP)
- Includes all baseband and radio functionality, from HCI up to antenna, needs only external antenna and reference clock.
- Fully compliant to Bluetooth Radio Specification version 1.2.
- Small dimensions (7 × 8 × 1.3 mm typical) in HVQFN like package with full BGB204 HVQFN compatible footprint

### 2.2 Radio hardware

- Fully integrated near-zero-IF receiver with high sensitivity (typical -88 dBm at antenna input)
- Digital demodulator for improved reception quality
- RSSI with high dynamic range
- Programmable output pre-amplifier
- Maximum output power up to +5.5 dBm typical
- Includes high performance blocking filter for co-existence in GSM/DCS/WCDMA applications
- Fully integrated low phase noise VCO operating in the 5 GHz frequency range

### 2.3 Baseband hardware

#### 2.3.1 Hardware features

- Bluetooth burst mode controller with
  - ◆ Ciphering, scrambling, CRC checking/generation, FEC encoding/decoding and data buffering control
  - ◆ Support for 7 slaves and three piconets, support of master-slave switch for new nodes entering the piconet, scatternet support with maximum one slave in master piconet while being slave in another piconet, support for 2 voice channels.
  - ◆ BT 1.2 features :
    - Fast connection,
    - EV3 (HV3+CRC),
    - AFH IP : AFH switch support as master, Channel assesment as master.
- Embedded 32-bit microprocessor consisting of
  - ◆ An ARM7TDMI-S RISC controller featuring low mW/MHz
  - ◆ Integrated Flash memory : 268 kBytes.
  - ◆ SRAM : 40 kBytes.
- Voice processing with
  - ◆ A CVSD, A-law or m-law.
  - ◆ Support of a direct link between PCM interface and BT 1.2 core for the voice channels.
- Power management providing
  - ◆ Power-on reset

- Clocking
  - ◆ Low power clock crystal oscillator for low power mode, accepting 3.2KHz, 32KHz, and 32.768KHz.
  - ◆ Low-power system clock crystal oscillator with programmable on-chip capacitors for frequency adjustment with large pulling range accepting the frequency 12MHz, 13MHz, 24MHz and 26 MHz.
- Microprocessor interfaces
  - ◆ General purpose I/O-pins
  - ◆ I<sup>2</sup>C-bus interface
  - ◆ Multi port PCM interface (linear and log PCM up to 16 bit/sample supported)
  - ◆ UART with hardware handshake and IrDA support
  - ◆ USB interface (vddio2 : 3.3V).
  - ◆ System timers
  - ◆ Watch dog timer
  - ◆ JTAG for ICE and flash memory programming
  - ◆ ETM7 for real time trace.
  - ◆ Patch interface for ROM version emulation.
- Voltage range
  - ◆ Radio 2.75 V
  - ◆ Core 1.8 V
  - ◆ Peripheral pins 1.8 and 3.3 V
- Operating ambient temperature range: -30 to +85 °C

### 2.3.2 Firmware features

- Bluetooth burst mode controller driver
- Link Controller (LC)
- Link Manager (LM)
- Host Controller Interface (HCI)
- Interface drivers
- Voice processing.

## 3. Applications

- Cellphones, smartphones
- Computing applications (PC, notebook, PDA)
- Cellular accessories (Bluetooth headsets)

## 4. Pinning information

### 4.1 Pinning

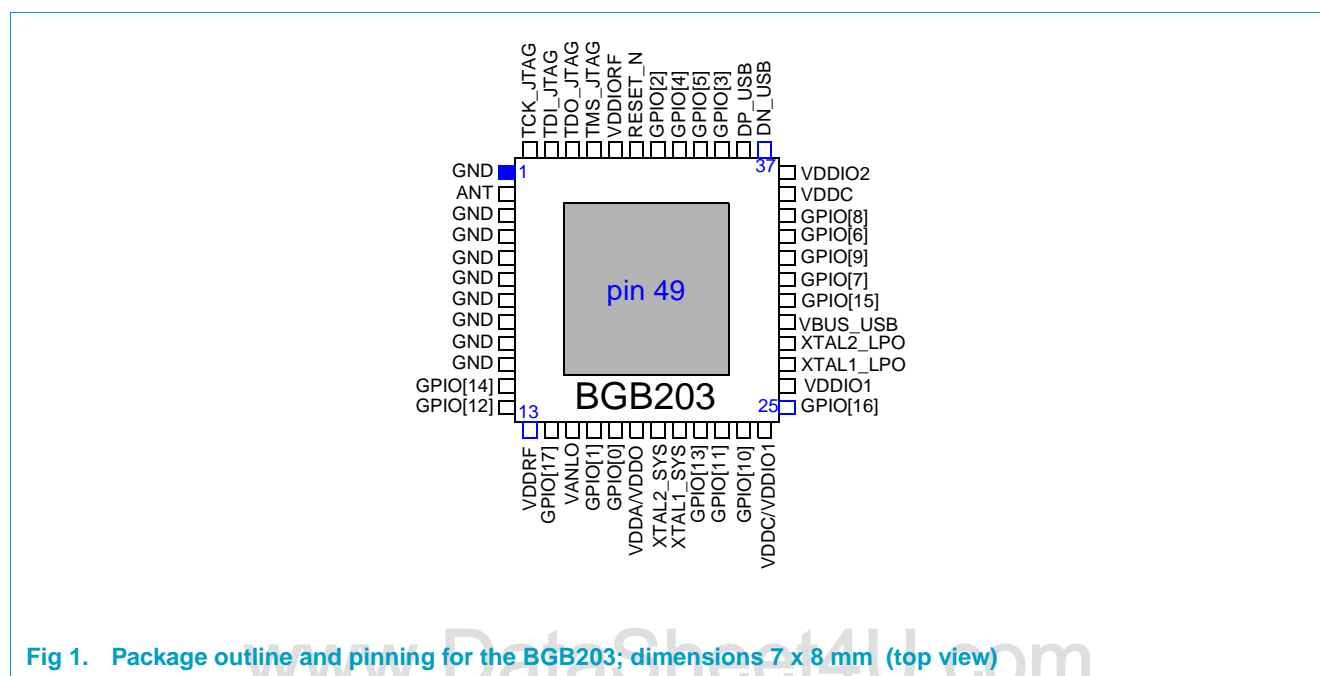


Fig 1. Package outline and pinning for the BGB203; dimensions 7 x 8 mm (top view)

### 4.2 Pin description

Table 1: Pin description BGB203

| Pin nr.               | Pin name          | I/O | Reset state | Supply domain | Description  |
|-----------------------|-------------------|-----|-------------|---------------|--|
| 1,3,4,5,6,7,8,9,10,49 | GND               |     |             |               | Ground   |
| 2                     | ANT               | I/O |             |               | Antenna input / output                                     |
| 11                    | GPIO[14]          | I/O | I pull-up   | Vddio1        | General purpose I/O 14                                     |
| 12                    | GPIO[12]          | I/O | I pull-up   | Vddio1        | General purpose I/O 12                                     |
| 13                    | VDDRF             |     |             |               | Positive radio supply voltage                              |
| 14                    | GPIO[17]          | I/O | I pull-up   | Vddio1        | General purpose I/O 17                                     |
| 15                    | VANLO             | I/O |             | Vdda          | Analog voltage source input                                |
| 16                    | GPIO[1] / I2C_SDA | I/O | I           | Vddio1        | General purpose I/O 1<br>I <sup>2</sup> C bus serial data  |
| 17                    | GPIO[0] / I2C_SCL | I/O | I           | Vddio1        | General purpose I/O 0<br>I <sup>2</sup> C bus serial clock |
| 18                    | VDDA / VDDO       |     |             |               | Positive analogue and oscillator supply voltage            |
| 19                    | XTAL2_SYS         | O   |             | Vddo          | System clock crystal oscillator output                     |
| 20                    | XTAL1_SYS         | I   |             | Vddo          | System clock crystal oscillator input                      |
| 21                    | GPIO[13]          | I/O | I pull-up   | Vddio1        | General purpose I/O 13                                     |
| 22                    | GPIO[11]          | I/O | I pull-up   | Vddio1        | General purpose I/O 11                                     |

Table 1: Pin description BGB203...continued

| Pin nr. | Pin name                                    | I/O | Reset state  | Supply domain | Description  |
|---------|---|-----|--------------|---------------|--|
| 23      | GPIO[10] /<br>SYS_CLK_REQ                   | I/O | O high       | Vddio1        | General purpose I/O 10<br>External system clock request                            |
| 24      | VDDC / VDDIO1                               |     |              |               | Positive core and I/O1 supply voltage  |
| 25      | GPIO[16] /<br>OSC_MODE                      | I/O | I pull-up    | Vddio1        | General purpose I/O 16<br>Oscillator mode selection (GND = slave mode)             |
| 26      | VDDC / VDDIO1                               |     |              |               | Positive core and I/O1 supply voltage  |
| 27      | XTAL1_LPO                                   | I   |              | Vddio1        | Low power clock crystal oscillator input   |
| 28      | XTAL2_LPO                                   | O   |              | Vddio1        | Low power clock crystal oscillator output  |
| 29      | VBUS_USB                                    | I   | I            | Vddio2        | USB Vbus detect  |
| 30      | GPIO[15] /<br>SYS_CLK_REQ                   | I/O | O high       | Vddio2        | General purpose I/O 15<br>External system clock request                            |
| 31      | GPIO[7] /<br>FSC_IP                         | I/O | I pull-up    | Vddio2        | General purpose I/O 7<br>PCM/IOM frame sync  |
| 32      | GPIO[9] /<br>DB_IP                          | I/O | I pull-up    | Vddio2        | General purpose I/O 9<br>Bidirectional PCM/IOM data line B (default: input)        |
| 33      | GPIO[6] /<br>DA_IP                          | I/O | I pull-up    | Vddio2        | General purpose I/O 6<br>Bidirectional PCM/IOM data line A (default: output)       |
| 34      | GPIO[8] /<br>DCLK_IP                        | I/O | I pull-up    | Vddio2        | General purpose I/O 8<br>PCM/IOM data clock  |
| 35      | VDDC  |     |              |               | Positive core supply voltage   |
| 36      | VDDIO2                                      |     |              |               | I/O2 supply voltage  |
| 37      | DN_USB                                      | I/O | I            | Vddio2        | USB data N   |
| 38      | DP_USB                                      | I/O | I            | Vddio2        | USB data P   |
| 39      | GPIO[3] /<br>RTS_UART<br>CONNECT_USB        | I/O | O low        | Vddio2        | General purpose I/O 3<br>UART request-to-send output<br>USB soft connect           |
| 40      | GPIO[5] /<br>RXD_UART                       | I/O | I pull-up    | Vddio2        | General purpose I/O 5<br>UART receive input  |
| 41      | GPIO[4] /<br>TXD_UART                       | I/O | I pull-up    | Vddio2        | General purpose I/O 4<br>UART transmit output                                      |
| 42      | GPIO[2] /<br>CTS_UART<br>LED_USB<br>CLK_EXT | I/O | I pull-up    | Vddio2        | General purpose I/O 2<br>UART clear-to-send input<br>USB LED<br>12MHz Clock output |
| 43      | RESET_N                                     | I   | I pull-up    | Vddio2        | Reset input (active LOW)   |
| 44      | VDDIORF                                     |     |              |               | RF-BB interface supply voltage   |
| 45      | TMS_JTAG                                    | I   | I pull-up    | Vddio1        | JTAG test mode select  |
| 46      | TDO_JTAG                                    | O   | O<br>3-state | Vddio1        | JTAG test data output  |
| 47      | TDI_JTAG                                    | I   | I pull-up    | Vddio1        | JTAG test data input   |
| 48      | TCK_JTAG                                    | I   | I pull-up    | Vddio1        | JTAG test clock  |

## 5. Block Diagram

### 5.1 Full SiP

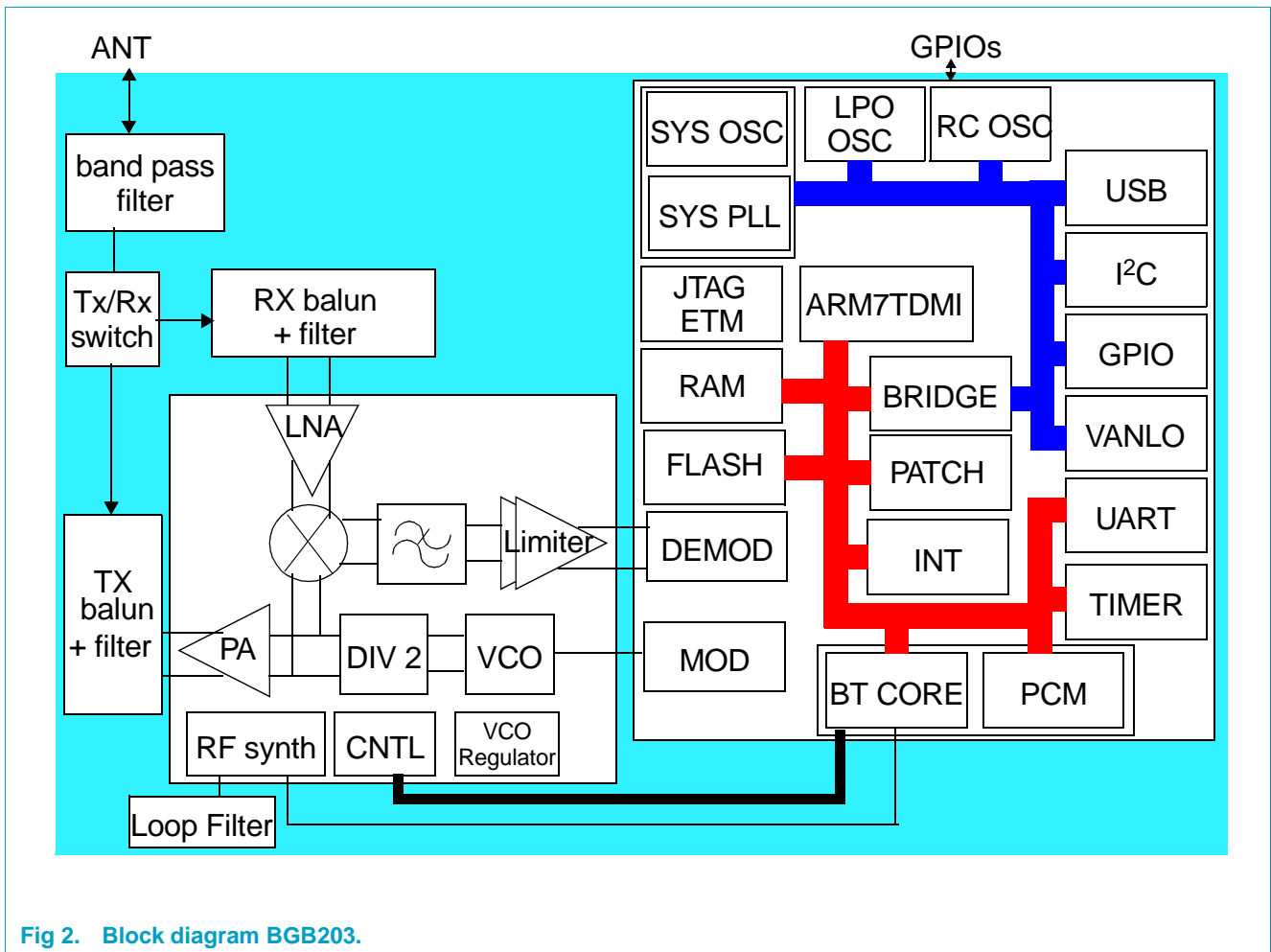


Fig 2. Block diagram BGB203.

## 6. Limiting values

**Table 2: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                                   | Parameter   | Min  | Max                     | Unit |
|--|---|------|-------------------------|------|
| V <sub>DDRF</sub>                        | RF supply voltage   | -0.5 | +3.6                    | V    |
| V <sub>DDIORF</sub>                      | RF BB interface supply voltage  | -0.5 | +2.5                    | V    |
| V <sub>DDC</sub> /<br>V <sub>DDIO1</sub> | Core & I/O 1 supply voltage   | -0.5 | +2.5                    | V    |
| V <sub>DDIO2</sub>                       | I/O 2 supply voltage  | -0.5 | +4.6                    | V    |
| V <sub>DDC</sub>                         | Core supply voltage   | -0.5 | +2.5                    | V    |
| V <sub>DDO</sub> /<br>V <sub>DDA</sub>   | Oscillator & Analog supply voltage  | -0.5 | +2.5                    | V    |
| V <sub>PINIOx</sub>                      | Input voltage on any V <sub>DDIOx</sub> pin with respect to V <sub>SS</sub> | -0.5 | V <sub>DDIOx</sub> +0.5 | V    |
| V <sub>PINIO5V</sub>                     | Input voltage on 5V tolerant pins with respect to V <sub>SS</sub>           | -0.5 | 6.0                     | V    |
| I <sub>I</sub>                           | Input current through any pin (except supply pins)                          |      | 1                       | mA   |
| T <sub>amb</sub>                         | Ambient temperature   | -30  | +85                     | °C   |
| T <sub>stg</sub>                         | Storage temperature   | -40  | +125                    | °C   |

## 7. Electrical characteristics

**Table 3: AC/DC characteristics**

| Symbol                                   | Parameter                          | Conditions            | Min                      | Typ       | Max                      | Unit |
|--|------------------------------------|-----------------------|--------------------------|-----------|--------------------------|------|
| <b>Supplies</b>                          |                                    |                       |                          |           |                          |      |
| V <sub>DDRF</sub>                        | RF supply voltage                  |                       | 2.65                     | 2.75      | 3.3                      | V    |
| V <sub>DDIORF</sub>                      | RF BB interface supply voltage     |                       | 1.65                     | 1.8       | 1.95                     | V    |
| V <sub>DDC</sub> /<br>V <sub>DDIO1</sub> | Core & I/O 1 supply voltage        |                       | 1.65                     | 1.8       | 1.95                     | V    |
| V <sub>DDC</sub>                         | Core supply voltage                |                       | 1.65                     | 1.8       | 1.95                     | V    |
| V <sub>DDIO2</sub>                       | I/O 2 supply voltage               |                       | 1.65                     | 1.8 / 3.3 | 3.6                      | V    |
| V <sub>DDO</sub> / V <sub>DDA</sub>      | Oscillator & Analog supply voltage |                       | 1.65                     | 1.8       | 1.95                     | V    |
| <b>Digital IOs at V<sub>DDIO1</sub></b>  |                                    |                       |                          |           |                          |      |
| V <sub>ih</sub>                          | high level input voltage           |                       | 0.7 × V <sub>DDIO1</sub> | –         | –                        | V    |
| V <sub>il</sub>                          | low level input voltage            |                       | –                        | –         | 0.3 × V <sub>DDIO1</sub> | V    |
| V <sub>hyst</sub>                        | hysteresis voltage                 |                       | 0.3 × V <sub>DDIO1</sub> | –         | –                        | V    |
| V <sub>oh</sub>                          | high level output voltage          | I <sub>oh</sub> = 4mA | V <sub>DDIO1</sub> – 0.4 | –         | –                        | V    |
| V <sub>ol</sub>                          | low level output voltage           | I <sub>ol</sub> = 4mA | –                        | –         | 0.4                      | V    |

Table 3: AC/DC characteristics...continued

| Symbol   | Parameter                                    | Conditions   | Min                      | Typ   | Max                      | Unit |
|--|--|--|--------------------------|-------|--------------------------|------|
| <b>Digital IOs at V<sub>DDIO2</sub></b>                        |  |  |                          |       |                          |      |
| V <sub>ih</sub>  | high level input voltage                     |  | 0.7 × V <sub>DDIO2</sub> | –     | –                        | V    |
| V <sub>il</sub>  | low level input voltage                      |  | –                        | –     | 0.3 × V <sub>DDIO2</sub> | V    |
| V <sub>hyst</sub>  | hysteresis voltage                           |  | 0.3 × V <sub>DDIO2</sub> | –     | –                        | V    |
| V <sub>oh</sub>  | high level output voltage                    | I <sub>oh</sub> = 4mA                                | V <sub>DDIO2</sub> – 0.4 | –     | –                        | V    |
| V <sub>ol</sub>  | low level output voltage                     | I <sub>ol</sub> = 4mA                                | –                        | –     | 0.4                      | V    |
| <b>Power dissipation and current consumption<sup>[1]</sup></b> |  |  |                          |       |                          |      |
| Power  | system off                                   | oscillator is switched off                           | –                        | 15    | –                        | μA   |
|  | active HV3                                   | Master <sup>[2]</sup>                                | –                        | 42.88 | –                        | mW   |
|  | Baseband consumption                         | All VDD=1.8V (except VDDRF)                          |                          | 8.42  |                          | mA   |
|  | Radio  | VDDRF = 2.75V  |                          | 10.08 |                          | mA   |
|  | active HV3                                   | Slave <sup>[2]</sup>                                 | –                        | 54.14 | –                        | mW   |
|  | Baseband consumption                         | All VDD=1.8V (except VDDRF)                          |                          | 8.78  |                          | mA   |
|  | Radio  | VDDRF = 2.75V  |                          | 13.94 |                          | mA   |
|  | active EV5                                   | Master   | –                        | 31.5  | –                        | mW   |
|  | Baseband consumption                         | All VDD=1.8V (except VDDRF)                          |                          | 8.29  |                          | mA   |
|  | Radio  | VDDRF = 2.75V  |                          | 6.03  |                          | mA   |
|  | active EV5                                   | Slave  | –                        | 45.58 | –                        | mW   |
|  | Baseband consumption                         | All VDD=1.8V (except VDDRF)                          |                          | 8.61  |                          | mA   |
|  | Radio  | VDDRF = 2.75V  |                          | 10.94 |                          | mA   |
|  | ACL Sniff, T <sub>sniff</sub> = 1024 (1.28s) | Master   | –                        | 0.28  | –                        | mW   |
|  |  | Slave  | –                        | 0.51  | –                        | mW   |
|  | active ACL                                   | ACL link Master,<br>VDDRF=2.75V,<br>Other VDDs =1.8V | –                        | 14.17 | –                        | mW   |
|  | active ACL                                   | ACL link Slave,<br>VDDRF=2.75V,<br>Other VDDs =1.8V  | –                        | 31.2  | –                        | mW   |
|  | Discoverable mode                            | VDDRF=2.75V,<br>Other VDDs =1.8V                     | –                        | 2.12  | –                        | mW   |

[1] At room temperature

[2] In link NULL sent



## 7.1 Timing characteristics

Table 4: Timing

| Symbol                   | Parameter                     | Conditions     | Min                | Typ  | Max                | Unit    |
|--------------------------|-------------------------------|----------------|--------------------|------|--------------------|---------|
| $t_{osc}$                | Xtal start up time            | BGB203         | 630 <sup>[2]</sup> |      | 682 <sup>[1]</sup> | $\mu$ s |
| $t_{pll}$                | lock time PLL                 | BGB203         |                    |      | 250                | $\mu$ s |
| $t_{osc} + t_{pll}$      | Start up time with PLL locked | BGB203         | 880 <sup>[2]</sup> |      | 932 <sup>[1]</sup> | $\mu$ s |
| $t_{rst}$                | baseband reset delay          |                | –                  | 1024 |                    | cycles  |
| $t_{rc\_delay}$          | Minimal RF reset delay        |                | 200                |      |                    | ns      |
| $t_{long\_reset}$        | typical long reset duration   |                | 7.37               |      | 10                 | s       |
| $t_{VDDx}$               | Minimal VDD rise time         | <sup>[3]</sup> |                    |      | 700                | $\mu$ s |
| $t_{regulator\_respons}$ | Response time to VDDRF supply | <sup>[4]</sup> |                    |      | 20                 | $\mu$ s |

[1] 12 MHz Crystal

[2] 13 MHz Crystal

[3] From POR trip level, the VDD has 700 $\mu$ s to reach VDDA/VDO min@1.65V without going back lower than the trip level.

[4] At the start of a packet the supply current jumps from zero to a level as defined in chapter 19.3. The supply should recover quick enough to keep Vddrf above 2.65V.

## 7.2 Analog characteristics

Table 5: System and Low power oscillators

| Symbol                       | Parameter  | Conditions                   | Min     | Typ      | Max     | Unit |
|------------------------------|--|------------------------------|---------|----------|---------|------|
| <b>System clock input</b>    |  |                              |         |          |         |      |
| $f_{sys\_xtal}$              | system oscillator input frequency                    |                              | 12      | 13 or 24 | 26      | MHz  |
| $V_{swing\_sys}$             | Voltage input swing                                  | slave mode <sup>[5]</sup>    | 300     |          | 1700    | mVpp |
| $V_{DC\_sys}$                | DC input level                                       | slave mode <sup>[1][4]</sup> |         | 950      |         | mV   |
| $V_{DD\_sysIH}$              | High level input voltage on Xtal1_sys pin            | bypass mode                  | 0.8VDDO | -        | VDDO    | V    |
| $V_{DD\_sysIL}$              | Low level input voltage on Xtal1_sys pin             | bypass mode                  | 0       | -        | 0.2VDDO | V    |
| $R_{i\_sys\_xtal}$           | system oscillator input impedance                    | slave mode <sup>[6]</sup>    |         | 63       |         | kohm |
| $C_{i\_sys\_xtal}$           | system oscillator input capacitance to Ground        | oscil. mode <sup>[2]</sup>   |         | 12       |         | pF   |
|                              |  | slave mode <sup>[6]</sup>    |         | 5        |         | pF   |
| $C_{i\_tune\_max}$           | system oscillator programmable capacitance to Ground | <sup>[3]</sup>               |         | 25       |         | pF   |
| $C_{i\_steps}$               | tuning step size for programmable capacitance        |                              |         | 0.1      |         | pF   |
| $g_{m\_sys}$                 | transconductance                                     |                              |         | 21       | 40      | mA/V |
| $r_{out\_sys}$               | output impedance on XTAL2_SYS pin                    |                              |         | 900      |         | ohm  |
| <b>Low power clock input</b> |  |                              |         |          |         |      |
| $f_{lpo\_xtal}$              | low power osc frequency                              | oscil. mode                  |         | 32.768   |         | kHz  |
| $t_{start,avg}$              | LPO average start-up time                            | oscil. mode                  |         | 6        |         | ms   |
| $V_{swing\_lpo}$             | low power input swing                                | slave mode <sup>[7]</sup>    | 320     |          | 1800    | mVpp |
| $V_{DC\_lpo}$                | DC input level                                       | slave mode <sup>[7]</sup>    |         | 320      |         | mV   |
| $V_{DD\_lpoIH}$              | High level input voltage on Xtal1_lpo pin            | bypass mode                  | 0.8VDDO | -        | VDDO    | V    |

Table 5: System and Low power oscillators...continued

| Symbol                 | Parameter                                | Conditions                 | Min | Typ | Max     | Unit |
|------------------------|--|----------------------------|-----|-----|---------|------|
| VDD_IpoIL              | Low level input voltage on Xtal1_Ipo pin | bypass mode                | 0   | -   | 0.2VDDO | V    |
| Ipo_acc                | LPO RC clock accuracy Calibrated         |                            |     | ±50 |         | ppm  |
| V <sub>thl</sub> (POR) | Lower Power-on reset threshold voltage   | measured on pin VDDA/ VDDO | -   | 1.0 | -       | V    |
| V <sub>thu</sub> (POR) | Upper Power-on reset threshold voltage   | measured on pin VDDA/ VDDO | -   | 1.4 | -       | V    |

- [1] For lowest current consumption the input signal must be AC coupled with 100 pF and have a maximum input level of 1700 mV (p-p)
- [2] Excluding on-chip tuning capacitance (RXTUN set to 0x00).
- [3] Typical value for full capacitance. The capacitor array has a tolerance of +/- 30%.
- [4]  $V_{swing\_sys} + 0.5V_{swing\_sys(pp)}$  must be lower than 1.3 V. When the input signal is AC coupled the DC input level is biased at 950 mV.
- [5] For input voltage below 400mV (p-p), an external 120Kohms pull-up resistor between XTAL1\_SYS pin and V<sub>DDIO18</sub> is required.
- [6] In slave mode, the input impedance of the system is modelled as a parallel resistor and capacitor to ground.
- [7] The capacitor for the AC coupling is already integrated in the SIP.

Table 6: Analog AIO

| Symbol               | Parameter                        | Conditions | Min | Typ | Max | Unit |
|----------------------|----------------------------------|------------|-----|-----|-----|------|
| Vref                 | Voltage reference                |            |     | 1.4 |     | V    |
| <b>D/A converter</b> |                                  |            |     |     |     |      |
| Vanlo                | DAC output Voltage               | [1]        | VSS |     | 1.4 | V    |
| Ianlo                | DAC output current               | pull-up    |     | 120 | 150 | µA   |
|                      |                                  | pull-down  |     |     | 3   | mA   |
| DAC resolution       |                                  |            |     |     | 8   | bits |
| ILE                  | DAC Integral Linearity Error     |            | -2  |     | 2   | LSB  |
| DLE                  | DAC Differential Linearity Error |            | -1  |     | 1   | LSB  |
| <b>A/D converter</b> |                                  |            |     |     |     |      |
| Vin                  | Input voltage                    | [2]        | VSS |     | 1.4 | V    |
| Rin                  | Input resistor                   |            |     | 1   |     | Mohm |
| Radc                 | ADC input resistance             |            |     | 1   |     | Mohm |
| Res                  | ADC Resolution                   |            |     |     | 8   | bit  |
| Offset               |                                  |            | -1  |     | +1  | LSB  |
| ILE                  | Integral Linearity Error         |            | -2  |     | +2  | LSB  |
| DLE                  | Differential Linearity Error     |            | 0   |     | +1  | LSB  |

- [1] VANLO pin configured as analog Output.
- [2] VANLO pin configured as analog Input.

Table 7: Analog Bandgap

| Symbol                | Parameter   | Conditions             | Min  | Typ  | Max  | Unit |
|-----------------------|---|------------------------|------|------|------|------|
| V <sub>bg</sub>       | Bandgap Voltage   |                        | 1.15 | 1.21 | 1.25 | V    |
| I <sub>ddBG</sub>     | Bandgap and ABV buffer consumption                      | to be measured on VDDA | 5    | 10   | 20   | μA   |
| I <sub>ddBGOFF</sub>  | Bandgap and ABV buffer consumption with buffer disabled | to be measured on VDDA | -    | -    | 25   | nA   |
| t <sub>BGbuffer</sub> | Bandgap buffer start-up time                            |                        |      | 100  |      | μs   |

### 7.3 Radio characteristics

Table 8: Radio [5]

| Symbol                         | Parameter                               | Conditions  | Min  | Typ  | Max  | Unit |
|--------------------------------|---|---|------|------|------|------|
| <b>Power consumption</b>       |   |   |      |      |      |      |
| I <sub>DDRF</sub>              | RF supply current                       | RX guard space                                      | –    | 18   | –    | mA   |
|                                |   | RX (PLL off)  | –    | 33   | 46   | mA   |
|                                |   | TX guard space                                      | –    | 18   | –    | mA   |
|                                |   | TX (PLL off) [4]                                    | –    | 29   | 35   | mA   |
|                                |   | power-down mode                                     | –    | 1    | 2.5  | μA   |
| <b>Frequency selection</b>     |   |   |      |      |      |      |
| Δf <sub>1 slot</sub>           | carrier drift                           | over 1 TX slot [2]                                  | -25  | 0    | 25   | kHz  |
| Δf <sub>3, 5 slots</sub>       |   | over 3, 5 TX slots (DM3, DH3, DM5, DH5 packets) [2] | -40  | 0    | 40   | kHz  |
| ICFT                           | initial carrier frequency tolerance     | [2]   | -75  | 0    | 75   | kHz  |
| <b>Transmitter performance</b> |   |   |      |      |      |      |
| f <sub>RF</sub>                | RF frequency                            | over full temperature and supply range              | 2402 | –    | 2480 | MHz  |
| P <sub>o</sub>                 | Output power                            | max. PA_CNTRL=7                                     | 0    | +5.5 |      | dBm  |
|                                |   | nom. PA_CNTRL=4                                     | -5   | 0    | +4   | dBm  |
|                                |   | min. PA_CNTRL=0                                     | –    | -11  |      | dBm  |
|                                |   | [2]   |      |      |      |      |
|                                | step size                               | [7]   |      | 3    |      | dBm  |
| P <sub>o 1 MHz</sub>           | adjacent channel output power           | at 2 MHz offset [2] [3]                             |      | -45  | -20  | dBm  |
|                                |   | at 3MHz offset and more [2] [3]                     |      | -50  | -40  |      |
| f <sub>dev</sub>               | frequency deviation 1111000 bit pattern | [2] [3]   | 140  | –    | 175  | kHz  |
| BW <sub>20dB</sub>             | 20 dB bandwidth                         | [2] [3]   | –    | 0.7  | 1    | MHz  |
| VSWR                           | voltage standing wave ratio             | normalized to Z <sub>0</sub> 50 Ω                   | –    | 2    | –    |      |

Table 8: Radio [5]...continued

| Symbol               | Parameter                                  | Conditions  | Min  | Typ  | Max  | Unit |
|----------------------|--|---|------|------|------|------|
| Spurious             |  |   |      |      |      |      |
|                      | out of band spurious emissions (conducted) | 30 MHz to 1 GHz [2]                               | -    |      | -36  | dBm  |
|                      |  | 1 GHz to 12.75 GHz [2]                            | -    |      | -30  | dBm  |
|                      |  | 1.8 GHz to 1.9 GHz [2]                            | -    |      | -47  | dBm  |
|                      |  | 5.15 GHz to 5.3 GHz [2]                           | -    |      | -47  | dBm  |
| Receiver performance |  |   |      |      |      |      |
| SENS                 | sensitivity for BER = 0.1 %                | without carrier offset / hopping off              | -76  | -88  | -    | dBm  |
|                      |  | with dirty transmitter as specified in note 3 [2] | -76  | -80  | -    | dBm  |
|                      | sensitivity for PER = 0.5 %                | without carrier offset / hopping off              | -76  | -80  | -    | dBm  |
| $P_{i\max}$          | maximum input power in one channel         | BER < 0.1 % [2]                                   | -20  | -10  | -    | dBm  |
| VSWR                 | voltage standing wave ratio                | normalized to $Z_o = 50$                          | -    | 1.5  | -    |      |
| $f_{RF}$             | RF input frequency                         | [2]   | 2402 | -    | 2481 | MHz  |
| C/I                  | Co-channel                                 |   | +11  | +9.5 |      | dBc  |
|                      |  | N+/-1   | 0    | -10  |      | dBc  |
|                      |  | N-2   | -30  | -38  |      | dBc  |
|                      |  | N+2   | -9   | -30  | -    | dBc  |
|                      |  | N+3   | -20  | -45  | -    | dBc  |
|                      |  | N-3 and lower , N+4 and beyond                    | -40  | -48  | -    | dBc  |
|                      |  |   |      |      |      |      |
| OBB                  | out of band blocking                       |   |      |      |      |      |

[1] The actual VCO frequency is twice the programmed frequency. It is divided by 2 internally.

[2] Over full temperature and supply voltage range.

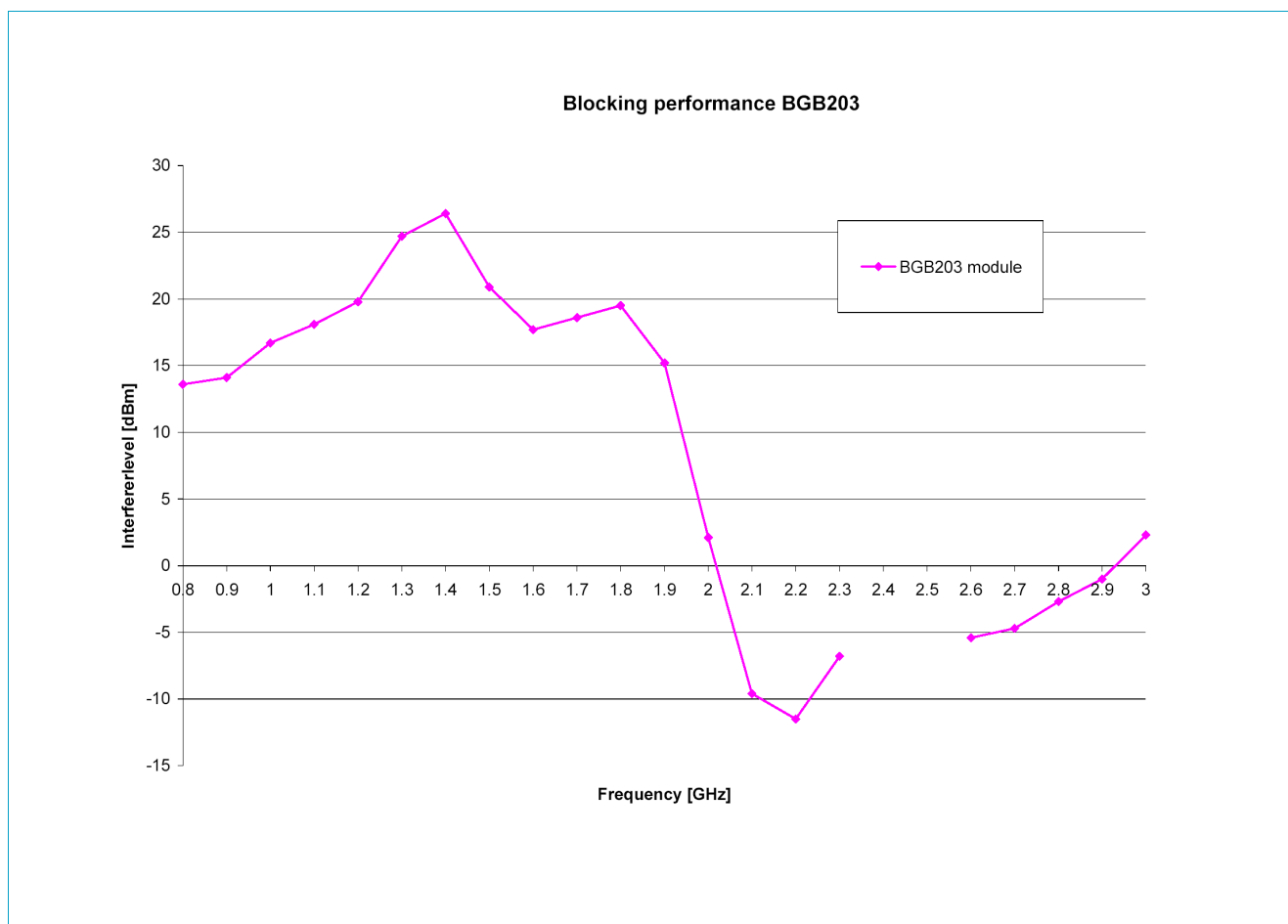
[3] Bluetooth test specification: RF, 2004-11-4, RFTS/2.0.E.2

[4] PA\_CNTRL = 0x04

[5] According to 1.2 Bluetooth specification.

[6] Measured in 100KHz bandwidth. Referred to wanted channel.

[7] PA\_CNTRL <= 0x05



## 8. ESD precautions

Inputs and outputs are protected against electrostatic discharge (ESD) during handling and mounting. A human-body model (HBM) and a machine model (MM) are used for ESD susceptibility testing. All pins withstands the following threshold voltages:

**Table 9: ESD threshold voltages**

| Parameter             | Method                             | Value    | Class |
|-----------------------|------------------------------------|----------|-------|
| ESD threshold voltage | HBM (JESD22-A114-B) <sup>[1]</sup> | 3500 (V) | 2     |
|                       | MM (JESD22-A115-A) <sup>[1]</sup>  | 300 (V)  | 2     |
|                       | HBM (JESD22-A114-B) <sup>[2]</sup> | 250 (V)  | 1A    |
|                       | MM (JESD22-A115-A) <sup>[2]</sup>  | 200 (V)  | 2     |

[1] for all pins except pin 2.

[2] for pin 2.

## 9. Thermal characteristics

Table 10: ESD threshold voltages

| Parameter     | Method                                      | Value | Unit |
|---------------|---|-------|------|
| $R_{th\ j-a}$ | Thermal resistance from junction to ambient | 30    | K/W  |

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### 10. Package outline

HLLGA48: plastic thermal enhanced low profile land grid array package; 48 lands; body 8 x 7 x 1.4 mm

SOT863-1

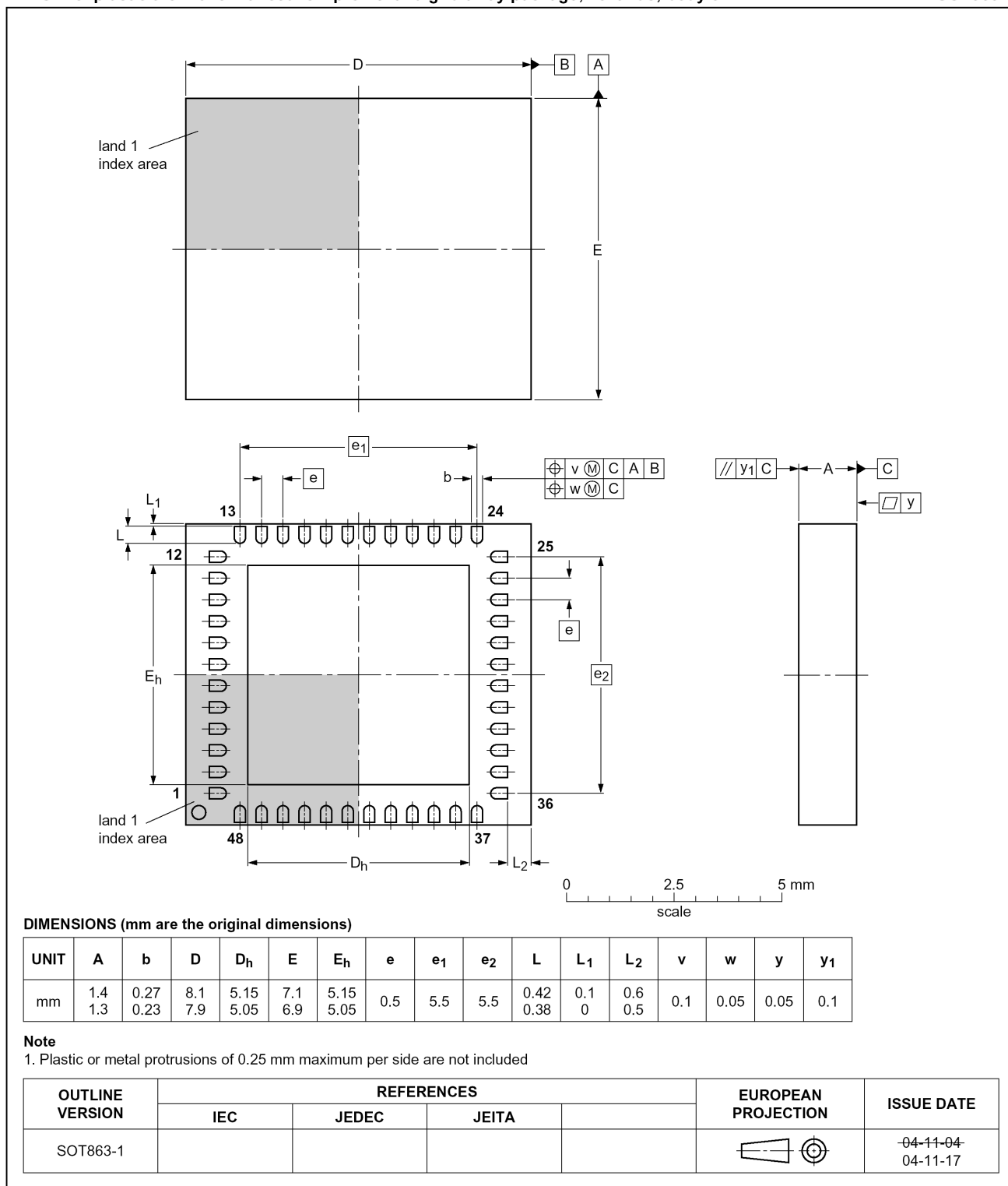


Fig 3. Package outline.

### 10.1 PCB footprint outline

Footprint layout BGB203/204 Non Solder Mask Defined (nsmd), copper defined

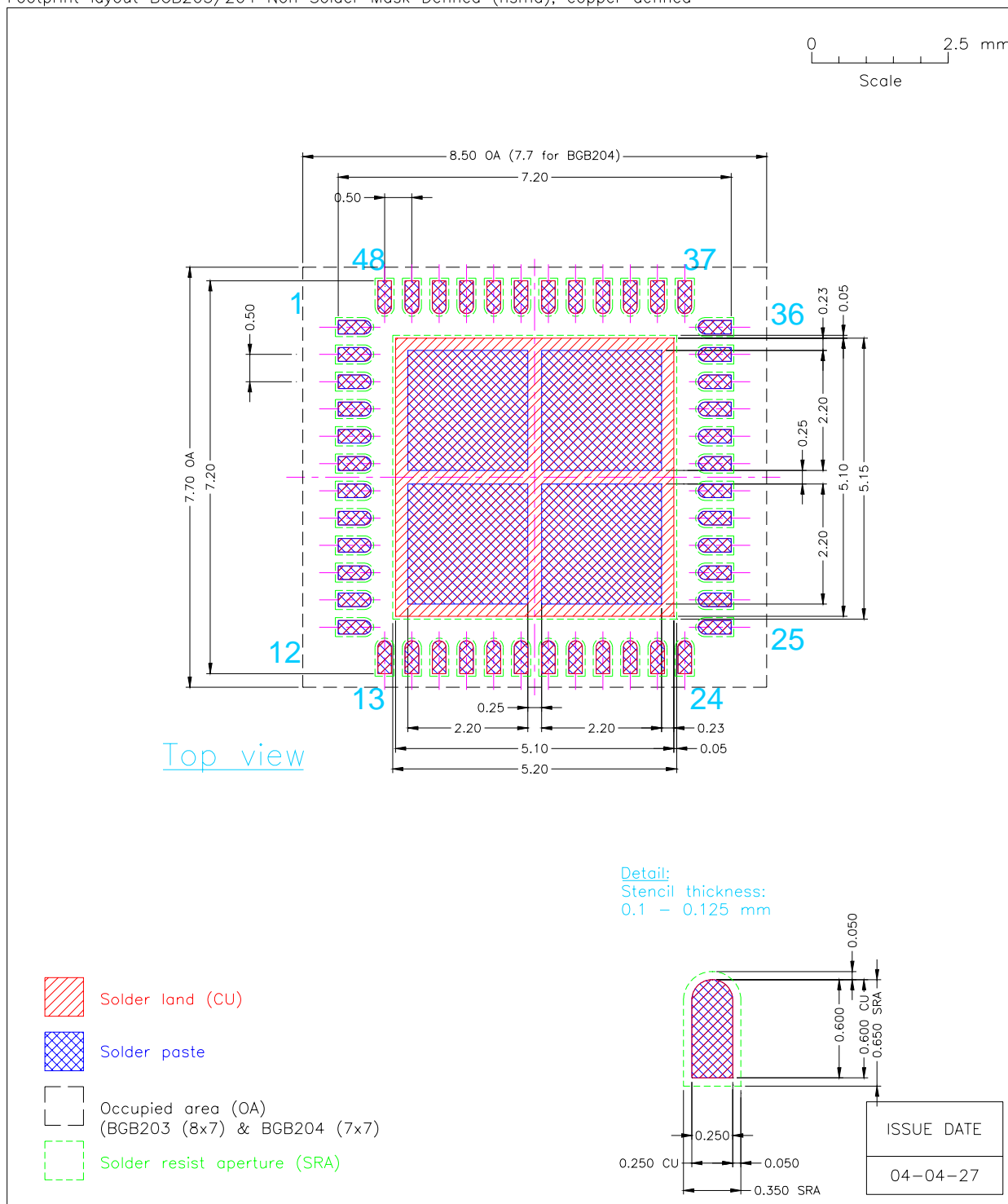


Fig 4. PCB Footprint outline, metal defined.



## 11. Soldering

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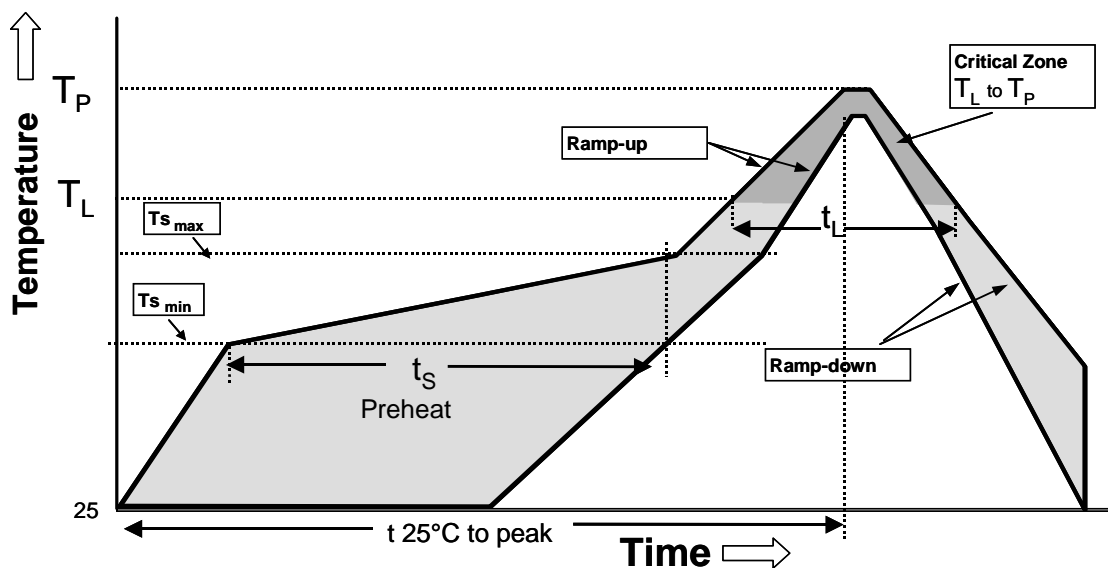
### 11.1 Solder paste

Standard (No-clean) Sn/Pb (63%/37%) or Pb-free solder pastes should be used for soldering the package. Solder pastes should be selected based on their printing and reflow behavior. For Pb-free solder paste it is recommended to use “SAC” type solder paste (e.g. SnAg3.8Cu0.7) with melting point of 217°C.

### Reflow profile

Industrial convection reflow oven should be used to mount the packages. The profile depends on the printed circuit board and other components that are used in the customer application. For maximum peak temperature JEDEC specification should be followed.

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Following reflow profile and constraints are recommended for eutectic Sn/Pb and Pb-free reflow solders.

|   | Eutectic Sn/Pb   | Pb-free  |
|---|--|--|
| Average Ramp-Up Rate ( $T_{s_{max}}$ to $T_P$ )       | 2 °C/second max.   | 2 °C/second max *.   |
| Preheat   |  |  |
| – Temperature Min ( $T_{s_{min}}$ )                   | 100 °C   | 150 °C   |
| – Temperature Max ( $T_{s_{max}}$ )                   | 150 °C   | 200 °C   |
| – Time ( $t_{s_{min}}$ to $t_{s_{max}}$ )             | 60-120 seconds   | 75-90 seconds ( $\leq 0.75^\circ\text{C/second}$ )         |
| Time maintained above:                                |  |  |
| – Temperature ( $T_L$ )                               | 183 °C   | 217 °C   |
| – Time ( $t_L$ )                                      | 60-90 seconds  | 70-90 seconds  |
| Max. Peak Temperature ( $T_P$ )                       | 240 +0/-5 °C   | 260 +0 °C  |
| Time within 5 °C of actual Peak Temperature ( $t_p$ ) | 10-30 seconds  | 20-30 seconds  |
| Ramp-Down Rate  | > 180 °C: 2 °C/second max.<br>< 180 °C: 6 °C/second max. | > 180 °C: 2 °C/second max *.<br>< 180 °C: 6 °C/second max. |
| Minimum peak temperature ( $T_{P_{min}}$ )            | 205 °C   | 230 °C   |
| Time 25°C to $T_P$ $T_P$ $T_P$ $T_P$                  | 4-5 minutes  | 4-5 minutes  |

\*Ramp-up and -down is lower than specified in JEDEC JSTD-020C.

Fig 5. Recommended reflow temperature profile.

## 11.2 Moisture Sensitivity Level

The following moisture sensitivity levels (MSL) is applicable for SOT863 HLLGA48 package.

|                                 |      |
|---------------------------------|------|
| Maximum peak temperature (Tmax) | MSL  |
| 240°C                           | MSL3 |
| 250°C                           | MSL3 |
| 260°C                           | MSL3 |

## 11.3 Rework

If rework is needed, then the packages can be removed or reworked using a “BGA” repair station.

The rework process involves the following steps:

- 1) Component Removal
- 2) Site Redress
- 3) Solder Paste Application,
- 4) Component Placement, and
- 5) Component Attachment.

These steps are discussed the following in more detail

- 1) Component removal

The first step in removal of component is the reflow of solder joints. It is recommended to preheat the PCB to 150C using a bottom heater. Heating of the top side of the component should be done using hot air while a special nozzle can be used for this purpose. Excessive airflow should also be avoided since this may cause shifting of adjacent components. Once the joints have reflowed, the vacuum lift-off can start. Because of their small size the vacuum pressure should be kept below 15 inch of Hg. This will prevent damage to the PCB solderland (“pad lift”). The temperature of the package should not exceed 260 °C during this rework process since damage can occur to either the package or the PCB. The temperature profile depends on the customer application.

- 2) Site Redress

After the component is removed, the PCB solderland needs to be cleaned properly. It is best to use a combination of a blade-style conductive tool and desoldering braid. The width of the blade should be matched to the maximum width of the footprint and the blade temperature should be low enough not to cause any damage to the circuit board. Flux residues on the PCB can be removed using IsoPropyl Alcohol (IPA).

- 3) Solder Paste Application

It is recommended to re-apply solder by dispensing or stencil printing. The amount of solder applied on the terminals should be in the order of 0.08 mg. In case of dispensing, a gage 27 (0.2 mm opening) needle (e.g. white EFD needle) should be used with 0.3s-0.4s shot at 4 bar. For stencil printing a mini stencil of 0.1 mm thickness can be used if application allows room for it.

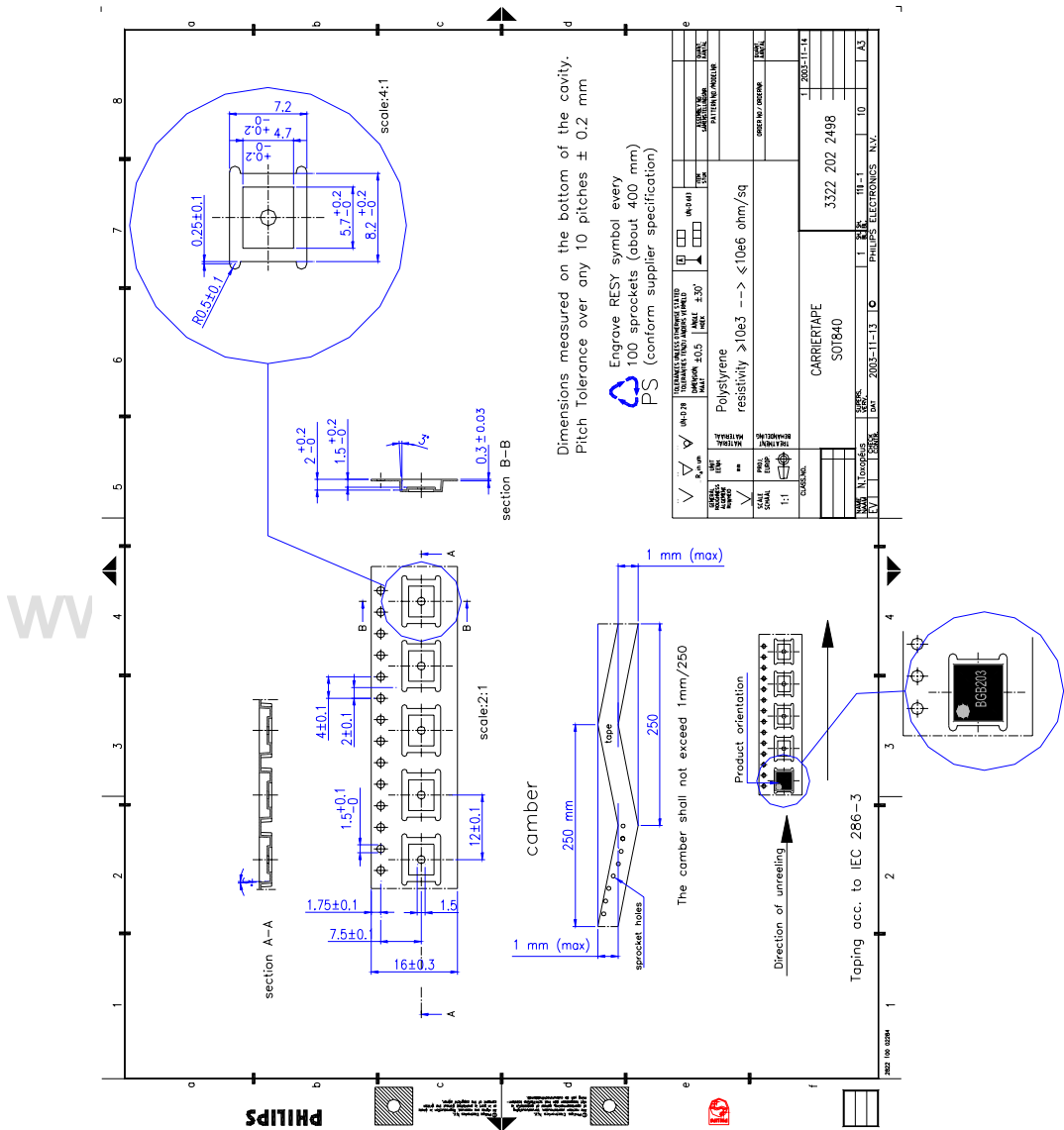
4) A BGA repair station has a vacuum pick up tool and usually some component alignment possibilities. A split-beam optical system should be used to align the component on the solder lands. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes. Manual placement is not recommended, although the package allows 0.1-0.15 mm misplacement.

5) For re-soldering of the newly placed component the same profile of bottom and top heating should be applied as described in the step 1). The moisture sensitivity levels are determined following JEDEC JSTD-020C. The datasheet of the device states the actual MSL witch might deviate from this guideline.

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## 12. Packing

BGB203 is available in Tape & Reel with standard packing quantity (PQP) of 2500 pcs. BGB203 packing is in drypack format since the component has MSL3, which gives it a floorlife of 72hrs outside drypack.



### 13. Revision history

Table 11: Revision history

| Rev | Date     | CPCN | Description                 |
|-----|----------|------|-----------------------------|
| 1.0 | 20050728 |      | Product Shortform Datasheet |

### 14. Trademarks

**GoodLink** — is a trademark of Koninklijke Philips Electronics N.V.

**BlueTooth**---- a trademark of SIG

### 15. Ordering information

Table 12: Ordering information

| Type number | Package   |  |         |
|-------------|-----------|--|---------|
|             | Name      | Description  | Version |
| BGB203/1    | SOT 863-1 | Bluetooth radio module with baseband controller; 12 nc: 9340 592 93518 | S01     |

### 16. Data sheet status

| Data sheet status | Product status | Definitions  |
|-------------------|----------------|--|
| Objective data    | Development    | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.  |
| Preliminary data  | Qualification  | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.                                     |
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