Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **2.75W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Pin layout compatible with CYM1611 and CYM1622**
- **Low profile**
  - **Max. height of .54 in.**
- **Small PCB footprint**
  - **0.7 sq. in.**

Functional Description

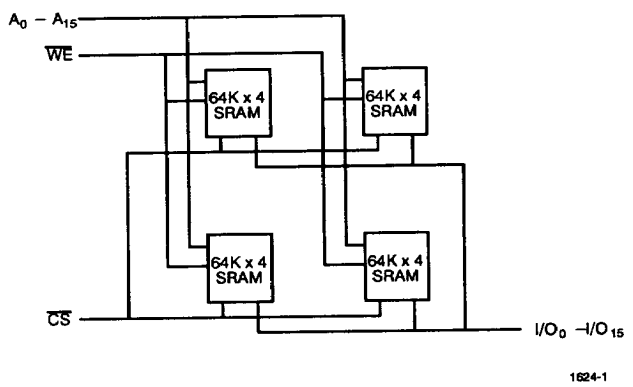
The CYM1624 is a very high performance 1-megabit static RAM module organized as 64K words by 16 bits. This module is constructed using four 64K x 4 static RAMs in SOJ packages mounted on an epoxy laminate board with pins. The pinout of this module is compatible with two other Cypress modules (CYM1611 and CYM1622) to maximize system flexibility.

Writing to the module is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the sixteen input/output pins (I/O_0 through I/O_{15}) of the device is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{15}) will appear on the appropriate data input/output pins (I/O_0 through I/O_{15}).

The data input/output pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH or when write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



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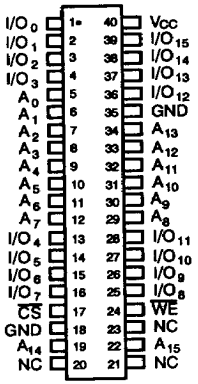
Pin Configuration

Plastic VDIP



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Selection Guide

	1624-25	1624-35	1624-45
Maximum Access Time (ns)	25	35	45
Maximum Operating Current (mA)	500	500	500
Maximum Standby Current (mA)	160	160	160

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −45°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1624		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−20	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		500	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		160	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		80	mA

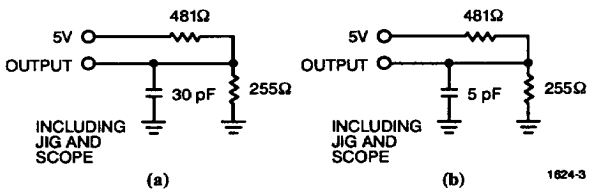
Capacitance[2]

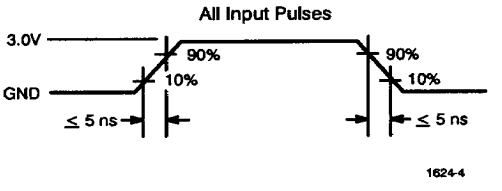
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		15	pF

Notes:

1. $V_{IL(MIN)}$ = −3.0V for pulse widths less than 20ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range[3]

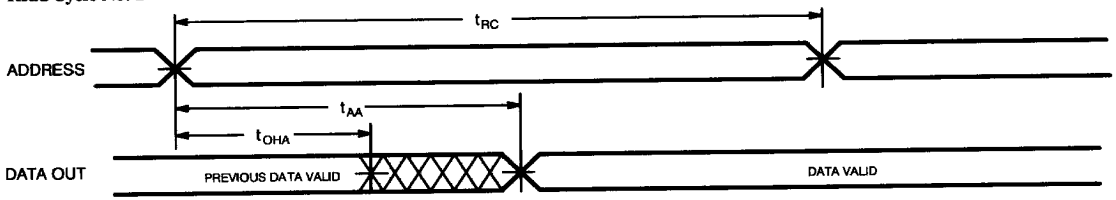
Parameters	Description	1624-25		1624-35		1624-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [4]		15		25		30	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		30		35		ns
t_{AW}	Address Set-Up to Write End	20		30		35		ns
t_{HA}	Address Hold from Write End	3		5		5		ns
t_{SA}	Address Set-Up from Write Start	2		3		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		35		ns
t_{SD}	Data Set-Up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	3		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [4]	0	15	0	15	0	15	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured +500 mV from steady state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS} = V_{IL}$.
8. Address valid prior to or coincident with $\overline{CS}$ transition low.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

Read Cycle No. 1 [6, 7]



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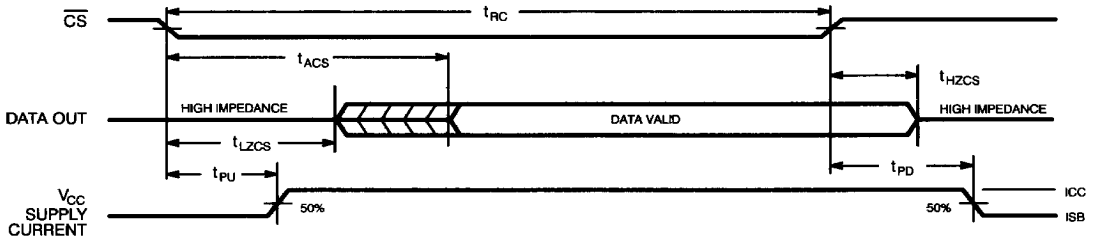
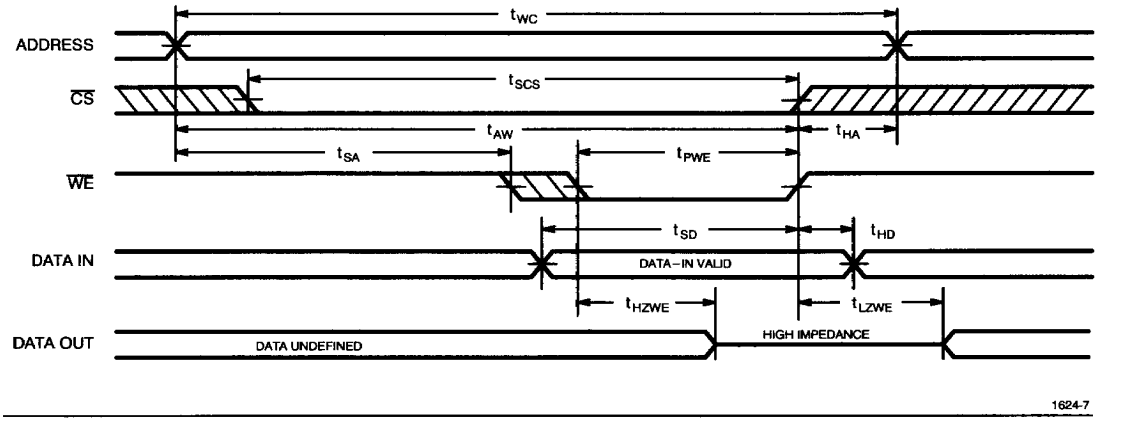
Switching Waveforms (continued)

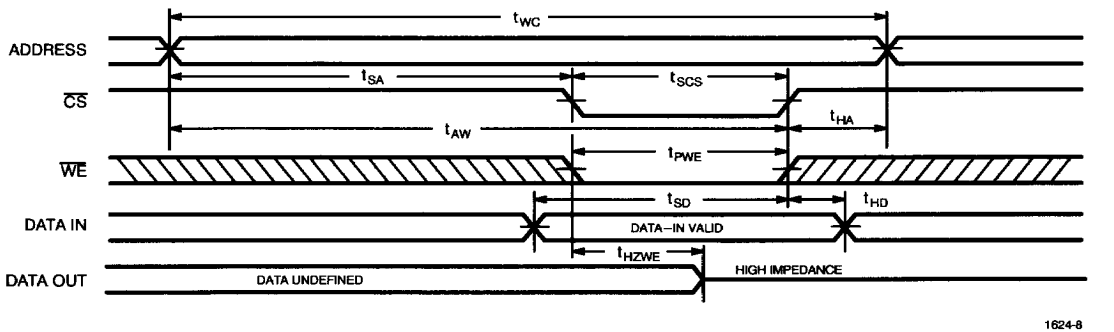
Read Cycle No. 2 [6, 8]



Write Cycle No. 1 ($\overline{WE}$ Controlled) [5]



Write Cycle No. 2 ($\overline{CS}$ Controlled) [5, 9]



Truth Table

$\overline{CS}$	$\overline{WE}$	Input/Outputs	Mode
H	X	High Z	Deselect Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
25	CYM1624PV-25C	PV01	Commercial
35	CYM1624PV-35C	PV01	Commercial
45	CYM1624PV-45C	PV01	Commercial

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