

MOS FIELD EFFECT TRANSISTOR

NP24N10CLB, NP24N10DLB, NP24N10ELB

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

These products are N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance
 $R_{DS(on)1} = 80 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 12 \text{ A)}$
 $R_{DS(on)2} = 93 \text{ m}\Omega \text{ MAX. (} V_{GS} = 5.0 \text{ V, } I_D = 10 \text{ A)}$
- Low C_{iss} : $C_{iss} = 1300 \text{ pF TYP.}$
- Built-in gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP24N10CLB	TO-220AB
NP24N10DLB	TO-262
NP24N10ELB	TO-263

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DS}	100	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 24	A
Drain Current (Pulse) ^{Note1}	$I_{D(pulse)}$	± 80	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	1.8	W
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_T	100	W
Single Avalanche Current ^{Note2}	I_{AS}	24 / 7	A
Single Avalanche Energy ^{Note2}	E_{AS}	57 / 245	mJ
Repetitive Avalanche Current ^{Note3}	I_{AR}	20	A
Repetitive Avalanche Energy ^{Note3}	E_{AR}	10	mJ
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$

Notes 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$

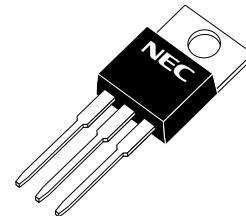
2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

3. $T_{ch} \leq 175^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$, Duty cycle $\leq 3\%$

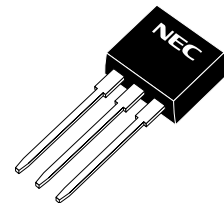
THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.50	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

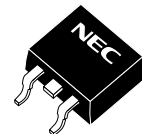
(TO-220AB)



(TO-262)



(TO-263)



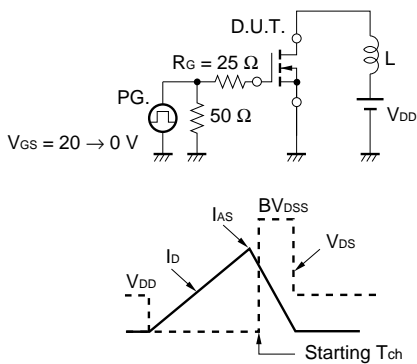
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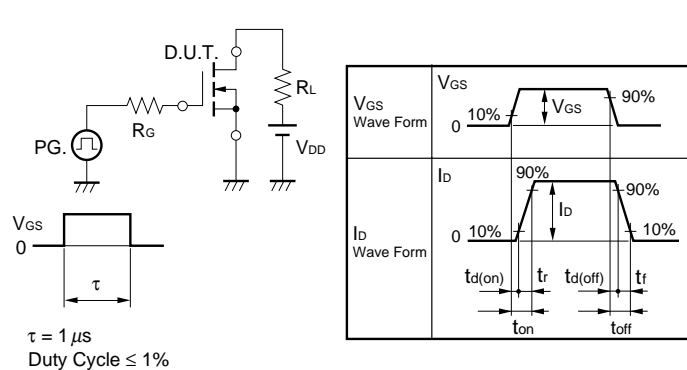
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 10 A	12	22		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 12 A		55	80	mΩ
	R _{DS(on)2}	V _{GS} = 5.0 V, I _D = 10 A		61	93	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 10 A		65	100	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		1300	3100	pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		460	700	pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		150	300	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 50 V, I _D = 10 A		22	50	ns
Rise Time	t _r	V _{GS} = 10 V		110	280	ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		140	280	ns
Fall Time	t _f			120	280	ns
Total Gate Charge	Q _G	V _{DD} = 80 V		51	80	nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		4.9		nC
Gate to Drain Charge	Q _{GD}	I _D = 20 A		15		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 20 A, V _{GS} = 0 V		1.1		V
Reverse Recovery Time	t _{rr}	I _F = 20 A, V _{GS} = 0 V		170		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		770		nC

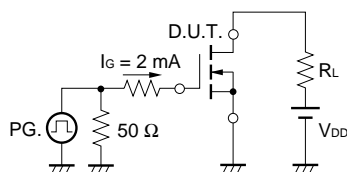
TEST CIRCUIT 1 AVALANCHE CAPABILITY



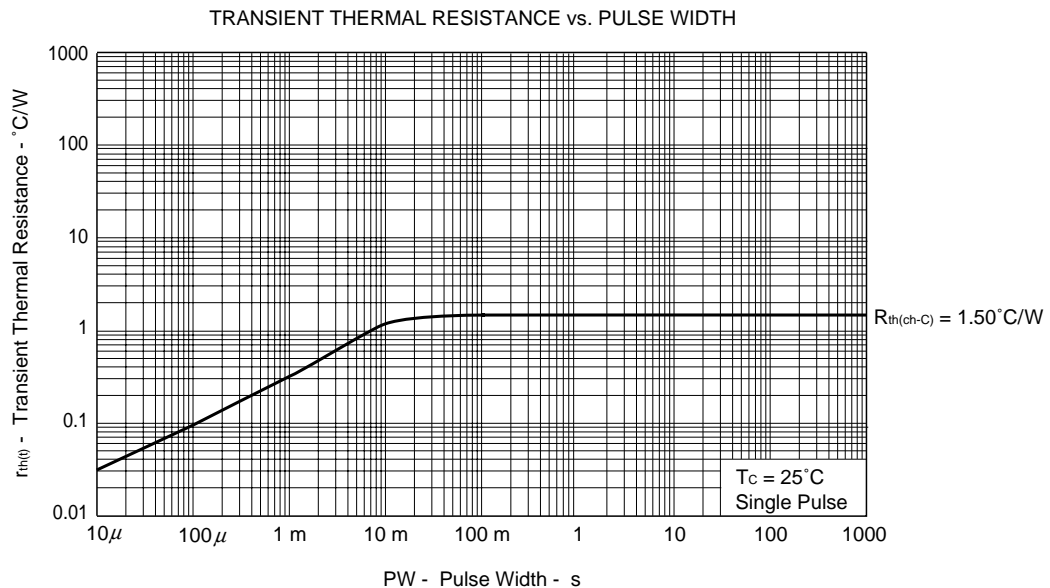
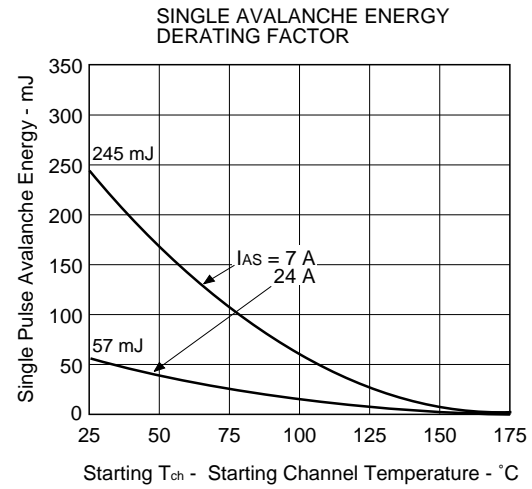
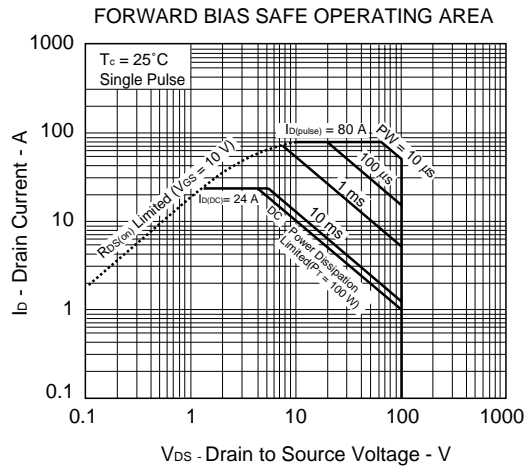
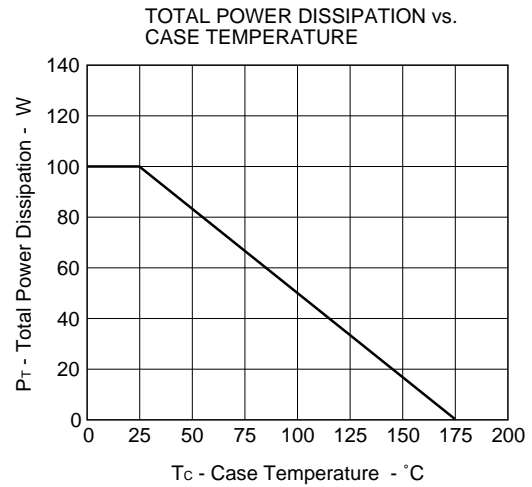
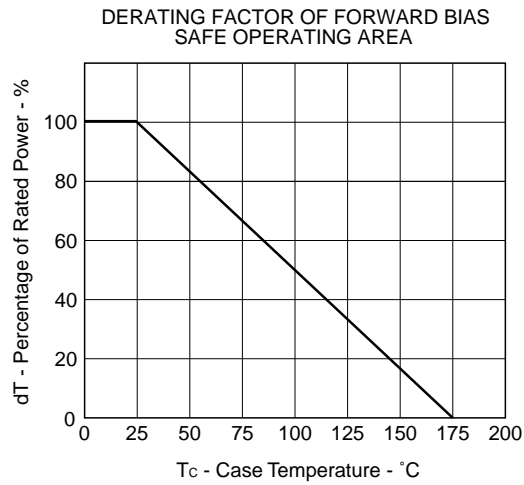
TEST CIRCUIT 2 SWITCHING TIME

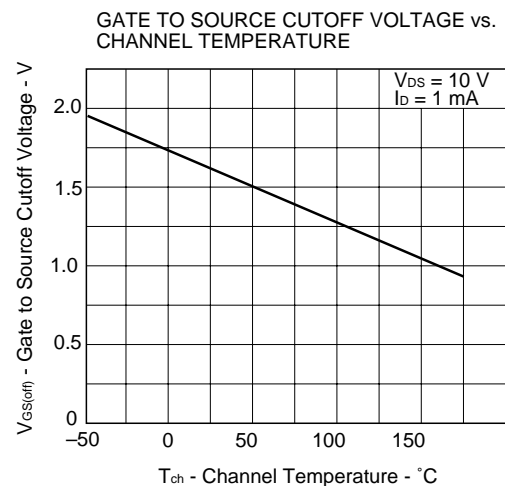
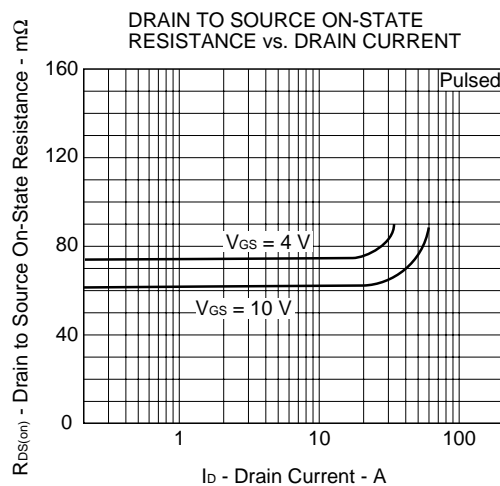
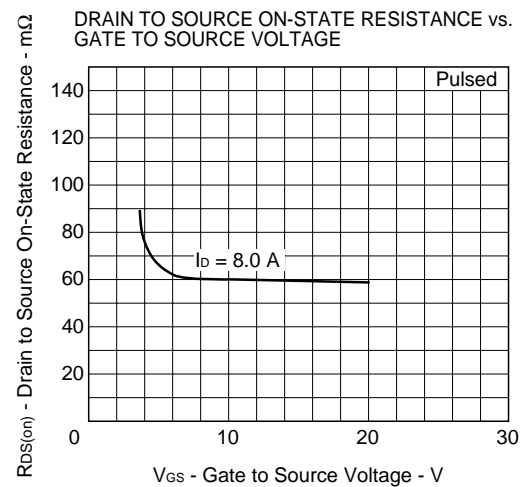
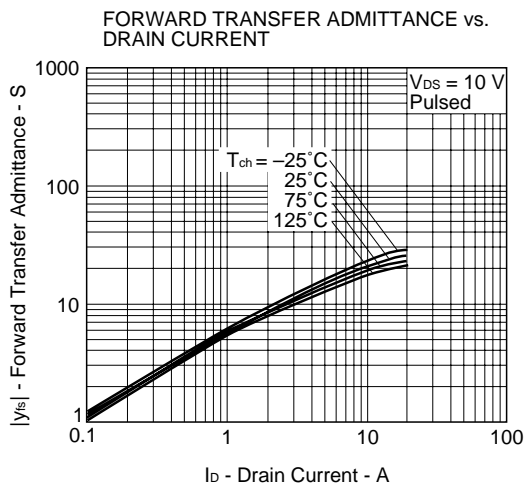
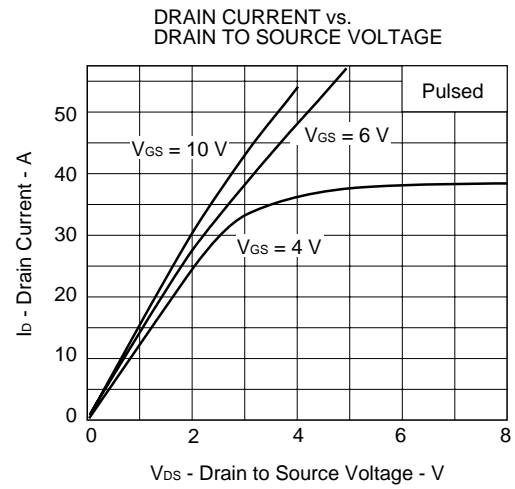
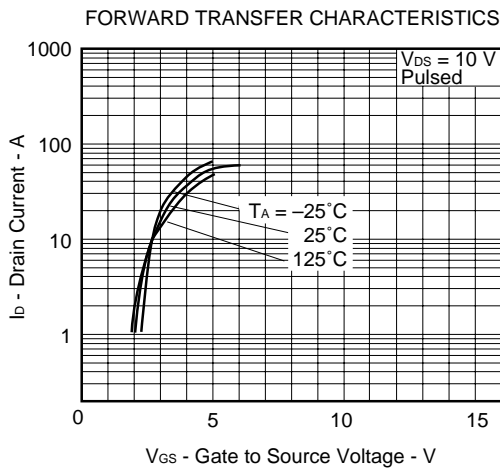


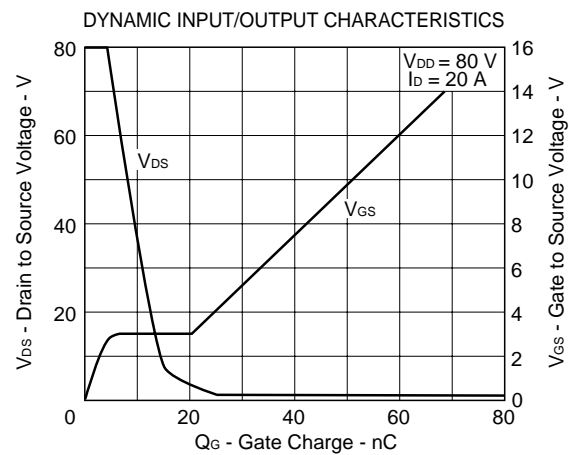
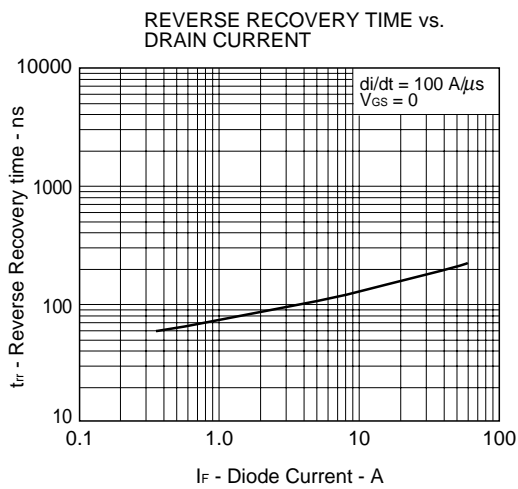
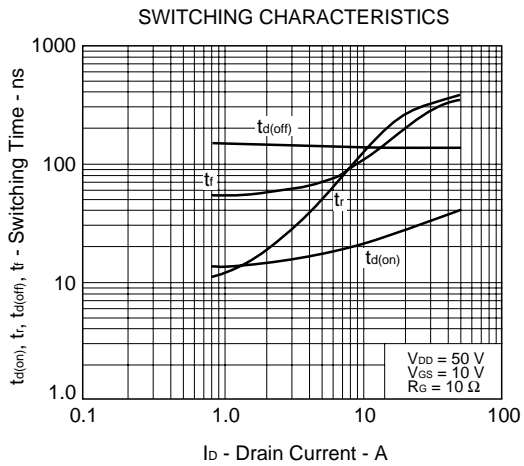
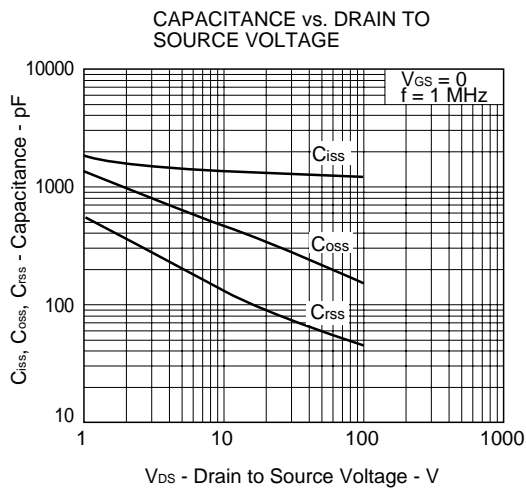
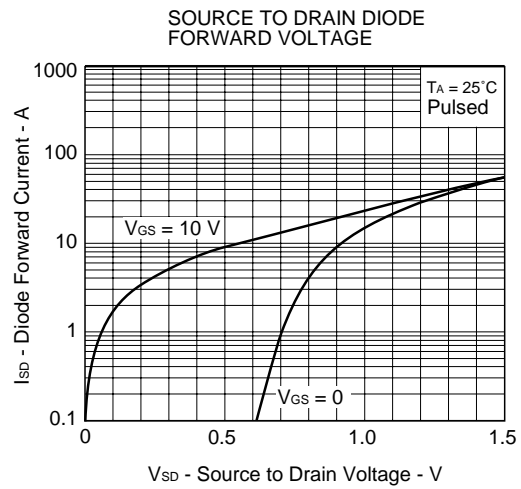
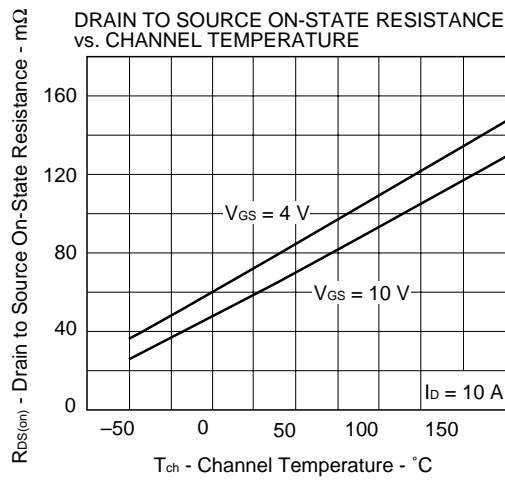
TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

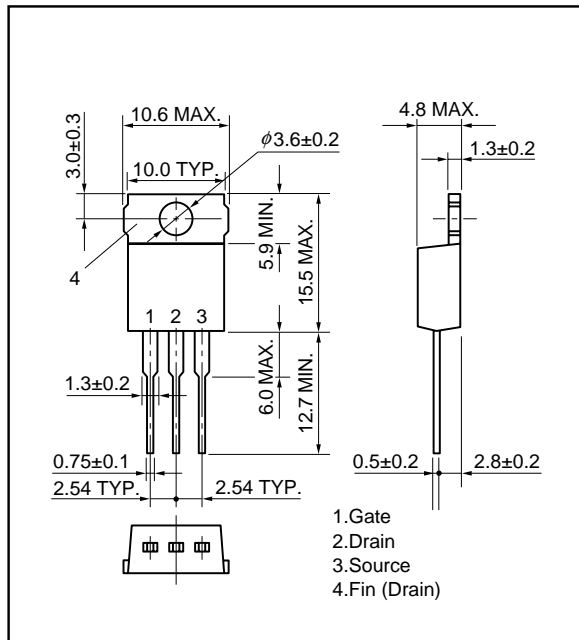




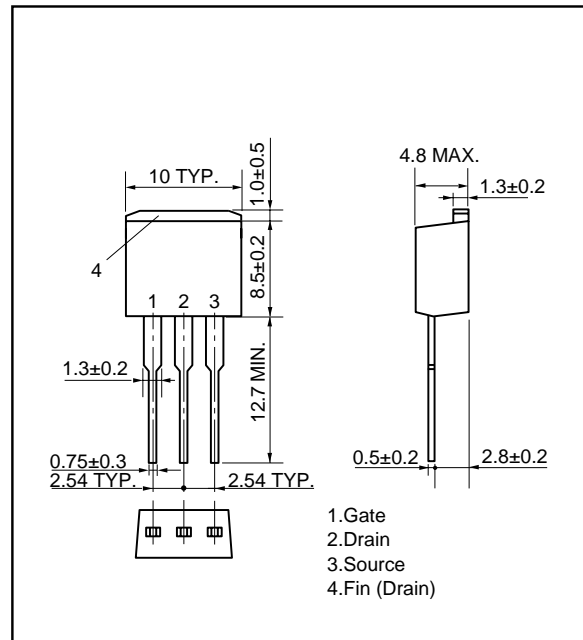


PACKAGE DRAWINGS (Unit: mm)

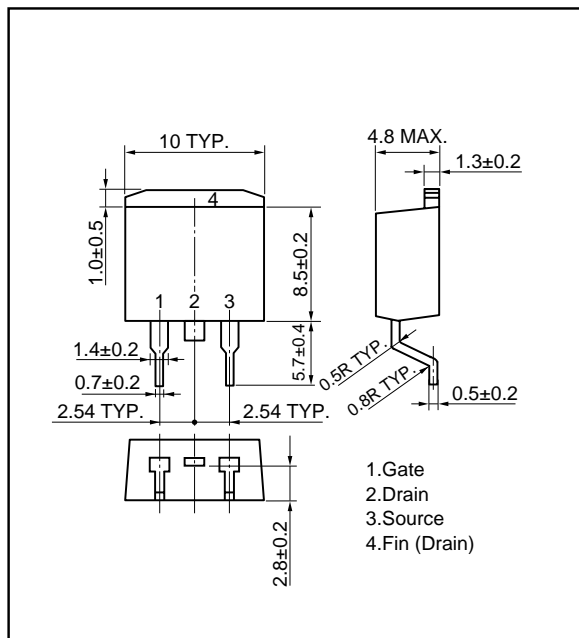
1) TO-220AB (MP-25)



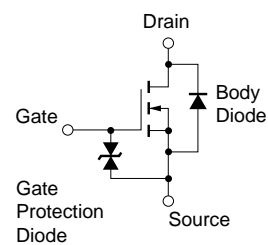
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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