RC4153 Voltage-to-Frequency Converter

Features

- 0.1Hz to 250kHz dynamic range
- 0.01% F.S. maximum nonlinearity error — 0.1Hz to 10kHz
- 50ppm/°C maximum gain temperature coefficient (external reference)
- Few external components required

Applications

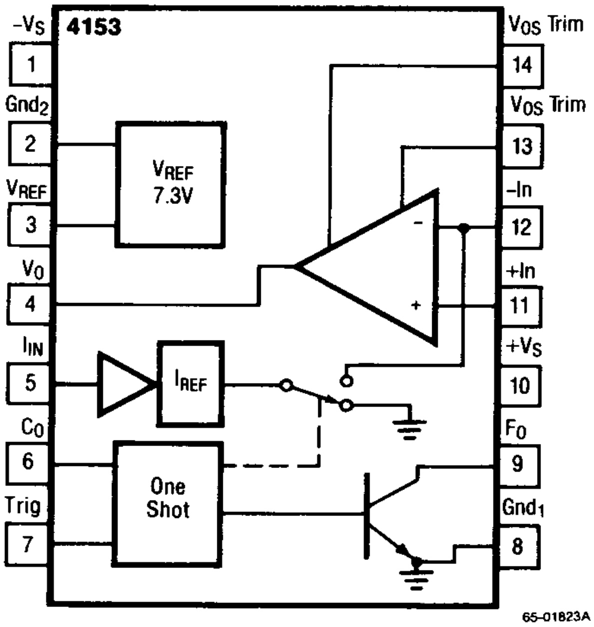
- Precision voltage-to-frequency converters
- Serial transmission of analog information
- Pulse width modulators
- Frequency-to-voltage converters
- A/D converters and long term integrators
- Signal isolation
- FSK modulation/demodulation
- Frequency scaling
- Motor speed controls
- Phase lock loop stabilization

Description

The 4153 sets a new standard for ease of application and high frequency performance in monolithic voltage-to-frequency converters. This voltage-to-frequency requires only four passive external components for precision operation, making it ideal for many low cost applications such as A/D conversion, frequency-to-voltage conversion, and serial data transmission. The improved linearity at high frequency makes it comparable to many dual slope A/D converters both in conversion time and accuracy, while retaining the benefits of voltage-to-frequency conversion, i.e., serial output, cost and size. The speed, accuracy, and temperature performance of the 4153 is achieved by incorporating high speed ECL logic, a high gain, wide bandwidth op amp, and a buried zener reference on a single monolithic chip.

4153 Functional Block Diagram

14 Lead
Dual In-Line Package
(Top View)



Pin	Function	Pin	Function
1	$-V_S$	8	Circuit Gnd
2	REF Gnd	9	Frequency Output (Open Collector)
3	V_{REF} Output	10	$+V_S$
4	V_{OUT} (Op Amp)	11	(+) Op Amp Input
5	I_{IN} (REF Input)	12	(-) Op Amp Input
6	C_O (Pulse Width)	13	V_{OS} Trim
7	Trigger Input	14	V_{OS} Trim

Ordering Information

Part Number	Package	Operating Temperature Range
RC4153D	D	0°C to +70°C
RM4153D	D	-55°C to +125°C

Notes:
D = 14- lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

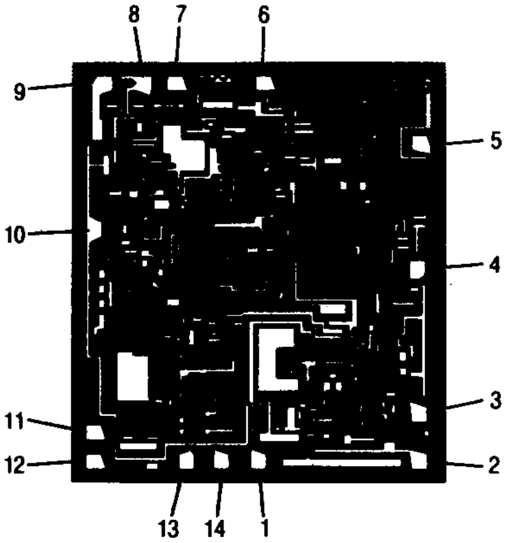
Absolute Maximum Ratings

Supply Voltage	±18V
Internal Power Dissipation	500 mW
Input Voltage Range	$-V_S$ to $+V_S$
Output Sink Current (Freq. Output)	20 mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
RM4153	-55°C to +125°C
RC4153	0°C to +70°C

Thermal Characteristics

	14-Lead Ceramic DIP
Max. Junction Temp.	175°C
Max. P_D T_A <50°C	1042 mW
Therm. Res θ_{JC}	60°C/W
Therm. Res. θ_{JA}	120°C/W
For T_A >50°C Derate at	8.33 mW/°C

Mask Pattern



Die Size: 90 x 108 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Min	Typ	Max	Units
Power Supply Requirements Supply Voltage	±12	±15	±18	V
Supply Current (I_O = 0, Pos) (I_O = 0, Neg)		+4.2 -7	+7.5 -10	mA
Full Scale Frequency	250	500		kHz
Transfer Characteristics Nonlinearity Error Voltage-to-Frequency[1] 0.1 Hz ≤ F_{OUT} ≤ 10 kHz		0.002	0.01	%FS
0.1 Hz ≤ F_{OUT} ≤ 100 kHz		0.025	0.05	%FS
5.0 Hz ≤ F_{OUT} ≤ 250 kHz		0.06	0.1	%FS
Nonlinearity Error Frequency-to-Voltage[1] 0.1 Hz ≤ F_{IN} ≤ 10 kHz		0.002	0.01	%FS
0.1 Hz ≤ F_{IN} ≤ 100 kHz		0.05	0.1	%FS
5.0 Hz ≤ F_{IN} ≤ 250 kHz		0.07	0.12	%FS
Scale Factor Tolerance, F = 10 kHz $K = \frac{1}{2V_{REF} R_{IN} C_O}$		±0.5		%
Change of Scale Factor With Supply		0.008		%/V
Reference Voltage (V_{REF})		7.3		V
Temperature Stability [1,2,3] Scale Factor 10 kHz Nominal		±75	±150	ppm/°C
Reference Voltage		±50	±100	ppm/°C
Scale Factor (External Ref) 10 kHz FS		±25	±50	ppm/°C
Scale Factor (External Ref) 100 kHz FS		±50	±100	ppm/°C
Scale Factor (External Ref) 250 kHz FS		±100	±150	ppm/°C

Notes:

1. Guaranteed but not tested.
2. V_{REF} Range 6.6V ≤ VR ≤ 8.0V.
3. Over the specified operating temperature range

Electrical Characteristics (Continued)

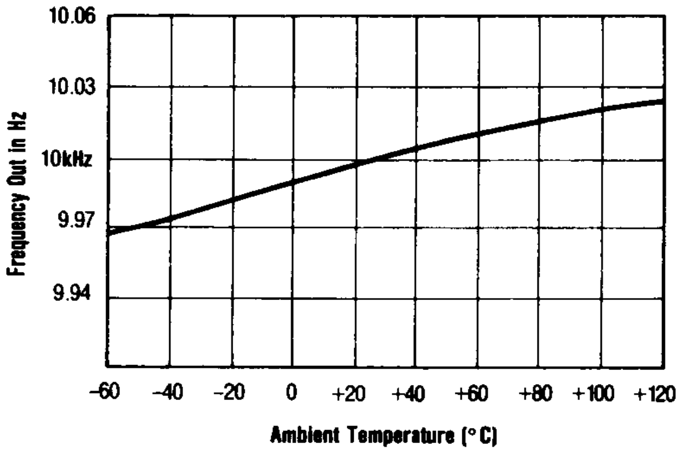
Parameters	Min	Typ	Max	Units
Op Amp				
Open Loop Output Resistance		230		Ω
Short Circuit Current		25		mA
Gain Bandwidth Product[1]	2.5	3.0		MHz
Slew Rate	0.5	2.0		V/µS
Output Voltage Swing ($R_L \geq 2K$)	0 to +10	-0.5 to +14.3		V
Input Bias Current		70	400	nA
Input Offset Voltage (Adjustable to 0)		0.5	5.0	mV
Input Offset Current		30	60	nA
Input Resistance (Differential Mode)		1.0		MΩ
Common Mode Rejection Ratio	75	100		dB
Power Supply Rejection Ratio	70	106		dB
Large Signal Voltage Gain	25	350		V/mV
Switched Current Source				
Reference Current (Ext Ref)		1.0		mA
Digital Input (Frequency-to-Voltage, Pin 7)				
Logic "0"			0.5	V
Logic "1"	2.0			V
Trigger Current		-50		µA
Logic Output (Open Collector)				
Saturation Voltage (Pin 9)				
I_{SINK} = 4 mA		0.15	0.4	V
I_{SINK} = 10 mA		0.4	1.0	V
Leakage Current (Off State)		150		nA

Notes:

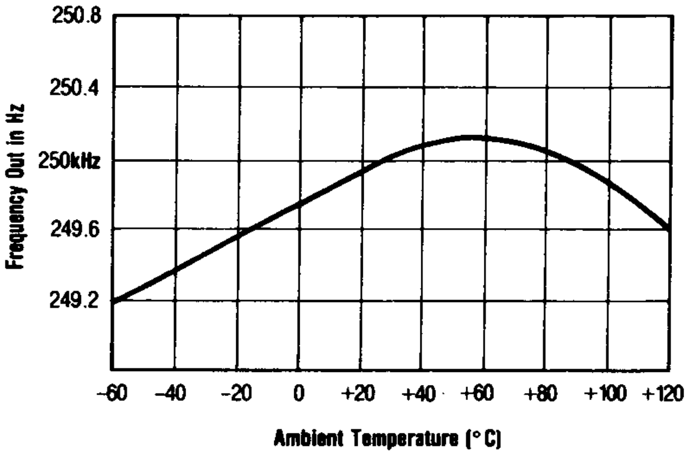
1. Guaranteed but not tested.

Typical Performance Characteristics

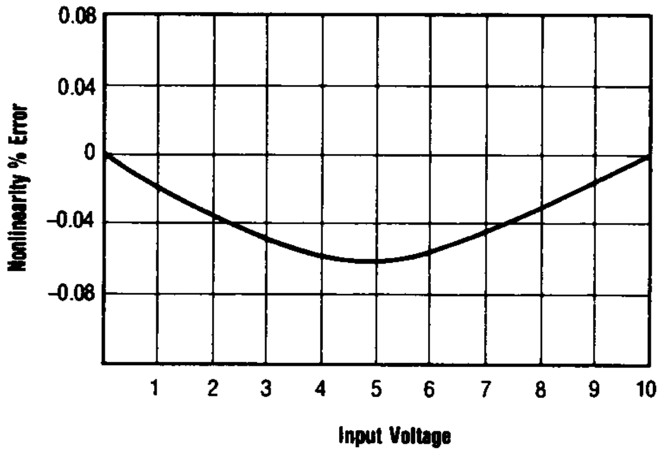
4153 10kHz Full Scale Temperature Drift



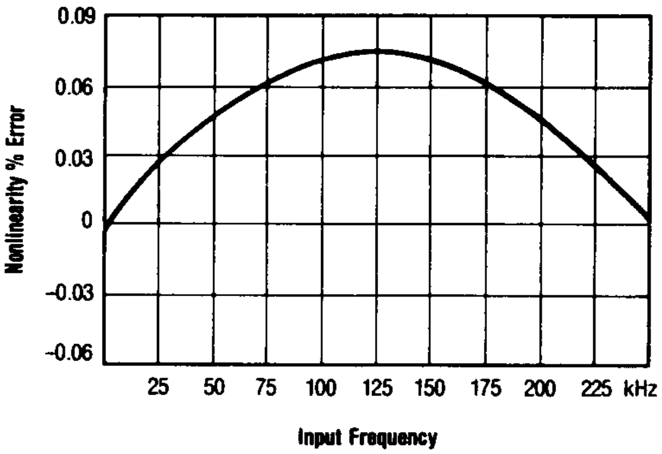
4153 250kHz Full Scale Temperature Drift



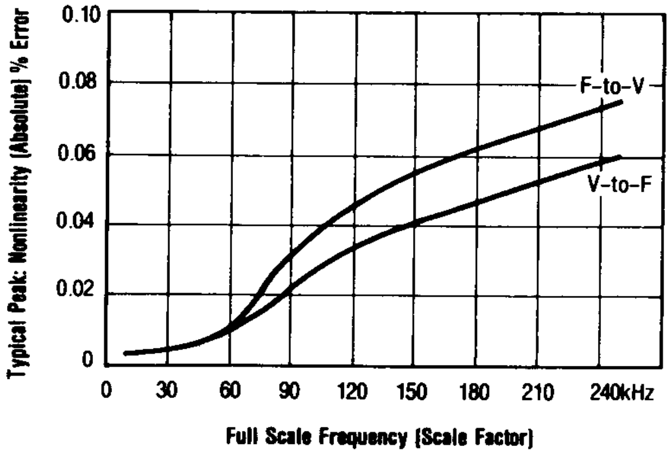
4153 250kHz Frequency-to-Voltage Nonlinearity



4153 250kHz Voltage-to-Frequency Nonlinearity

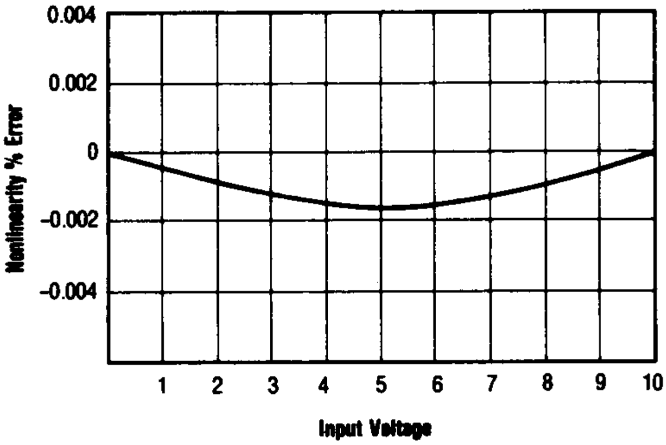


4153 Scale Factor vs. Typical Peak Linearity

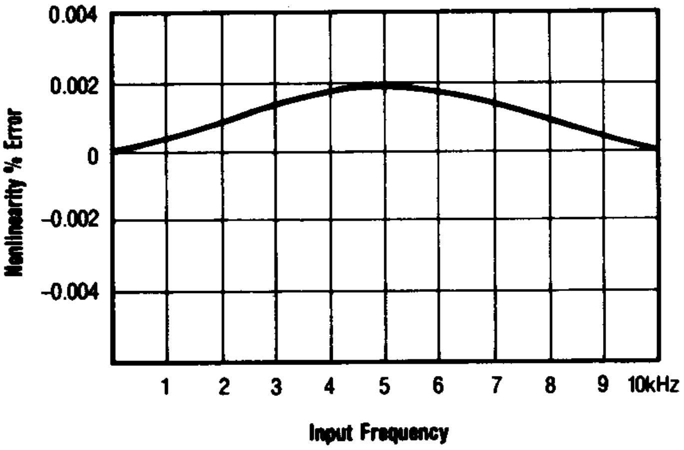


Typical Performance Characteristics (Continued)

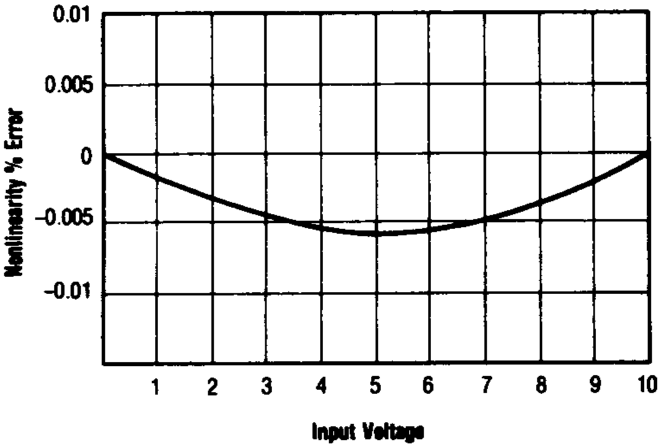
4153 10kHz Voltage-to-Frequency Nonlinearity



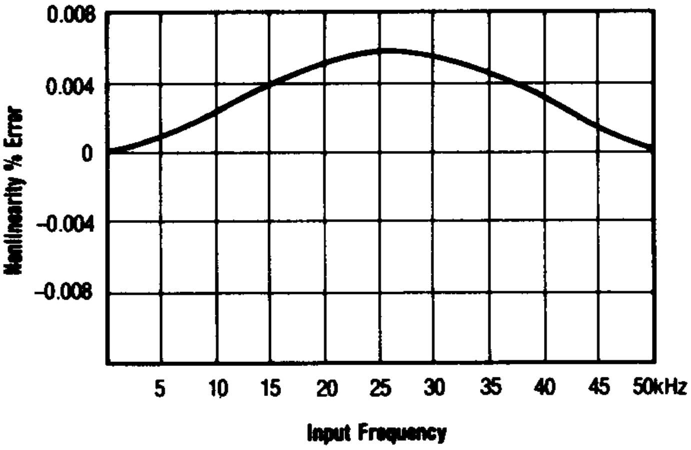
4153 10kHz Frequency-to-Voltage Nonlinearity



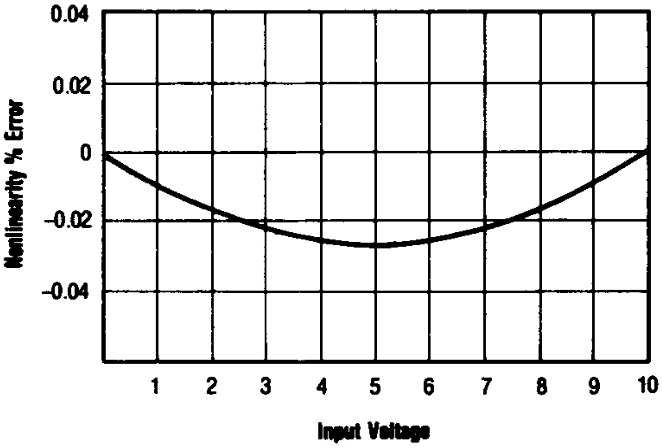
4153 50kHz Voltage-to-Frequency Nonlinearity



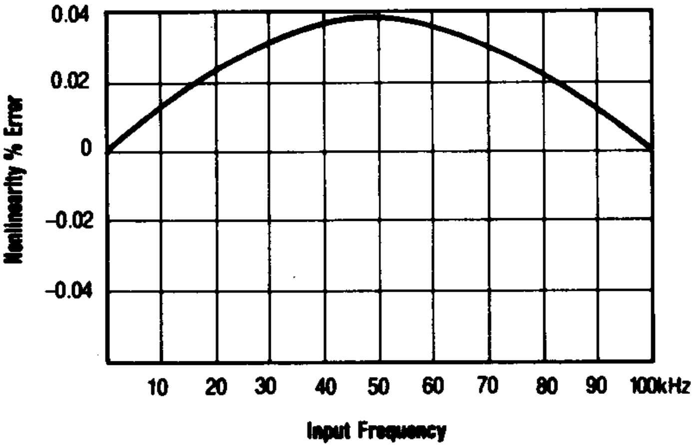
4153 50kHz Frequency-to-Voltage Nonlinearity



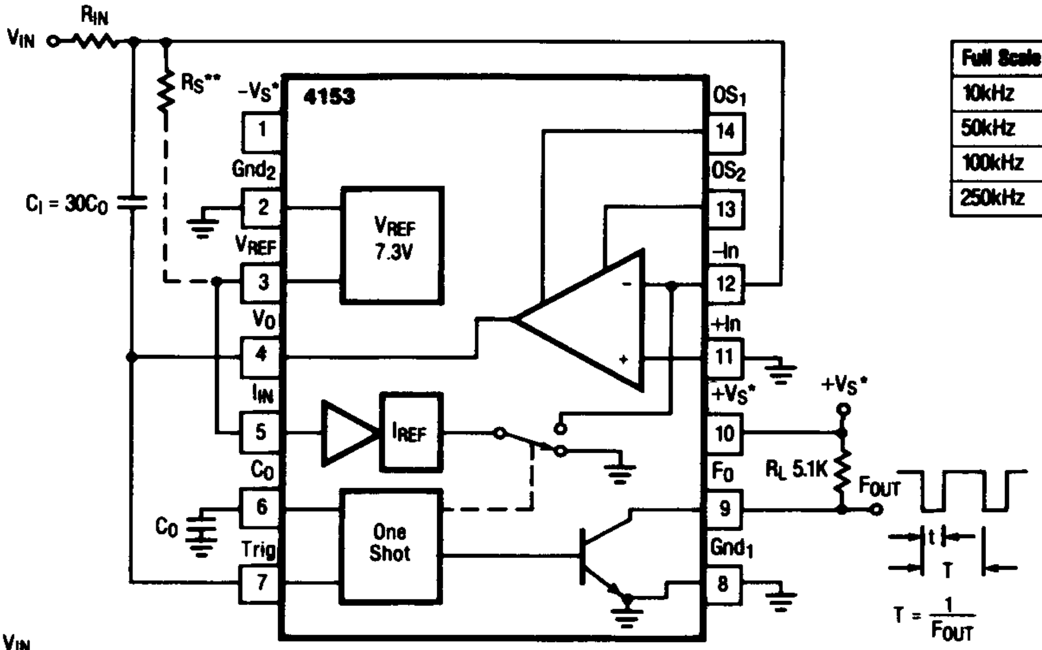
4153 100kHz Voltage-to-Frequency Nonlinearity



4153 100kHz Frequency-to-Voltage Nonlinearity



Typical Application Circuits



Full Scale	C_I	C_O	R_IN
10kHz	0.1μF	3300pF	20K
50kHz	0.02μF	680pF	20K
100kHz	4300pF	330pF	20K
250kHz	1000pF	130pF	20K

$F_{OUT} = \frac{V_{IN}}{2V_{REF} R_{IN} C_O}$

$(V_{REF} = 7.3V)$

**For Bipolar Input

$F_{OUT} = \frac{V_{IN} R_S + V_{REF} R_{IN}}{2R_{IN} R_S V_{REF} C_O}$

$T = \frac{1}{F_{OUT}}$

$t = 1.5 \times 10^4 C_O$

$C_O \leq \frac{5 \times 10^{-5}}{F_{OUT}\,(max)}$

*±V_S must be thoroughly decoupled.
**For Bipolar Input.
Resistance in Ohms unless otherwise specified.

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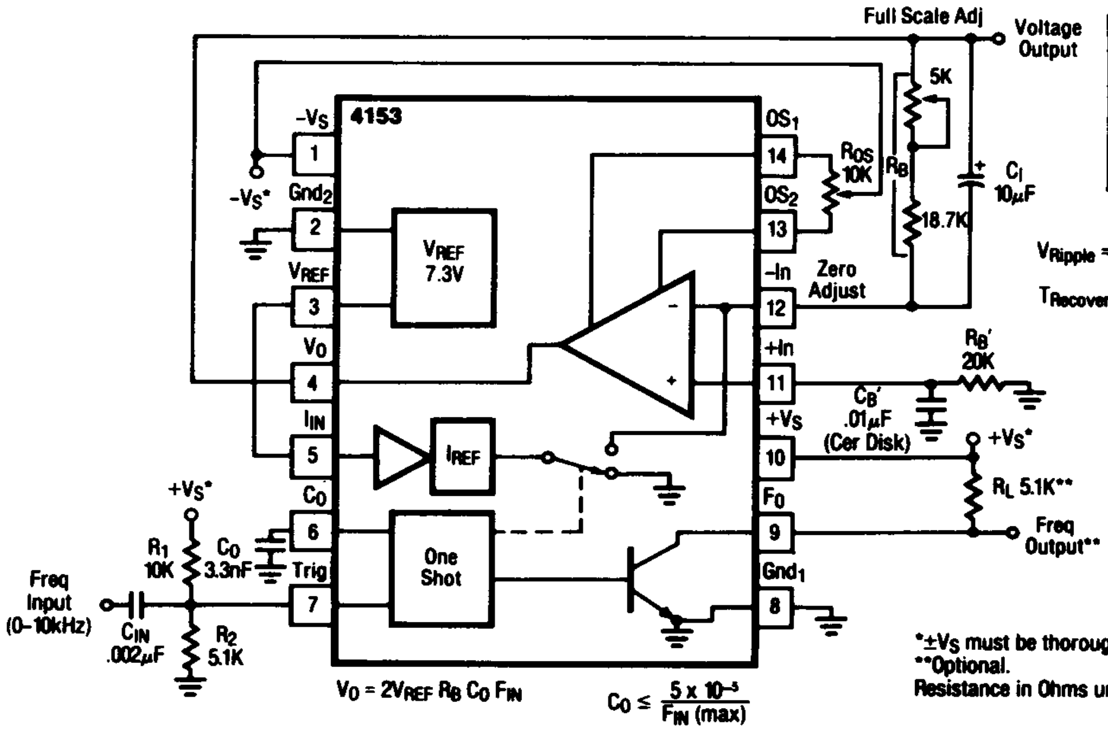
Figure 1. Voltage-to-Frequency Converter Minimum Circuit



Full Scale	C_I	C_O	R_B
10kHz	10μF	3300pF	20K
50kHz	2μF	330pF	40K
100kHz	1μF	150pF	43K
250kHz	0.2μF	60pF	39K

$V_{Ripple} = \frac{2V_{REF} C_O (1 - 1.5 \times 10^4 C_O F_{IN})}{C_I}$

$T_{Recovery} = 1.36 \times 10^4 C_I C_O R_B \Delta F_{IN}$

$V_O = 2V_{REF} R_B C_O F_{IN}$

$C_O \leq \frac{5 \times 10^{-5}}{F_{IN}\,(max)}$

*±V_S must be thoroughly decoupled.
**Optional.
Resistance in Ohms unless otherwise specified.

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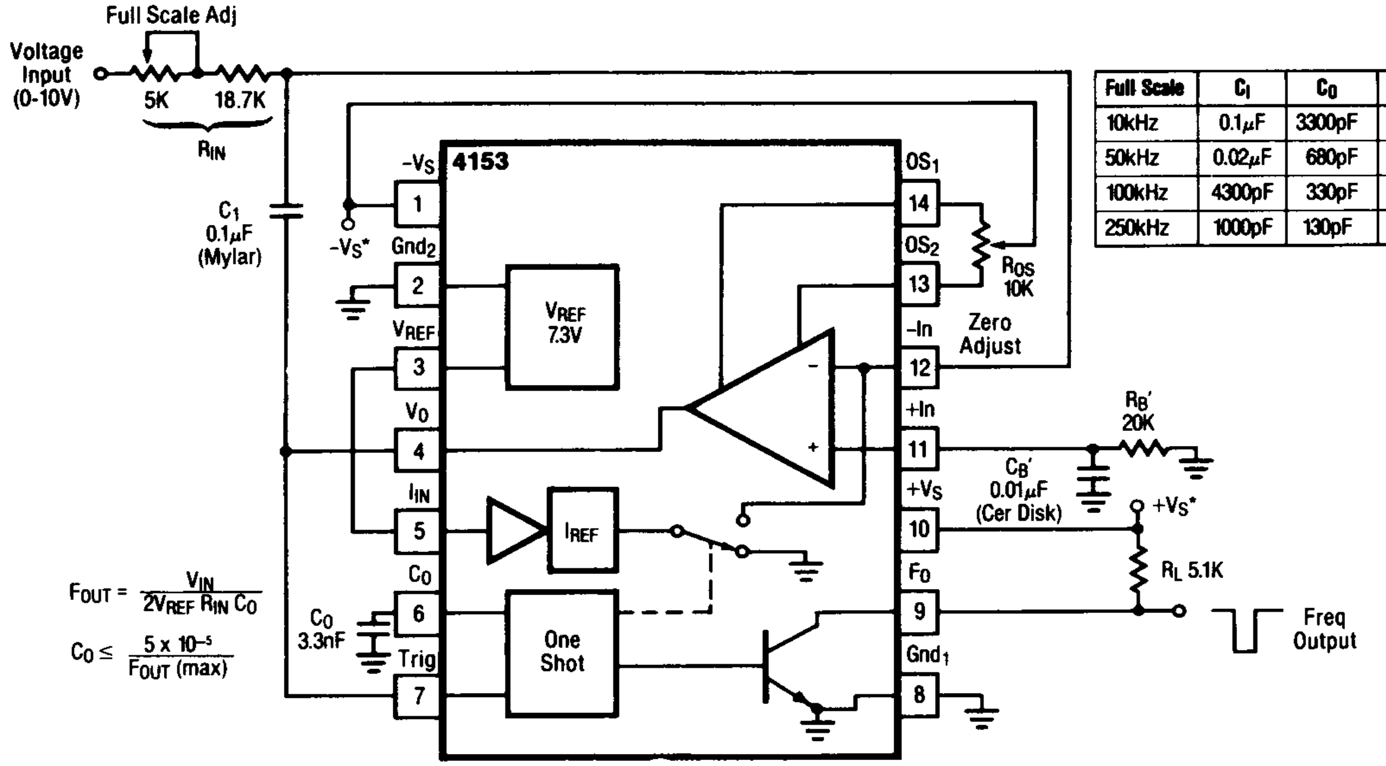
Figure 2. Frequency-to-Voltage Converter — V_O (Volts) = F_{IN} (kHz) — 100kHz Max

Typical Application Circuits (Continued)



Full Scale	C_I	C_O	R_{IN}
10kHz	0.1µF	3300pF	20K
50kHz	0.02µF	680pF	20K
100kHz	4300pF	330pF	20K
250kHz	1000pF	130pF	20K

$$F_{OUT} = \frac{V_{IN}}{2V_{REF}\,R_{IN}\,C_O}$$

$$C_O \leq \frac{5 \times 10^{-5}}{F_{OUT}\,(\mathrm{max})}$$

*±V_S must be thoroughly decoupled.
Resistance in Ohms unless otherwise specified.

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Figure 3. Voltage-to-Frequency Converter With Offset and Gain Adjusts

Principles of Operation

The 4153 consists of several functional blocks which provide either voltage-to-frequency or frequency-to-voltage conversion, depending on how they are connected. The operation is best understood by examining the block diagram as it is powered in a voltage-to-frequency mode.

When power is first applied, all capacitors are discharged. The input current, V_{IN}/R_{IN}, causes C_{IN} to charge, and point **C** will try to ramp down. The trigger threshold of the one-shot is approximately +1.3V, and if the integrator output is less than +1.3V, the one-shot will fire and pulse the open collector output **E** and the switched current source **A** (see Figures 4 and 5). Because the point **C** is less than +1.3V, the one-shot fires, and the switched current source delivers a negative current pulse to the integrator. This causes C_{IN} to charge in the opposite direction, and point **C** will ramp up until the end of the one-shot pulse. At that time, the positive current V_{IN}/R_{IN} will again make point **C** ramp down until the trigger threshold is reached.

When power is applied, the one-shot will continuously fire until the integrator output exceeds the trigger threshold. Once this is reached, the one-shot will fire as needed to keep the integrator output above the trigger threshold. If V_{IN} is increased, the slope of the downward ramp increases, and the one-shot will fire more often in order to keep the integrator output high. Since the one-shot firing frequency is the same as the open collector output frequency, any increase in V_{IN} will cause an increase in F_{OUT}. This relationship is very linear because the amount of charge in each I_{OUT} pulse is carefully defined, both in magnitude and duration. The duration of the pulse is set by the timing capacitor C_O (point **D**). This feedback system is called a charge balanced loop.

The scale factor (the number of pulses per second for a specified V_{IN}) is adjusted by changing either R_{IN} and therefore I_{IN}, or by changing the amount of charge in each I_O pulse. Since the magnitude of I_O is fixed at 1 milliamp,

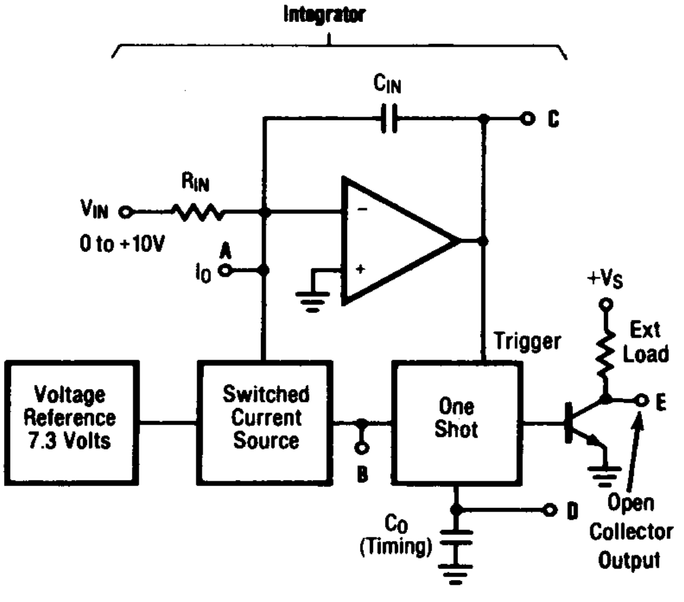

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Figure 4. VFC Block Diagram

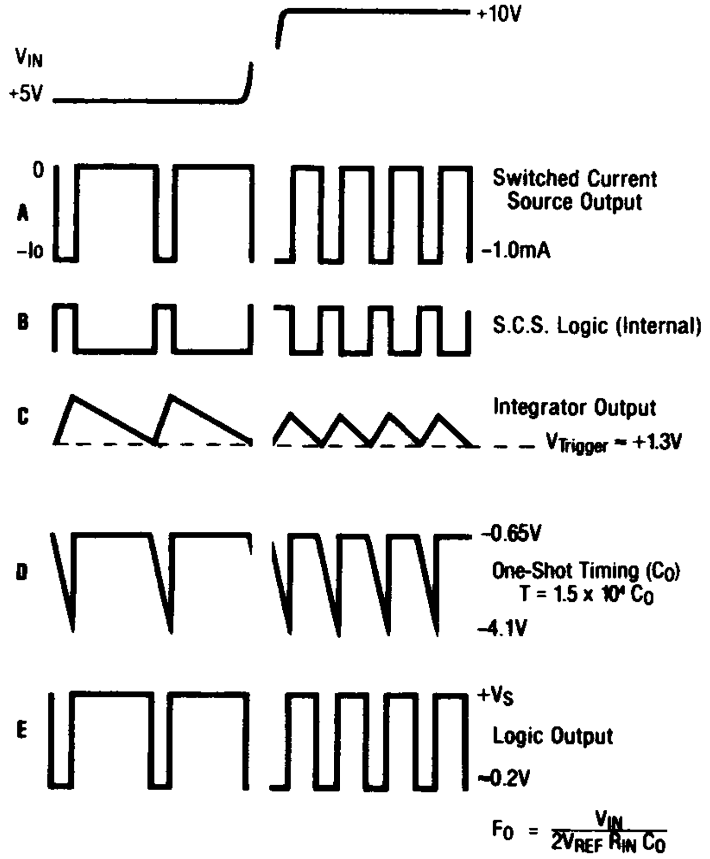

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Figure 5. 4153 Voltage-to-Frequency Timing Waveforms

the way to change the amount of charge is by adjusting the one-shot duration set by C_O. (I_O may be adjusted by changing V_{REF}.) The accuracy of the relationship between V_{IN} and F_{OUT} is affected by three major sources of error: temperature drift, nonlinearity, and offset.

The total temperature drift is the sum of the individual drift of the components that make up the system. The greatest source of drift in a typical application is in the timing capacitor; C_O. Low temperature coefficient capacitors, such as silver mica and polystyrene, should be measured for drift, using a capacitance meter. Experimentation has shown that the lowest tempco's are achieved by wiring a parallel capacitor composed of 70% silver mica and 30% polystyrene.

The reference on the chip can be replaced by an external reference with much tighter drift specifications, such as an LM199. The 199s 6.9V output is close to the 4153s 7.3V output, and has less than 10 ppm/° C drift.

Nonlinearity is primarily caused by changes in the precise amount of charge in each I_{OUT} pulse. As frequency increases, internal stray capacitances and switching problems change the width and amplitude of the I_{OUT} pulses, causing a nonlinear relationship between V_{IN} and F_{OUT}. For this reason, the scale factor you choose should be below 1kHz/V or as low as the acquisition time of your system will allow.

Nonlinearity is also affected by the ratio of C_I to C_O. Less error can be achieved by increasing the value of C_I, but this affects response time and temperature drift. Optimum values for C_I and C_O are shown in the tables in Figures 1, 2, and 3. These values represent the best compromise of nonlinearity and temperature drift. Polypropylene, mylar or polystyrene capacitors should be used for C_I.

The accuracy at low input voltages is limited by the offset and V_{OS} drift of the op amp. To improve this condition, an offset adjust is provided.
Once your system is running, it may be calibrated as follows: apply a measured full scale input voltage and adjust R_{IN} until the scale factor is correct. For precise applications, trimming by soldering metal film resistors in parallel is recommended instead of trimpots, which have bad tempco's and are easily taken out of adjustment by mechanical shock. After the scale factor is calibrated, apply a known small input voltage (approximately 10mV) and adjust the op amp offset until the output frequency equals the input multiplied by the scale factor.

The output **E** consists of a series of negative going pulses with a pulse width equal to the one-shot time. The open collector pull up resistor may be connected to a different supply (such as 5V for TTL) as long as it does not exceed the value of $+V_S$ applied to pin 10. The load current should be kept below 10mA in order to minimize strain on the device. Pins 2 and 8 must be grounded in all applications, even if the open collector transistor is not used.

Figure 6 shows the complete circuit for a precision frequency-to-voltage converter. This circuit converts an input frequency to a proportional voltage by integrating the switched current source output. As the input frequency increases, the number of I_{OUT} pulses delivered to the integrator increases, thus increasing the average output voltage. Depending on the time constant of the integrator, there will be some ripple on the output. The output may be further filtered, but this will reduce the response time. A second order filter will decrease ripple and improve response time.

The output waveform must meet three conditions for proper frequency-to-voltage operation. First, it must have sufficient amplitude and offset to swing above and below the 1.3V trigger threshold. (See Figure 6 for an example of AC coupling and offset bias.) Second, it must be a fast slewing waveform having a quick rise time. A comparator may be used to square it up. Finally, the input pulse width must not exceed the one-shot time, in order to avoid retriggering the one-shot (AC couple the input).

Capacitive coupling between the trigger input and the timing capacitor pin may occur if the input waveform is a squarewave or the input has a short period. This can cause gross nonlinearity due to changes in the one-shot timing waveform (see Figure 7). This problem can be avoided by keeping the value of C_O small, and thereby keeping the timing period less than the input waveform period.

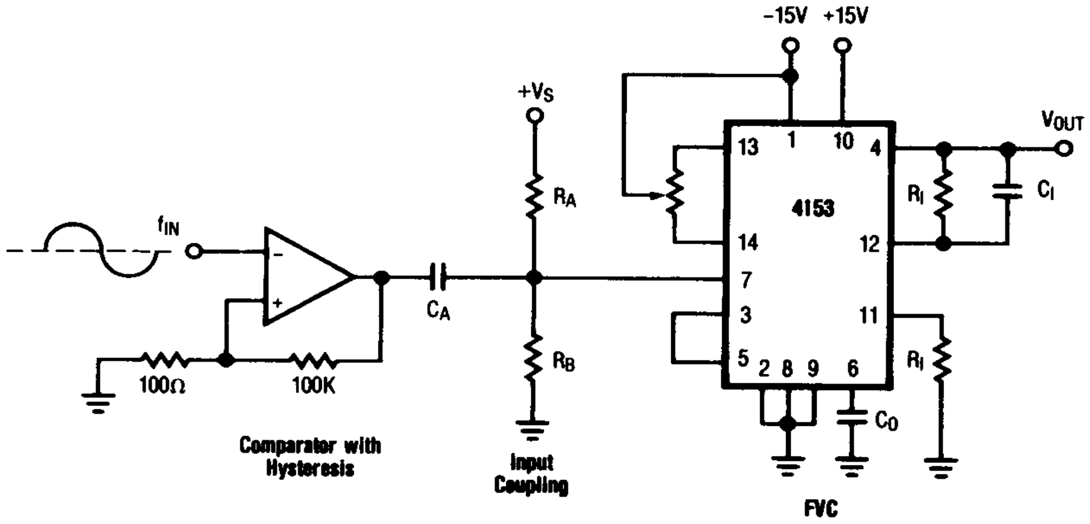

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Figure 6. FVC Input Conditioning

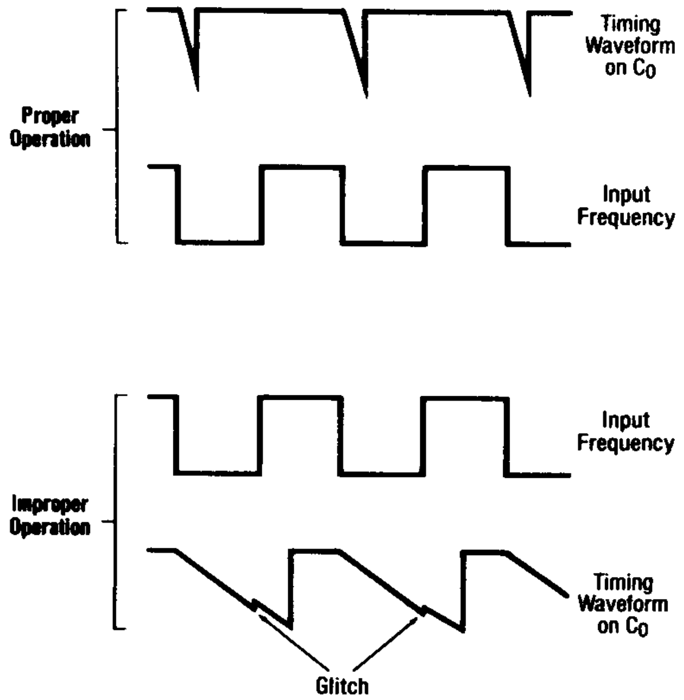

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Figure 7. FVC Timing Waveform

Detailed Circuit Operation

The circuit consists of a buried zener reference (breakdown occurs below the surface of the die, reducing noise and contamination), a high speed one-shot, a high speed switched precision voltage-to-current converter, and an open collector output transistor.

Figure 8 shows a block diagram of the high speed one-shot and Figure 9 shows the monolithic implementation. A trigger pulse sets the R-S latch, which lets C_O charge from I_T. When the voltage on C_O exceeds V_{TH}, the comparator resets the latch and discharges C_O. Looking at the detailed schematic, a positive trigger voltage turns on Q5, turns off Q4, and turns on Q3. Q3 provides more drive to Q5 keeping it on and latching the base of Q11 low. This turns on the switched current source and turns off Q1, allowing C_O to charge in a negative direction. When the voltage on C_O exceeds V_{TH}, Q13's collector pulls Q3's base down, resetting the latch, turning off the switched current source and discharging C_O through Q1. Note that all of the transistors in the signal path are NPNs and that the voltage swings are minimized ECL fashion to reduce delays. Minimum delay means minimum drift of the resultant VFC scale factor at high frequency.

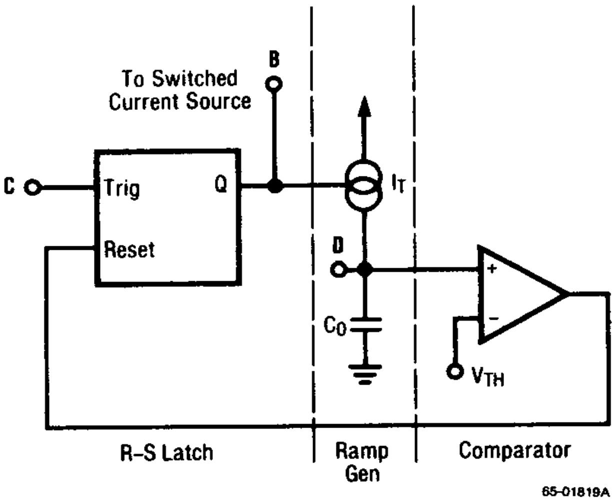

Figure 8. One-Shot Block Diagram

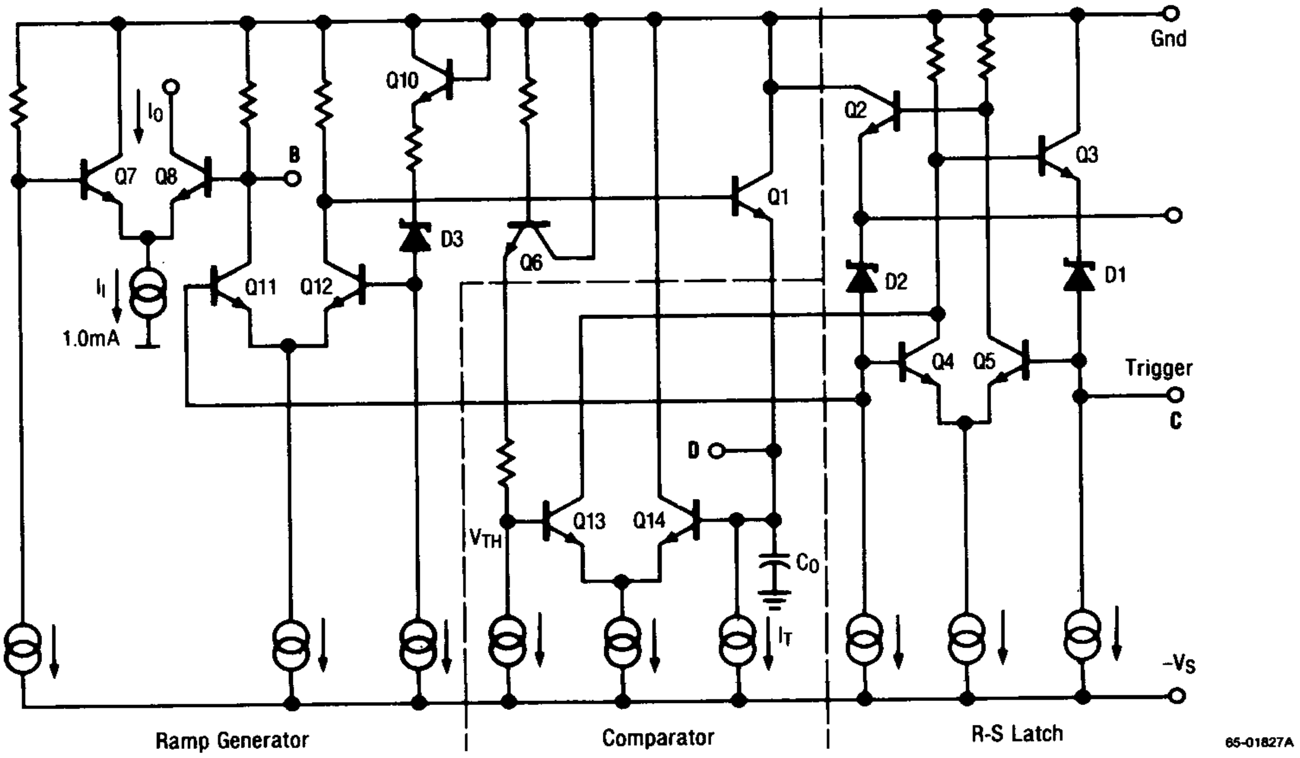

Figure 9. One-Shot Detail

The switched current source is shown as a block diagram in Figure 10 and detailed in Figure 11. The summing node (+ input of op amp) is held at 0V by the amplifier feedback, causing V_{REF} to be applied across R60. This current (V_{REF}/R60), minus the small amplifier bias current, flows through Q35. Q35 develops a V_{BE} dependent on that current. This V_{BE} is developed across Q36. Since Q35 and Q36 are equal in area, their currents are equal. This mirrored current is switched by the one-shot output.

The detail schematic shows the amplifier and load (Q21 through Q34), the mirror transistors (Q35, Q36) and the differential switching transistors (Q7, Q8). The amplifier uses a complementary paraphase input composed of Q21 through Q26 with a current mirror formed by Q27 through Q30, which converts from differential to single ended output. Level shift diodes Q32 and Q34 and emitter follower Q31 bootstrap the emitters of the mirror devices Q29 and Q30 to increase gain and lower input offsets, which would otherwise be caused by unbalanced collector voltages on Q23 and Q26. Matching emitter currents in Q35 and Q36 are assured by degeneration resistors R3 and R4. The differential switch allows the current source to remain active continuously, shunting to ground in the off state. This helps stabilize the output, and again, NPNs reduce switching time, timing errors, and most important, drift of timing errors over temperature.

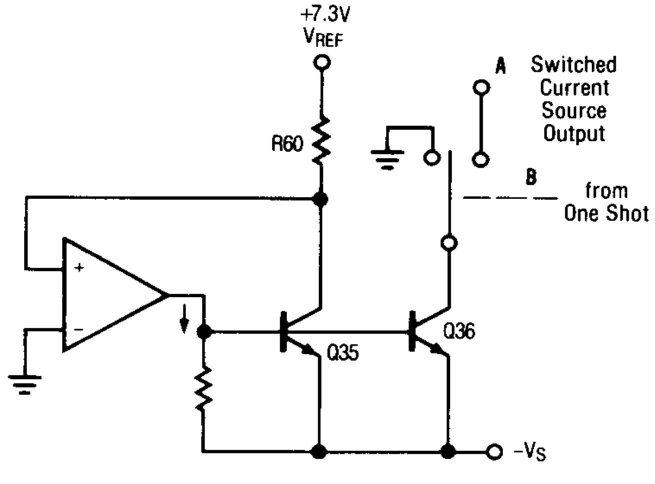

Figure 10. Switched Current Source Simplified Diagram

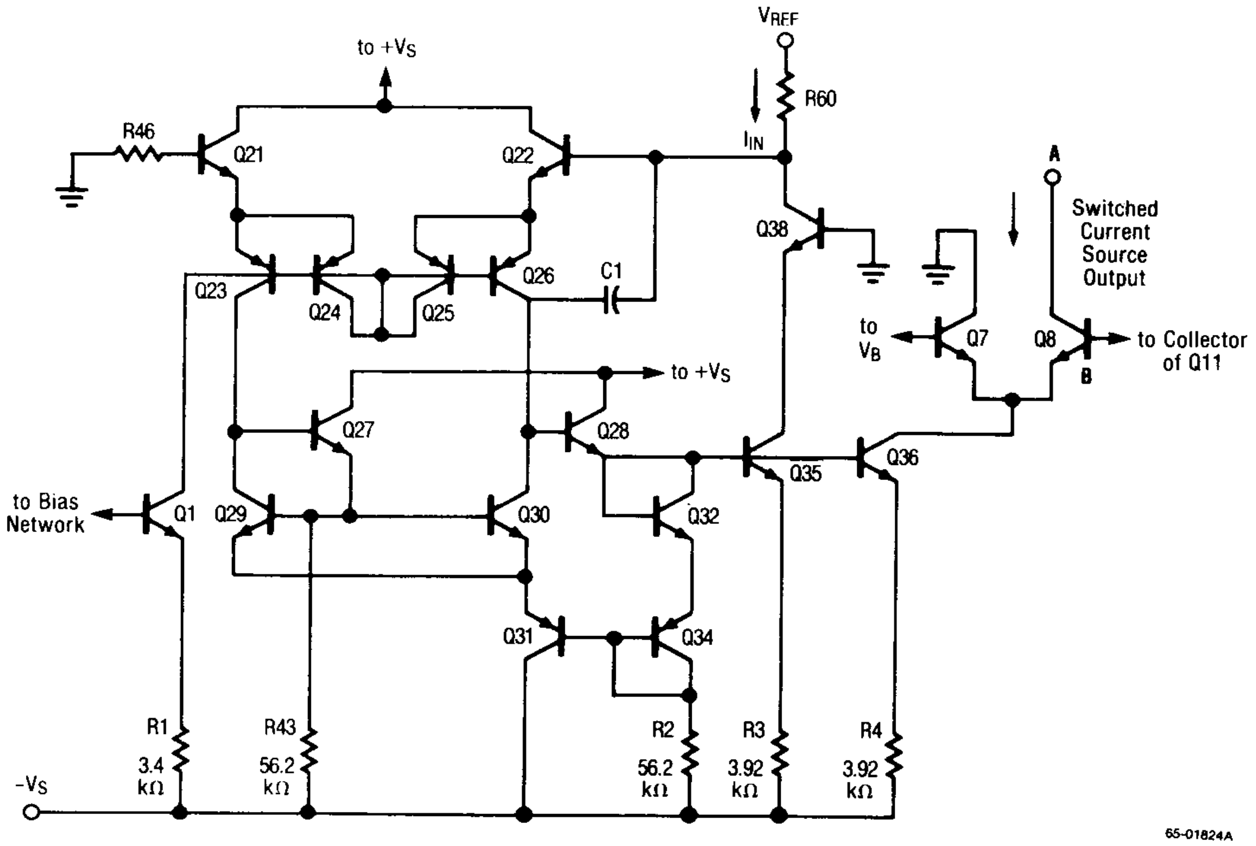

Figure 11. Switched Current Source (Detail)