REVISIONS				
LTR	DESCRIPTION		DATE (YR-MO-DA)	APPROVED
A	Add PRESET and CLEAR propagation delays to table I for device types 02 and 04. Change figure 4. Editorial changes throughout.		88/07/22	M.A. Frye
B	Added devices 05 and 06. Changes to table I. Editorial changes throughout.		92/11/02	

REV																				
SHEET																				
REV	B																			
SHEET	15																			

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Ray Monnin	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Dan Di Cenzo	MICROCIRCUIT, HIGH PERFORMANCE CMOS 9-WIDE AND 10-WIDE BUS INTERFACE LATCHES, MONOLITHIC SILICON		
	APPROVED BY N.A.Hauck			
	DRAWING APPROVAL DATE 87-09-10	SIZE A	CAGE CODE 67268	5962-87603
	REVISION LEVEL B	SHEET 1	OF	15

5962-E667-92

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

```
5962-87603            01              K               X
    |                 |               |               |
    |                 |               |               |
____|____        _____|_____     _____|_____     _____|_____
Drawing number   Device type     Case outline    Lead finish per
                 (see 1.2.1)     (see 1.2.2)     MIL-M-38510
```

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	29C841	High performance CMOS 10-wide bus interface latch
02	29C843	High performance CMOS 9-wide bus interface latch
03	29C941	High performance CMOS 10-wide bus interface latch 1/
04	29C943	High performance CMOS 9-wide bus interface latch 1/
05	29C841A	High performance CMOS 10-wide bus interface latch
06	29C843A	High performance CMOS 9-wide bus interface latch

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	Flat package
L	GDIP3-T24 or CDIP4-F24	24	Dual-in-line package
3	CQCC1-N28	28	Square chip carrier

1.3 Absolute maximum ratings.

Supply voltage range	−0.5 V dc to +7.0 V dc
Input voltage range	−0.5 V dc to 6.0 V dc
Output voltage range	−0.5 V dc to 6.0 V dc
Storage temperature range	−65°C to +150°C
Maximum power dissipation P_D	500 mW
DC output diode current:	
Into output	+50 mA
Out of output	−50 mA
DC input diode current:	
Into input	+20 mA
Out of input	−20 mA
DC output current per pin:	
I_{sink}	
Device types 01 - 04	+48 mA (2 x I_{OL})
Device types 05, 06	+100 mA
I_{source}	
Device types 01 - 04	−30 mA (2 x I_{OH})
Device types 05, 06	−100 mA
Total dc ground current	(n x I_{OL} + m x I_{CCT}) mA 2/
Total dc V_{CC}	(n x I_{OL} + m x I_{CCT}) mA 2/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases K, L, and 3	See MIL-STD-1835
Junction temperature (T_J)	+150°C

_____
1/   Not available from an approved source of supply.
2/   N = number of outputs, m = number of inputs.

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) . . . . +4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH}) . . . . 2.0 V dc
Maximum low level input voltage (V_{IL}) . . . . 0.8 V dc
Case operating temperature range (T_C) . . . . -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510   -   Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883   -   Test Methods and Procedures for Microelectronics.
MIL-STD-1835   -   Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103   -   List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ unless otherwise specified		Group A subgroups	Device type	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -15$ mA $V_{IN} = V_{IL}$ or V_{IH}		1,2,3	All	2.4		V
Low level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or V_{IL}		1,2,3	01-04		0.5	V
			$I_{OL} = 32$ mA		05,06			
Input clamp voltage	V_{IC}	$V_{CC} = 4.5 \text{ V}$, $I_{IN} = -18$ mA		1,2,3	All		-1.2	V
Low level input current	I_{IL1}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0.0 \text{ V}$		1,2,3	01-04		-10	μA
					05,06		-5	
	I_{IL2}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0.4 \text{ V}$			01-04		-5	μA
High level input current	I_{IH1}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.7 \text{ V}$		1,2,3	01-04		5	μA
	I_{IH2}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 5.5 \text{ V}$			01-04		10	μA
					05,06		5	
Off-state current	I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 5.5 \text{ V}$		1,2,3	All		10	μA
Off-state current	I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0.0 \text{ V}$		1,2,3	All		-10	μA
Short circuit output current	I_{SC}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0.0 \text{ V}$ 1/		1,2,3	All	-60		mA
Static supply current	I_{CCQ}	$V_{CC} = 5.5 \text{ V}$ outputs open	$V_{IN} = 5.5 \text{ V}$ or 0.0 V	1,2,3	01-04		160	μA
					05-06		1.5	mA
	I_{CCT}		$V_{IN} = 3.4 \text{ V}$ Data input		All		1.5	mA/bit
			$\overline{OE}$,LE		01,03 05		3.0	mA/bit
			$\overline{OE}$,LE $\overline{PRE}$,$\overline{CLR}$		02,04 06		3.0	mA/bit

See footnotes at end of table.

TABLE I. __Electrical performance characteristics__ - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance	C_{IN}	See 4.3.1c	4	All		16	pF
Output capacitance	C_{OUT}	See 4.3.1c	4	All		20	pF
Functional testing		See 4.3.1d	7,8	All			
Propagation delay data (Di) to Yi (LE = HIGH)	t_{PLH1}	See figure 4 C_L = 50 pF, R_1 = 500Ω, R_2 = 500Ω	9,10,11	01-04		14	ns
				05,06		8.5	
Propagation delay data (Di) to Yi (LE = HIGH)	t_{PHL1}		9,10,11	01-04		14	ns
				05,06		8.5	
Propagation delay latch enable (LE) to Yi	t_{PLH2}		9,10,11	01-04		14	ns
				05,06		9	
Propagation delay latch enable (LE) to Yi	t_{PHL2}		9,10,11	01-04		14	ns
				05,06		9	
Propagation delay preset to Yi	t_{PLH3}		9,10,11	02,04		15	ns
				06		11	
Propagation delay preset to Yi	t_{PHL3}		9,10,11	02,04		15	ns
				06		11	
Propagation delay clear to Yi	t_{PLH4}		9,10,11	02,04		14	ns
				06		12	
Propagation delay clear to Yi	t_{PHL4}		9,10,11	02,04		14	ns
				06		12	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C $\leq T_C \leq$ +125°C 4.5 V $\leq V_{CC} \leq$ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Propagation delay output enable (OE) to Yi	t_{ZH}	See figure 4 C_L = 50 pF, R_1 = 500Ω, $\bar{R}_2$ = 500Ω	9,10,11	01-04		14	ns
				05,06		9.5	
Propagation delay output enable (OE) to Yi	t_{ZL}		9,10,11	01-04		14	ns
				05,06		13	
Propagation delay output disable (OE) to Yi	t_{HZ}		9,10,11	01-04		14	ns
				05,06		8.5	
Propagation delay output disable (OE) to Yi	t_{LZ}		9,10,11	01-04		14	ns
				05,06		8.5	
Data (Di) to LE setup time	t_s		9,10,11	01-04	3		ns
				05,06	2.5		
Data (Di) to LE hold time	t_h		9,10,11	01-04	4		ns
				05,06	2.5		
LE pulse width	t_{PWH}		9,10,11	01-04	9		ns
				05,06	4		
Preset to LE recovery time	t_{REC}		9,10,11	02,04 06	4		ns
Clear to LE recovery time	t_{REC}		9,10,11	02,04 06	3		ns
Preset pulse width	t_{PWL}		9,10,11	02,04	12		ns
				06	4		
Clear pulse width	t_{PWL}		9,10,11	02,04	12		ns
				06	4		

1/ Not more than one output shorted at a time. Duration should not exceed 100 ms.

Device types 01 and 05

Case outlines K and L

$\overline{OE}$	1 ●	24	V_{CC}
D_0	2	23	Y_0
D_1	3	22	Y_1
D_2	4	21	Y_2
D_3	5	20	Y_3
D_4	6	19	Y_4
D_5	7	18	Y_5
D_6	8	17	Y_6
D_7	9	16	Y_7
D_8	10	15	Y_8
D_9	11	14	Y_9
GND	12	13	LE

Device types 01 and 05

Case outline 3

D_1 D_0 $\overline{OE}$ NC V_{CC} Y_0 Y_1
4 3 2 1 28 27 26

D_2	5	25	Y_2
D_3	6	24	Y_3
D_4	7	23	Y_4
NC	8	22	NC
D_5	9	21	Y_5
D_6	10	20	Y_6
D_7	11	19	Y_7

12 13 14 15 16 17 18

D_8 D_9 GND NC LE Y_9 Y_8

Device types 02 and 06

Case outlines K and L

$\overline{OE}$	1 ●	24	V_{CC}
D_0	2	23	Y_0
D_1	3	22	Y_1
D_2	4	21	Y_2
D_3	5	20	Y_3
D_4	6	19	Y_4
D_5	7	18	Y_5
D_6	8	17	Y_6
D_7	9	16	Y_7
D_8	10	15	Y_8
$\overline{CLR}$	11	14	$\overline{PRE}$
GND	12	13	LE

Device types 02 and 06

Case outline 3

D_1 D_0 $\overline{OE}$ NC V_{CC} Y_0 Y_1
4 3 2 1 28 27 26

D_2	5	25	Y_2
D_3	6	24	Y_3
D_4	7	23	Y_4
NC	8	22	NC
D_5	9	21	Y_5
D_6	10	20	Y_6
D_7	11	19	Y_7

12 13 14 15 16 17 18

D_8 $\overline{CLR}$ GND NC LE $\overline{PRE}$ Y_8
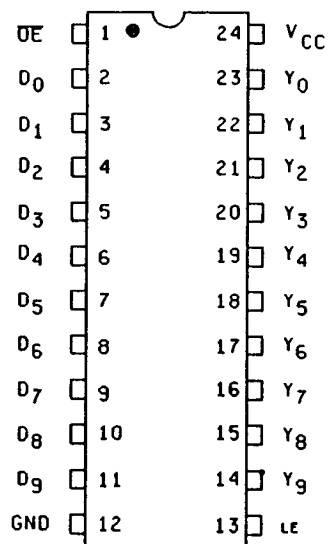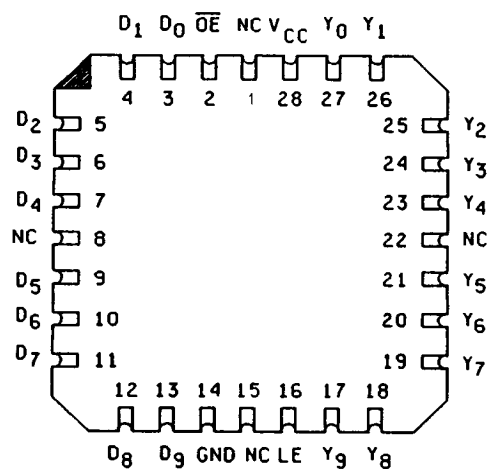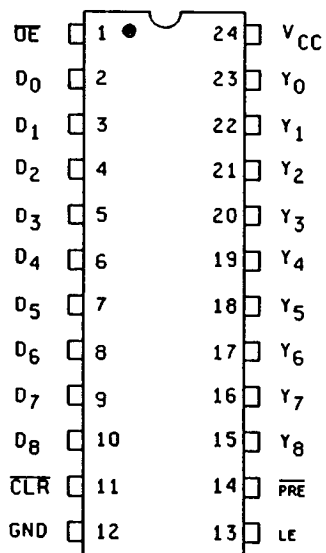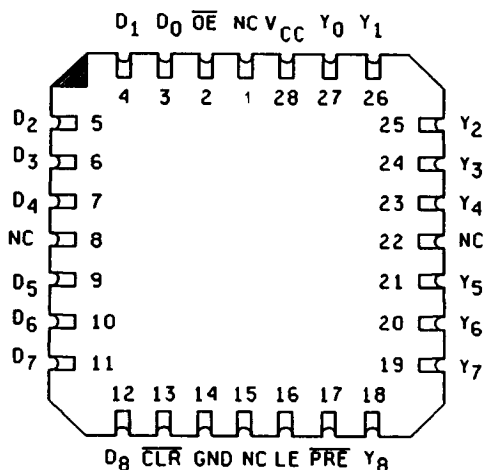
FIGURE 1. Terminal connections.

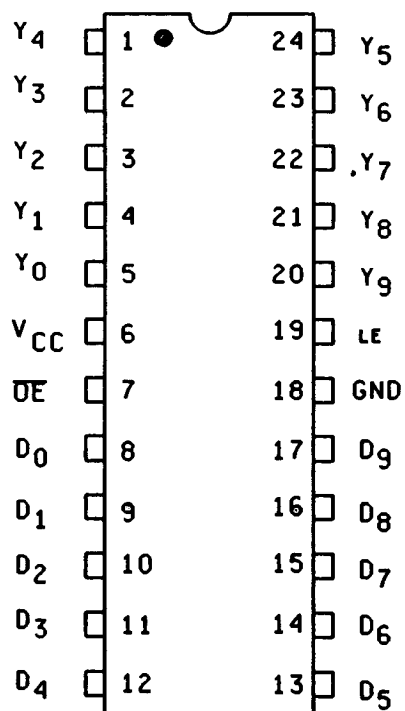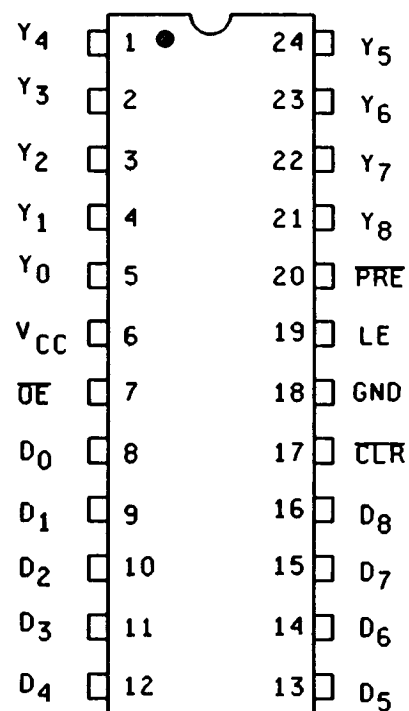| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87603
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Device type 03

Case outline L

```
        ┌───┐ ∪ ┌───┐
 Y4 ──┤ 1 ●     24 ├── Y5
 Y3 ──┤ 2        23 ├── Y6
 Y2 ──┤ 3        22 ├── .Y7
 Y1 ──┤ 4        21 ├── Y8
 Y0 ──┤ 5        20 ├── Y9
 VCC ─┤ 6        19 ├── LE
 OE ──┤ 7        18 ├── GND
 D0 ──┤ 8        17 ├── D9
 D1 ──┤ 9        16 ├── D8
 D2 ──┤ 10       15 ├── D7
 D3 ──┤ 11       14 ├── D6
 D4 ──┤ 12       13 ├── D5
        └────────────┘
```

Device type 04

Case outline L

```
        ┌───┐ ∪ ┌───┐
 Y4 ──┤ 1 ●     24 ├── Y5
 Y3 ──┤ 2        23 ├── Y6
 Y2 ──┤ 3        22 ├── Y7
 Y1 ──┤ 4        21 ├── Y8
 Y0 ──┤ 5        20 ├── PRE
 VCC ─┤ 6        19 ├── LE
 OE ──┤ 7        18 ├── GND
 D0 ──┤ 8        17 ├── CLR
 D1 ──┤ 9        16 ├── D8
 D2 ──┤ 10       15 ├── D7
 D3 ──┤ 11       14 ├── D6
 D4 ──┤ 12       13 ├── D5
        └────────────┘
```

FIGURE 1. Terminal connections – Continued.

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Devices 01, 03, and 05

Inputs			Internal	Outputs	Function
$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	
H	X	X	X	Z	Hi-Z
H	H	L	H	Z	Hi-Z
H	H	H	L	Z	Hi-Z
H	L	X	NC	Z	Latched (Hi-Z)
L	H	L	H	L	Transparent
L	H	H	L	H	Transparent
L	L	X	NC	NC	Latched

FIGURE 2. Truth tables.

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Devices 02, 04, and 06

Inputs					Internal	Output	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{QE}$	LE	D_i	Q_i	Y_i	
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	H	L	H	Transparent
H	H	L	H	L	H	L	Transparent
H	H	L	H	X	NC	NC	Latched
H	L	L	X	X	L	H	Preset
L	H	L	X	X	H	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	L	Z	Latched (Hi-Z)

H = High   NC = No change
L = Low   Z = High impedance
X = Don't care

FIGURE 2. Truth tables - Continued.

Device types 01, 03, and 05

Device types 02, 04, and 06
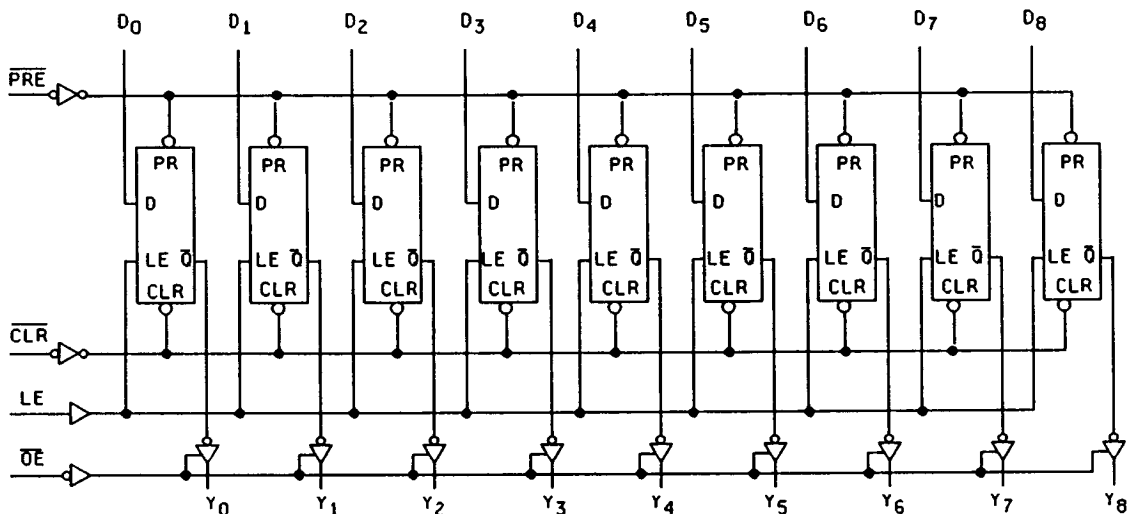
FIGURE 3. Logic diagrams.

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+7 V

R₁

S

FROM OUTPUT
UNDER TEST

C_L   R₂

Parameter	S Position
t_{PLH}	Open
t_{PHL}	Open
t_{HZ}	Open
t_{ZH}	Open
t_{LH}	Closed
t_{ZL}	Closed
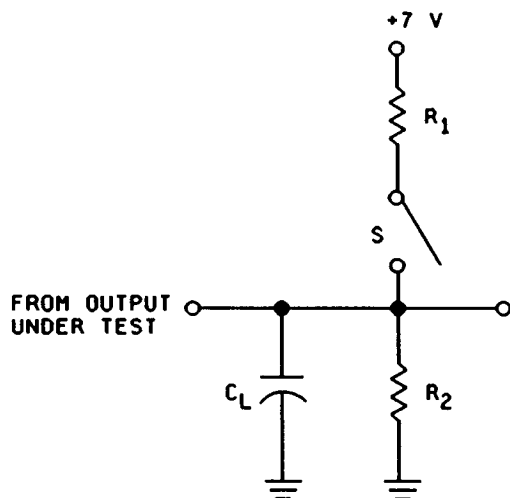
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS

SWITCH POSITION FOR
PARAMETER TESTING

SWITCHING CIRCUITS

Setup and hold times

DATA
INPUT   3.0 V
               1.5 V
               0 V

t_S t_h

LATCH
INPUT   3.0 V
               1.5 V
               0 V
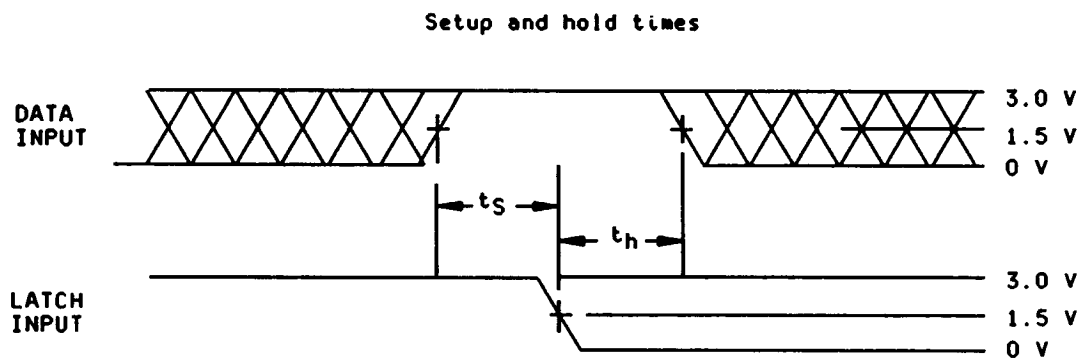
SWITCHING WAVEFORM

NOTES:

1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

FIGURE 4. Switching circuits and waveforms.

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Enable and disable times
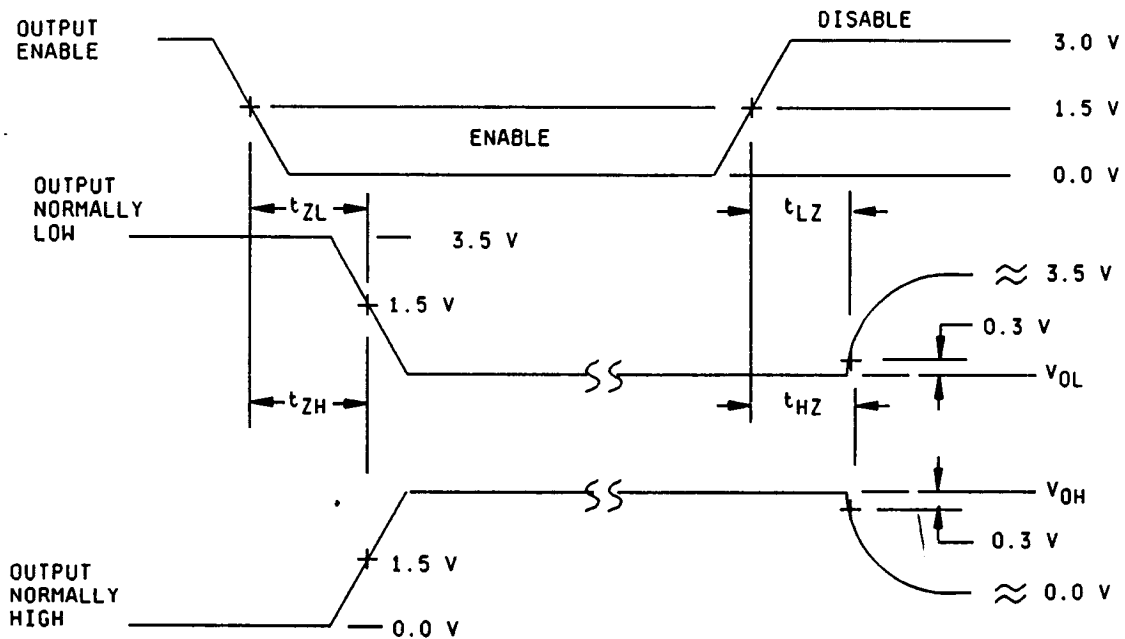
Propagation delay
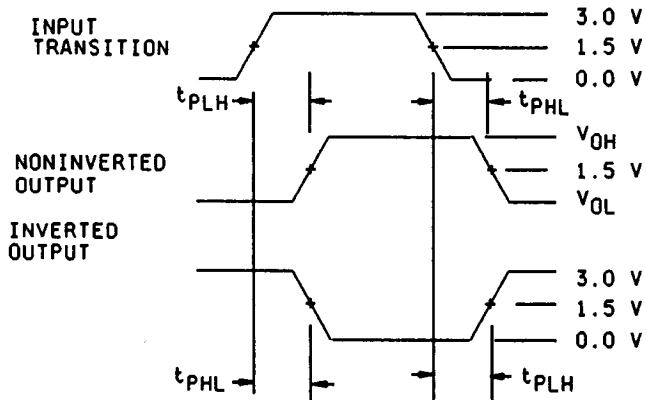
Pulse width
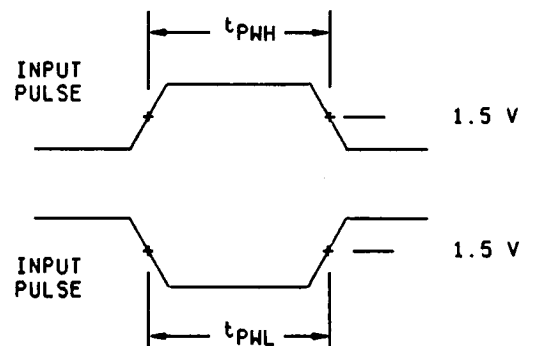
NOTE: Pulse generator for all pulses rate ≤ 1.0 MHz . Z_o = 50Ω
t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 4. Switching circuits and waveforms - Continued.

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3.5 <u>Marking</u>. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 <u>Notification of change</u>. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 <u>Verification and review</u>. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

    a. Burn-in test, method 1015 of MIL-STD-883.

        (1) Test condition A, C or D. The test circuit shall be maintained by the manufacturer under document
revision   level control and shall be made available to the preparing or acquiring activity upon request.
The test   circuit shall include the requirements for inputs, outputs, biases, and power dissipation, as
                applicable, in accordance with the specified purpose of method 1015.

        (2) T_A = +125°C, minimum.

    b. Interim and final electrical test parameters shall be as specified in table II herein, except interim
       electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. <u>Electrical test requirements</u>.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

    * PDA applies to subgroup 1.

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4.3 <u>Quality conformance inspection</u>. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 <u>Group A inspection</u>.

    a. Tests shall be as specified in table II herein.

    b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

    .c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

    d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 <u>Groups C and D inspections</u>.

    a. End-point electrical parameters shall be as specified in table II herein.

    b. Steady-state life test conditions, method 1005 of MIL-STD-883.

        (1) Test condition A, C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

        (2) T_A = +125°C, minimum.

        (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 <u>Comments</u>. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 <u>Approved sources of supply</u>. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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