silicon systems®
A TDK Group Company

SSI 67F687
Engine Interface Peripheral

Preliminary Data

July 1992

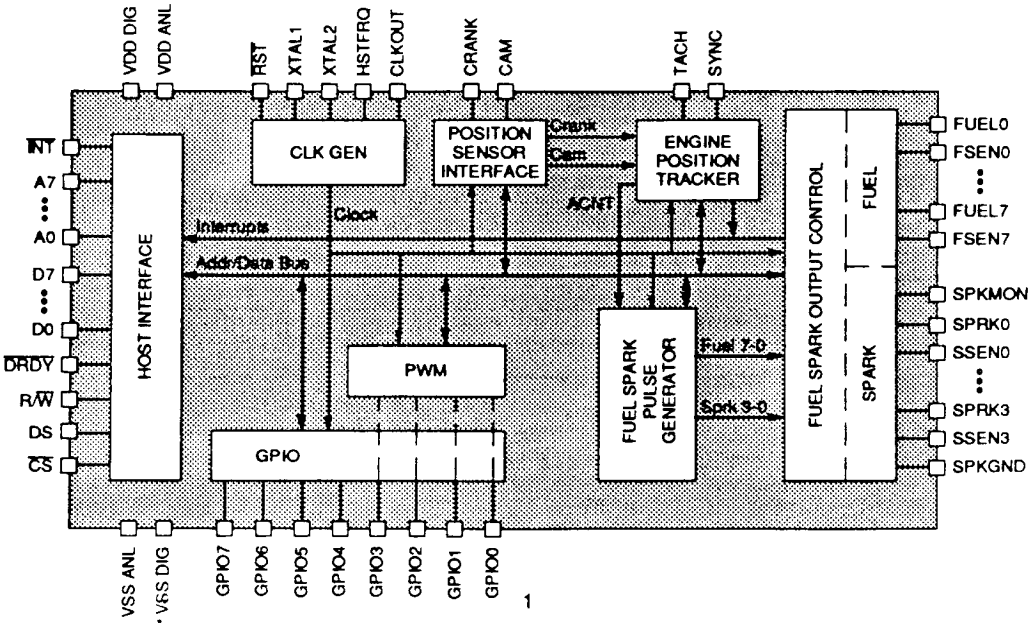
DESCRIPTION

The F687 is a high performance MSIC® (Mixed Signal Integrated Circuit) designed to work with a microprocessor in an engine management system. Using two sensor inputs (crank and cam), the F687 tracks engine position through one or two complete revolutions with a resolution of 0.25 degrees. Designed to be flexible, the F687 will accept a variety of sensor types and pulse patterns. It generates ignition and injection output pulses based on position and time parameters supplied by the host microprocessor, relieving it of many of the real time interrupt routines associated with these tasks. These outputs can directly drive power devices to actuate automotive ignition coils and fuel injectors. A sense input from each output device allows individual diagnostics, short circuit protection and ignition coil current limit. A timer, which measures coil charge time at the ignition sense inputs, enhances closed loop dwell control. Communication with a host microprocessor is through a parallel data and address bus. A general purpose parallel I/O port offers level sensitive input and output capability, in addition to edge detect inputs and PWM outputs.

FEATURES

- Engine control applications
- 2 or 4 cycle engines
- Parallel microprocessor bus for control
- Configurable for a variety of sensor patterns
- Variable Reluctance or Hall Effect sensor inputs
- Engine position angle counter
- 4 ignition outputs (8 individual spark advance values)
- 8 injection outputs
- Dwell timer
- Ignition coil current limit (for use with external power transistors)
- Injector driver short circuit protection
- Diagnostics
- 8 programmable I/O lines
- PMW outputs
- Edge detect inputs
- On chip oscillator with buffered 8 MHz/31.25 KHz output
- +5V operation
- CMOS technology for low power consumption
- Operating temperature range -40 to +125°C
- 68-pin PLCC

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The 67F687 Engine Interface Peripheral (EIP), is designed to track engine position from crank and cam sensor inputs and generate output pulses for up to eight fuel injectors and eight ignition spark plugs (multiplexed to four output pins). It is intended to be used with a host microprocessor which defines the engine configuration and calculates the position and time dependent parameters needed to generate fuel and spark pulses. The EIP acts as a memory at the host interface and outputs a single interrupt to the host.

The EIP is divided into modular blocks. There are two analog blocks (PSI and FSOC) and six digital blocks (CLKGEN, EPT, FSPG, PWM, GPIO and HOSTINT). The analog blocks provide the digital blocks with an interface to the engine sensors and ignition/injector drivers. The digital blocks perform engine position tracking, output pulse generation, pulse width modulation, general purpose I/O, clock generation and the host interface.

The Position Sensor Interface (PSI) converts crank and cam sensor inputs to digital signals for use by the EPT. Programmable registers control the input threshold levels, hysteresis amount and allows the use of time (frequency) dependent hysteresis. This allows the PSI to be tailored to the particular type of sensor being used, whether variable reluctance or Hall effect type.

The Engine Position Tracker (EPT) can be configured through internal RAM to track a large number of crank and cam sensor configurations. Once the EPT has attained synchronization with the engine, it maintains a monotonic angle count with a resolution of 0.25 degrees. The angle count and tracking status are available to the host through memory mapped registers. The EPT generates interrupts to the host when it attains or loses synchronization. Digital TACH and SYNC outputs also provide engine speed and position clocks.

The Fuel Spark Pulse Generator (FSPG) generates digital pulses that control fuel and ignition. The host controls the mode used to generate these pulses. In the normal mode, spark is controlled by writing the angle at which charging of the coil is to begin and the angle at which the spark is to occur. Fuel is controlled by writing the angle at which the fuel injector is to turn on and the time duration of the fuel pulse. In direct mode, the host can generate the output pulses through writes to memory mapped registers. The host can also execute a hard shutdown of all pulses by writing to a control register.

The Fuel Spark Output Controller (FSOC) converts the digital pulses generated by the FSPG into analog outputs. It performs a current limit function for external ignition drivers and contains an ignition dwell timer. The FSOC can also be configured to end a spark pulse when the coil current reaches a predetermined threshold. It monitors the external injector drivers for faults and can turn off pulses to protect these drivers. The FSOC also performs diagnostic tests on both fuel and spark outputs and generates interrupts to the host when a fault condition is indicated.

The General Purpose I/O (GPIO) provides eight user configurable I/O pins. As inputs, four are configurable as either level or edge sensitive and four are level sensitive only. As outputs, four are configurable as pulse width modulated or direct write outputs and four are direct write outputs only.

The Pulse Width Modulator (PWM) provides four pulse width modulated outputs for the GPIO. The outputs are grouped in two pairs. Each pair shares a common output frequency with individual duty cycle control. There are eight programmable output frequencies from 20 Hz to 651 Hz.

The Host Interface (HOSTINT) acts as a buffer between the asynchronous external memory bus and the internal bus. It also provides the interrupt output, interrupt register and interrupt control.

The Clock Generator (CLKGEN) contains the crystal oscillator circuit. It supplies all the necessary internal clocks as well as an external clock at the CLKOUT pin.

INTERNAL REGISTERS AND RAM

The 67F687 uses both static RAM and registers to store data. Memory on the EIP falls into one of two categories: (1) memory that must be accessable during normal operation and (2) EPT configuration memory that is loaded only once during power up.

To allow more than 256 memory locations using eight address pins, memory is divided into two pages. Memory locations 00 through BF HEX can be mapped to two different locations depending on the value of bit 0 in the

Global Configuration Register (GCR) - location F6 HEX. This allows a maximum of 448 locations. When GCR bit 0 = 0, the memory necessary for normal operation (FSPG RAM) is accessed. When GCR bit 0 = 1, the EPT configuration memory is accessed. These registers configure the F687 for the particular engine and sensors, and must be initialized by the host microprocessor before engine position tracking can begin. In normal operation, the EPT configuration registers are only written to once on power up, and should not be modified after initialization without first disabling the outputs.

Whenever GCR bit 0 = 1, the EPT is inhibited from attaining sync and will be forced out of sync if it attained it previously.

To differentiate the two pages of memory, addresses of locations on page 1 described in this document will be preceded by a "1" (1xx for page 1 locations and xx for page 0 locations).

Memory locations C0 through FF HEX access only one set of registers and are unaffected by the value of GCR bit 0. During reset GCR bit 0 is set to "1".

RESET

An external logic level low at the RST pin places the 67F687 in a defined initial state. All registers are set to known values. RAM values are unknown and should not be used until initialized. All output pulses are turned off. All GPIO pins are configured as level sensitive inputs. The PWM is configured to output no pulses. All interrupts are off and masked. The memory page bit of the GCR (location F6) is set to "1".

After reset the 67F687 internal RAM and registers cannot be accessed for 2 µs (sixteen 8 MHz clock pulses).

CLOCK GENERATOR (CLKGEN)

The CLKGEN uses a 16 MHz crystal at the XTAL1 and XTAL2 pins to generate the required internal clocks for the F687. Alternatively, XTAL1 can be driven by an external 16 MHz clock. If this is done XTAL2 should be left open. The CLKOUT pin provides a buffered output clock whose frequency depends upon the logic level at the HSTFRQ pin. If HSTFRQ=0, CLKOUT is 8 MHz; if HSTFRQ=1, CLKOUT is 31.25 KHz.

A reset will inhibit the internal clocks, but has no effect on the external clock at the CLKOUT pin. Figure 4 shows some typical external circuits for the Clock Generator.

HOST MICROPROCESSOR INTERFACE (HOSTINT)

The HOSTINT makes the 67F687 look like external memory to a host microprocessor. It supports non-multiplexed address and data buses. Both address and data are eight bits wide. Chip select bar ($\overline{CS}$), data strobe (DS) and read/write bar (R/$\overline{W}$) inputs are used to control the bus interface.

The DS pin can either be data strobe (DS) or data strobe bar ($\overline{DS}$) dependent on the logic level at the HSTFRQ pin. If HSTFRQ=0, DS is inverted internally. For the remainder of this description it is assumed that HSTFRQ=1. If HSTFRQ=0 replace "DS=0" with "DS=1" and vice-versa and replace "rising edge of DS" with "falling edge of DS" and vice-versa.

A data ready bar ($\overline{DRDY}$) output is available for use with hosts that can support extended bus cycles. A single interrupt bar ($\overline{INT}$) pin is also provided to the host. Both of these are open drain outputs.

The data bus pins (D0-D7) are outputs when R/$\overline{W}$=1 AND DS=0 AND $\overline{CS}$=0. They are inputs otherwise.

During a read cycle, the output data will be valid 500 nsec after DS=0. When DS=0 for less than this time and the host cannot use $\overline{DRDY}$ to extend its memory cycle, the host must execute multiple read cycles to interface with the EIP. For this condition, a host must read a location once to start the EIP internal read cycle. The same location must then be read a second time. There must be at least 500 nsec between the falling edge of DS during the first read and the rising edge of DS during the second read to get valid data. There can be no other reads or writes to the F687 between the double read.

If the host can use $\overline{DRDY}$, the R/$\overline{W}$ input must be valid for the entire duration of $\overline{CS}$=0. For a read, $\overline{DRDY}$=0 as soon as the data is valid and remains low until DS=1.

During a write cycle, the address inputs are latched by the falling edge of $\overline{CS}$ and DS. External data is latched by the rising edge of DS. Writes can occur no less than 500 nsec apart. For a write, $\overline{DRDY}$ goes low as soon as $\overline{CS}$=0 and and stays low until the rising edge of DS.

PIN DESCRIPTION

GENERAL

NAME	TYPE	DESCRIPTION
VddD	PWR	+5V Power supply for digital circuits.
VddA	PWR	+5V Power supply for analog circuits.
VssD	PWR	GROUND reference for digital circuits.
VssA	PWR	GROUND reference for analog circuits.
$\overline{\text{RESET}}$	I	RESET. Active low input turns off all outputs and initializes the 67F687 to a known state.

CLOCK GENERATOR

XTAL1, XTAL2	I	These pins are for the external 16 MHz crystal to generate the internal 8 MHz clock. An external clock (16 MHz) can also be input at XTAL1 with XTAL2 open.
CLKOUT	O	Buffered clock signal to microprocessor. Either 8 MHz or 31.25 KHz depending on state of HSTFRQ input.
HSTFRQ	I	Level at this pin determines the clock frequency at CLKOUT and the sense of DS.

HOST INTERFACE

A0:7	I	HOST ADDRESS LINES. These are used to address the internal registers of the 67F687.
$\overline{\text{CS}}$	I	CHIP SELECT. Active low signal, allows the internal registers of the 67F687 to be accessed.
D0:7	I/O	HOST DATA LINES. These are used to read and write to the 67F687 internal RAM and registers.
DS	I	DATA STROBE. Active low or high depending on state of HSTFRQ input. Indicates valid data on D0:7.
R/$\overline{\text{W}}$	I	READ/WRITE. Determines direction of data flow on D0:7.
$\overline{\text{DRDY}}$	O	DATA READY. Active low signal used with certain microprocessors that support extended bus cycles to indicate that data requested is available to be read.
$\overline{\text{INT}}$	O	INTERRUPT. Active low output, indicates interrupt request to microprocessor.

PSI

NAME	TYPE	DESCRIPTION
CRANK	I	Crankshaft sensor input.
CAM	I	Camshaft sensor input.
TACH	O	Output at this pin is either TACH or the conditioned CRANK sensor signal, depending on the contents of the EPTRST register.
SYNC	O	Output at this pin is either SYNC or the conditioned CAM sensor signal, depending on the contents of the EPTRST register.

FSOC

SPRK0:4	O	Spark outputs to ignition coil drivers.
SSEN0:4	I	Spark sense inputs used to detect current through ignition coil by measuring voltage across current sense resistor. Used for current limit, autofire and dwell timer threshold.
SPKGND	I	Ground reference for SSEN0:4. Should be connected directly to low side of current sense resistors.
SPKMON	I	Input pin to detect voltage spike generated when ignition coil is turned off (for diagnostics).
FUEL0:7	O	Fuel outputs to fuel injector drivers.
FSEN0:7	I	Fuel sense inputs from injector driver, used for short circuit protection and diagnostics on FUEL outputs.

GPIO

GPIO0:7	I/O	General purpose input or output pins. Four pins can also be configured as PWM outputs and the other four can be edge detect inputs.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond absolute maximum ratings may permanently damage the device. All voltages are referenced to logic ground unless otherwise specified. Current flowing into the integrated circuit is positive.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage	-digital VddD	Referenced to VssD	-0.5		7.0	V
	-analog VddA	Referenced to VssA	-0.5		7.0	V
Input Current	Iin	All I/O Pins	-10		+10	mA
Input Voltage	Vin	All Inputs, referenced to VssD or VssA except FSEN, SPKMON	-.05		Vdd = +.5	V
Operating Temperature	To	Ambient	-40		+125	°C
Storage Temperature	Ts	Ambient	-55		+150	°C

RECOMMENDED OPERATING CONDITIONS

Unless otherwise specified, VddD = VddA = 5.0V, T(ambient) = 25 °C.

POWER SUPPLY

Supply Voltage	-digital VddD	Referenced to VssD	4.5	5.0	5.5	V
	-analog VddA	Referenced to VssA	4.5	5.0	5.5	V
Delta Supply Voltage		VddD - VddA	-.3	0.0	.3	V
Supply Current	Idd			18.0	25.0	mA
Clock Frequency				16.0		MHz
Bypass Capacitor Both power supplies				0.1		µF

HOST INTERFACE - INPUTS

(DS, $\overline{CS}$, R/$\overline{W}$, A(7:0), $\overline{RESET}$, D(7:0))

Input Voltage Range	Vin		-0.5		Vdd	V
Input Current	Iin	0V < Vin < Vdd		25	100	µA
Input Low Voltage	Vil	Referenced to VddD	0		.2xVdd	V
Input High Voltage	Vih	Referenced to VddD	.7xVdd		Vdd	V

HOST INTERFACE - OUTPUTS
(D(7:0))

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage - High	Voh	Io = -2.0mA	Vdd-.4			V
Output Voltage - Low	Vol	Io = +2.0mA			0.4	V

CLOCK FREQUENCY - OUTPUTS
(CLKOUT, SYNC, TACH)

Clkout Frequency - 1	Fo1	HSTFRQ(Pin 26) = Vdd		31.25		kHz
Clkout Frequency - 2	Fo2	HSTFRQ(Pin 26) = 0		8.0		MHz

CONTROL TIMING - CLOCK/RESET
(XTAL1, XTAL2, HSTFRQ, $\overline{\text{RESET}}$)

Frequency of Operation	Fosc	Clock at Pin 26		16.0		MHz
External Clock Option	Fc	Crystal oscillator at Xtal1, Xtal2		16.0		MHz
Crystal Oscillator Startup Time	Tst				10	ms

GENERAL PURPOSE I/O
(GPIO(7:0), $\overline{\text{DRDY}}$, $\overline{\text{INT}}$)

Input Low Voltage	Vil	Referenced to VddD	0		.2xVdd	V
Input High Voltage	Vih	Referenced to VddD	.7xVdd		Vdd	V
PWM output frequency	Fpwm	Programmable	20		651	Hz
Output voltage - low $\overline{\text{DRDY}}$, $\overline{\text{INT}}$ pins	Vol	Referenced to VddD Open Drain Outputs Io = +2.0 mA	0		.1xVdd	V

ELECTRICAL SPECIFICATIONS (continued)

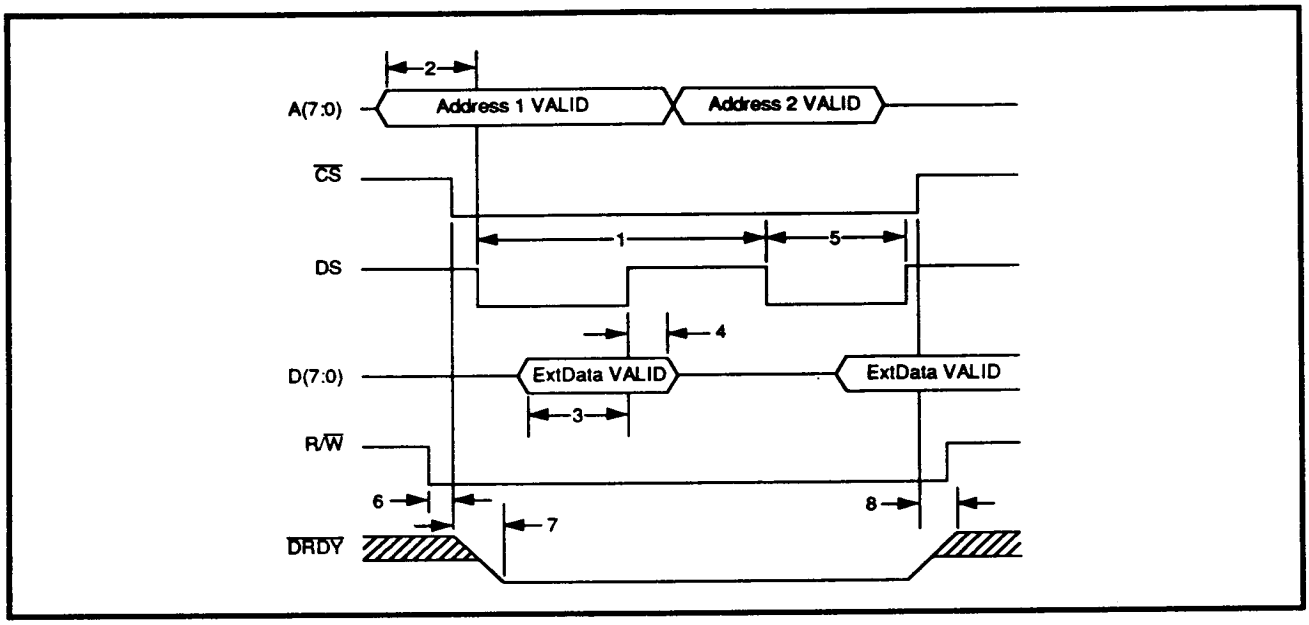


FIGURE 1: Write Cycle

CONTROL TIMING - WRITE
($\overline{CS}$, DS, A(7:0), D(7:0), R/$\overline{W}$), (HSTFRQ = 1)

(1) Data Strobe Period	Tdsb	Between falling edges	500			ns
(2) Address setup time	Tas	Before $\overline{CS}$ = 0 AND DS = 0	5			ns
(3) Data valid setup	Tdvs	DATA valid to DS = 1 OR $\overline{CS}$ = 1	10			ns
(4) DATA hold time	Tdh	From $\overline{CS}$ or DS = 1	5			ns
(5) DS pulse width	Tdsp	Minimum width	200			ns
(6) R/$\overline{W}$ setup time	Trds	Before $\overline{CS}$ falling edge	5			ns
(7) $\overline{DRDY}$ active time	Twra	From $\overline{CS}$ falling edge			10	ns
(8) $\overline{DRDY}$ inactive	Tri	From $\overline{CS}$ rising edge			10	ns

If HSTFRQ = 0, DS is inverted.

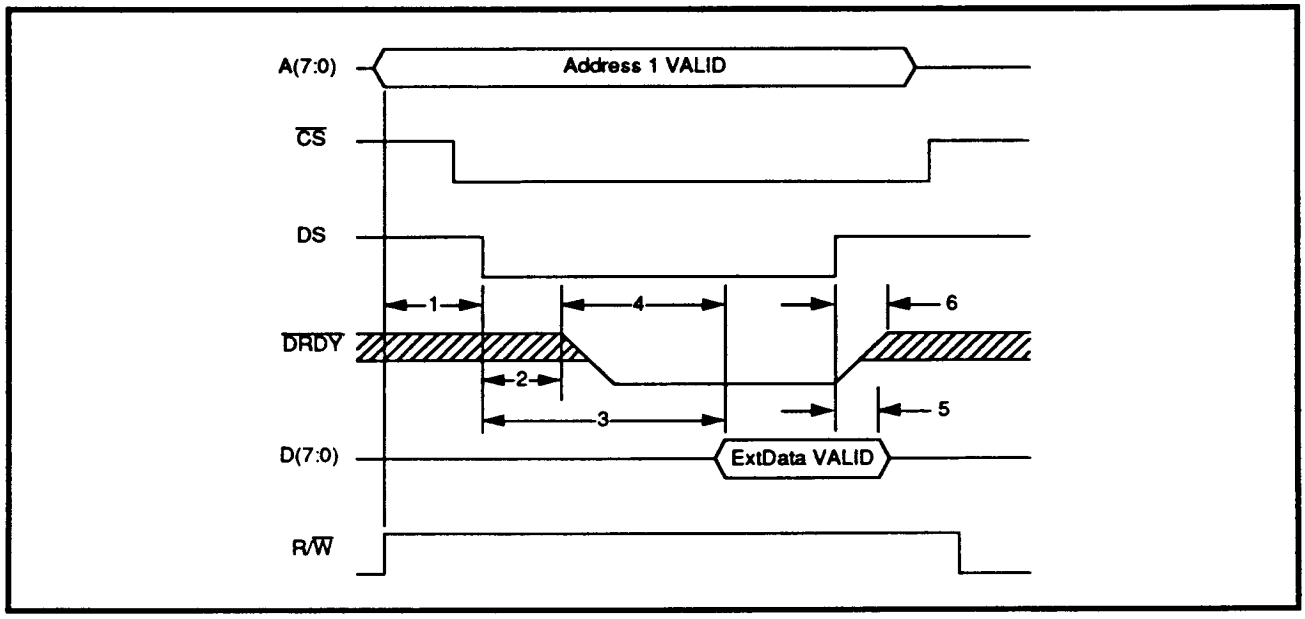


FIGURE 2: Read Cycle Applying $\overline{\text{DRDY}}$ Output

CONTROL TIMING - READ W/$\overline{\text{DRDY}}$
($\overline{\text{CS}}$, DS, A(7:0), D(7:0), R/$\overline{\text{W}}$, $\overline{\text{DRDY}}$), (HSTFRQ = 1)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
(1) Address setup time	Tas	Before DS = 0	5			ns
(2) $\overline{\text{DRDY}}$ active delay	Trra	DS = 0 and $\overline{\text{CS}}$ = 0 to time $\overline{\text{DRDY}}$ valid	320		445	ns
(3) DATA valid delay	Tvd	DS = 0 and $\overline{\text{CS}}$ = 0 to time DATA valid	320		450	ns
(4) DRDYb to DATA	Tde				5	ns
(5) DATA inactive	Trdi	From DS = 1			5	ns
(6) $\overline{\text{DRDY}}$ inactive	Tri	From DS = 1			5	ns

If HSTFRQ = 0, DS is inverted.

ELECTRICAL SPECIFICATIONS (continued)

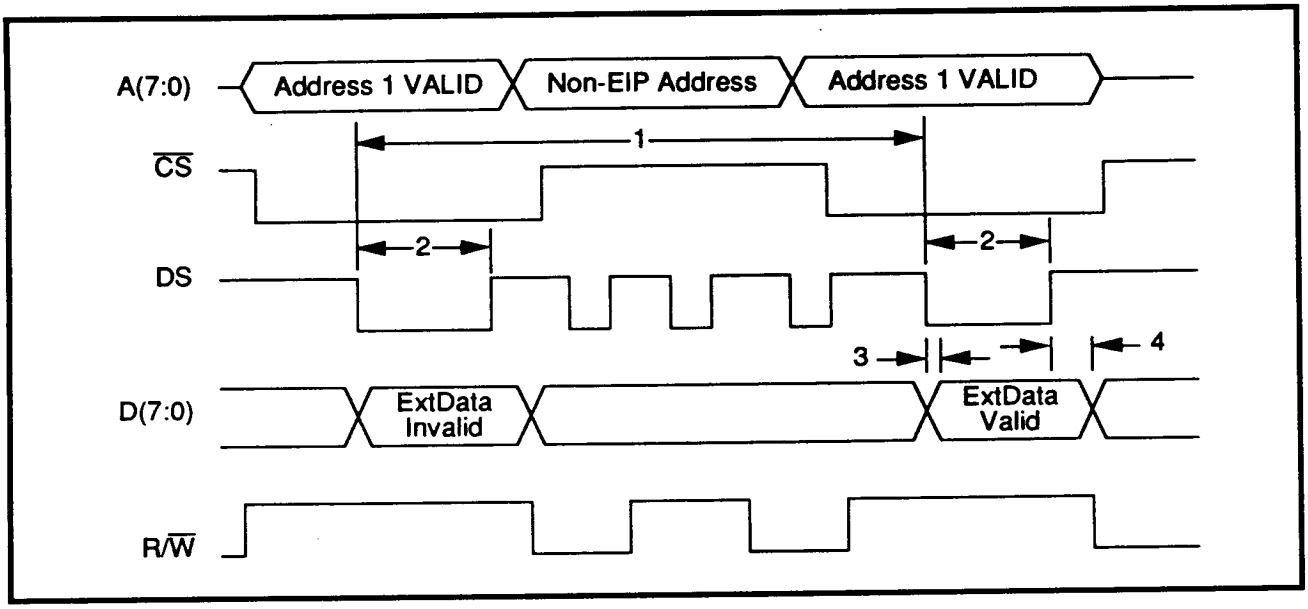


FIGURE 3: Multiple Reads

CONTROL TIMING - MULTIPLE READS
($\overline{CS}$, DS, A(7:0), D(7:0)), (HSTFRQ = 1)

(1) DS Period	Tds	Between falling edges	500			ns
(2) DS pulse width -multiple read	Tdsp	From DS falling edge to rising edge	200			ns
(3) DATA active time	Tda	From DS falling edge	5			ns
(4) DATA inactive	Tdi	From DS rising edge			5	ns

If HSTFRQ = 0, DS is inverted.

INPUTS - CRANK AND CAM

DC Voltage Range	VinDC	Steady state range	-0.5		Vdd+.3	V
Input Voltage Range	VinAC		-1		Vdd+1	V
Input Current	Iin	Gnd < Vin < Vdd		25	100	µA
Time Decreasing:						
Input Threshold -low rising	Vtlr	Ctrl bit 6 = 1 bits 2,1,0 = 0		0.15		V
Input Threshold -high rising	Vthr	Ctrl bit 6 = 1 bits 2,1,0 = 0		2.65		V
Input Threshold -low rising	Vtlr	Ctrl bit 6 = 1 bits 2,1,0 = 1		0.25		V
Input Threshold -high rising	Vthr	Ctrl bit 6 = 1 bits 2,1,0 = 1	.7xVdd	.75xVdd		V
Input Threshold falling	Vtf	Ctrl bit 6 = 1		0.0		V

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Threshold decay time Programmable value	Vtd	Ctrl bit 6 = 1	1.024		8.192	ms
Constant value:						
Input Threshold -rising Programmable value	Vptr	Ctrl bit 6 = 0	.125xVdd		Vdd	V
Input Threshold -falling Programmable value	Vptf	Ctrl bit 6 = 0	0.0		.875 x Vdd	V

FUEL OUTPUTS/SENSE
(FUEL(7:0), FSEN(7:0))

Input Threshold - High	Vfh	Vdd = 5.0V		3.33	3.5	V
Input Threshold - Low	Vfl	Vdd = 5.0V	1.5	1.66		V
Output Voltage - High		Iload < 200 µA	Vdd-.5			V
Output Voltage - Low		Iload < 100 µA			0.5	V

SPARK OUTPUT/SENSE
(SPRK(3:0), SSEN(3:0), SPKMON, SPKGND)

Dwell current Threshold	Vdw	Vdd=5.0V	270	300	330	mV
Current limit Threshold	Vcl	Vdd=5.0V	320	350	380	mV
Autofire Threshold	Vaf	Vdd=5.0V	460	500	540	mV
SPKGND Current	Isg	Current out of Pin		270	400	µA
SPKMON Threshold		Vdd=5.0V		3.4		V
Power Supply sensitivity		All Thresholds		20		%/V
Temperature sensitivity		All Thresholds	-200		+200	ppm/°C
Output Voltage - High		Iload = 2.0 mA	Vdd-1			V
Output Voltage - Low		Iload < 100 µA			0.5	V

REGISTER DESCRIPTION

POSITION SENSOR INTERFACE (PSI)

The Position Sensor Interface (PSI) accepts 2 sensor inputs which are used to determine the operating position of an engine. One can indicate crankshaft angle position, and the other camshaft position. These sensors can typically be either Variable Reluctance (VR) or Hall Effect type. Figure 5 shows a typical VR sensor external input circuit. These are conditioned in the 67F687 to provide clean digital pulses to the Engine Position Tracker (EPT).

The circuits for crank and cam sensor conditioning are identical comparators with variable positive and negative switch points. They can be individually configured to optimize the signal processing for the particular type of sensor. The switch points can either be fixed levels (for Hall Effect sensors) or time decreasing (for VR sensors). They are controlled by configuration registers CRKCFG (crank) and CAMCFG (cam) at locations 16C and 16D HEX, respectively. These registers can only be read or written when bit 0 of the GCR (location F6) is a "1". Under normal operation, they would only be configured at power up, along with the EPT registers. The two registers have the same format, shown below.

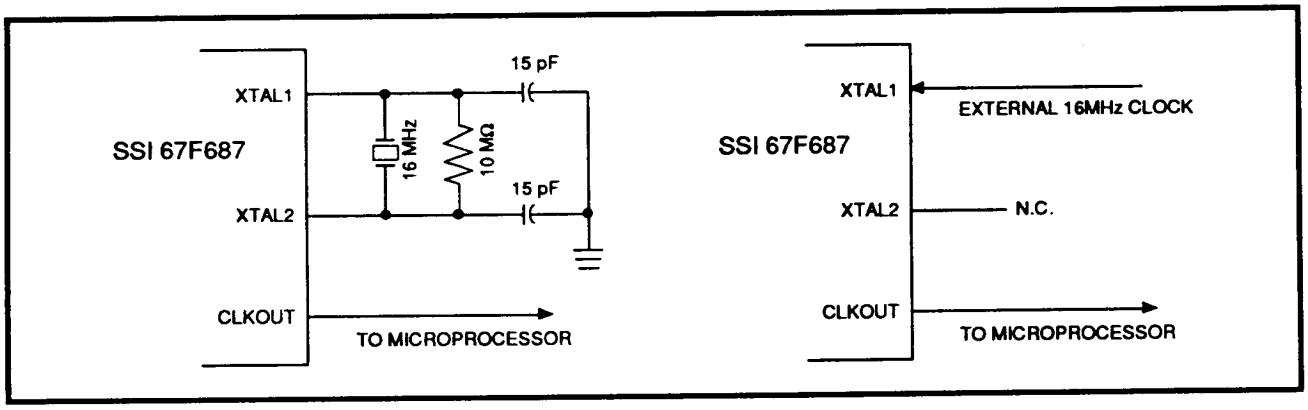


FIGURE 4: Typical Clock Generator Circuits

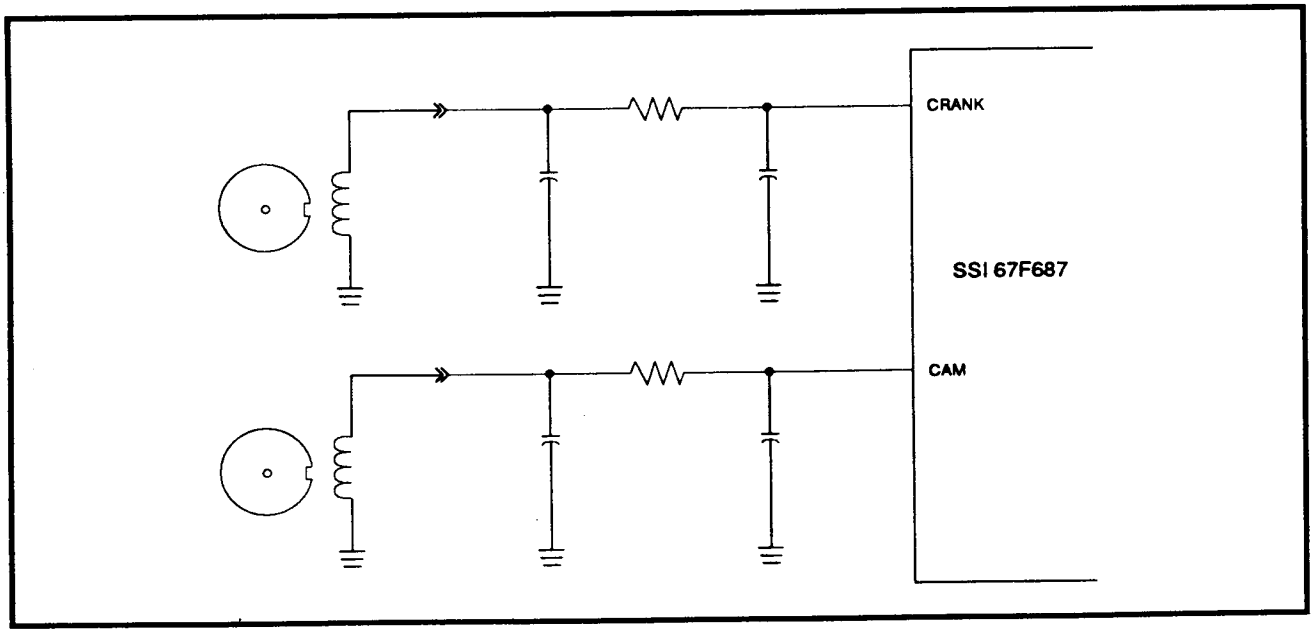


FIGURE 5: Typical EIP VR Sensor External Circuit

CRKCFG AND CAMCFG FORMAT

CRKCFG
Location 16C

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INV	DEC	VTLOW			VTHIGH		

CAMCFG
Location 16D

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INV	DEC	VTLOW			VTHIGH		

Bit 7	INV: Inverts the output of the PSI before it is input to the EPT. 0 = NOT INVERTED, 1 = INVERTED
Bit 6	DEC: Determines whether the positive switch point is fixed or time decreasing. 0 = FIXED SWITCH POINTS, 1 = TIME DECREASING
Bit 5-3	VTLOW: If DEC (bit 6) = 1, this controls the time dependency of the positive switch point. If DEC (bit 6) = 0, this controls the negative switch point.
Bit 2-0	VTHIGH: Controls the level of the positive switch point.

If INV = 0, the PSI signal path is non-inverting from the sensor inputs to the PSI output (EPT input). The EPT acts on rising edges. If INV = 1, the sensor signal will be inverted in the PSI. A falling edge at the sensor inputs will generate a rising edge at the EPT input.

The DEC bit selects either fixed or time decreasing switch points. If fixed switch points are selected (DEC = 0), the remaining bits (VTLOW and VTHIGH) set the negative and positive switch points as shown below.

For DEC = 0	VTLOW			Negative Switch Point
	Bit 5	Bit 4	Bit 3	
	0	0	0	0 volts
	0	0	1	1/8 Vdd
	0	1	0	1/4 Vdd
	0	1	1	3/8 Vdd
	1	0	0	1/2 Vdd
	1	0	1	5/8 Vdd
	1	1	0	3/4 Vdd
	1	1	1	7/8 Vdd

REGISTER DESCRIPTION (continued)

CRKCFG AND CAMCFG FORMAT (continued)

For DEC = 0	VTHIGH			Positive Switch Point
	Bit 2	Bit 1	Bit 0	
	0	0	0	1/8 Vdd
	0	0	1	1/4 Vdd
	0	1	0	3/8 Vdd
	0	1	1	1/2 Vdd
	1	0	0	5/8 Vdd
	1	0	1	3/4 Vdd
	1	1	0	7/8 Vdd
	1	1	1	Vdd

NOTE: To insure proper operation, the positive switch point must be at least 1/8 Vdd above the negative switch point.

If time decreasing hysteresis is selected (DEC = 1), the positive switch point is a function of time. The negative switch point is always set to 0 volts. Initially, the positive threshold is set to its maximum value. After a high to low transition on the sensor input (falling edge passing through 0 volts), the positive threshold decays linearly in 16 steps to its minimum value. After a low to high transition (rising edge passes through positive threshold), the positive threshold is again set to its maximum and held there until a high to low transition. Figure 6 shows the time decreasing threshold with a sensor input and PSI digital output. Figure 7 shows how this can be used to increase noise immunity at higher speeds.

The maximum positive threshold is always set to 1/2 Vdd above the minimum. The VTLOW and VTHIGH bits are used to select the minimum switch point and the decay rate from maximum to minimum positive switch point.

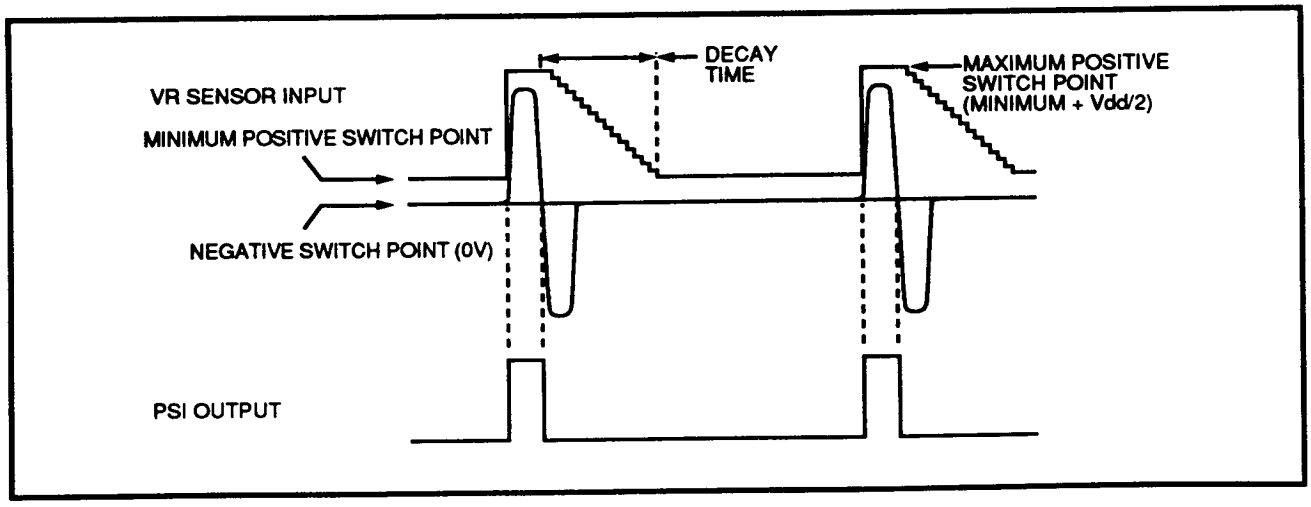


FIGURE 6: EIP VR Sensor Input, Threshold Levels and PSI Output

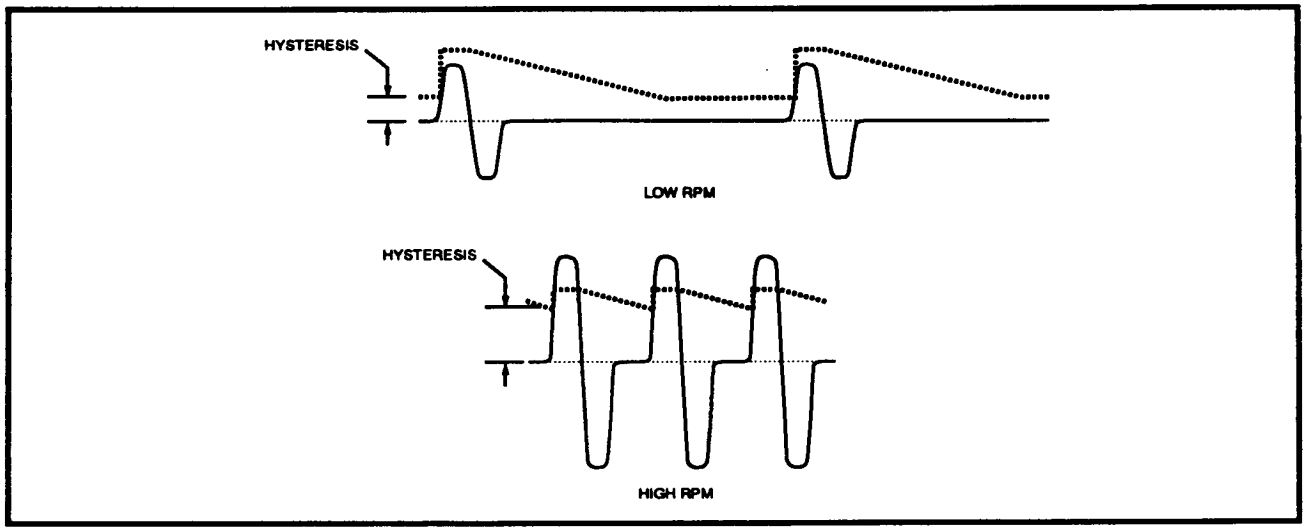


FIGURE 7: EIP Time Decreasing Hysteresis

For DEC = 1	VTLOW			Decay Time (Maximum to minimum threshold)
	Bit 5	Bit 4	Bit 3	
	0	0	0	8.192 msec
	0	0	1	1.024
	0	1	0	2.048
	0	1	1	3.072
	1	0	0	4.096
	1	0	1	5.120
	1	1	0	6.114
	1	1	1	7.168
For DEC = 1	VTHIGH			Minimum Positive Switch Point
	Bit 2	Bit 1	Bit 0	
	0	0	0	1/32 Vdd
	0	0	1	1/16 Vdd
	0	1	0	3/32 Vdd
	0	1	1	1/8 Vdd
	1	0	0	5/32 Vdd
	1	0	1	3/16 Vdd
	1	1	0	7/32 Vdd
	1	1	1	1/4 Vdd

REGISTER DESCRIPTION (continued)

ENGINE POSITION TRACKER (EPT)

The Engine Position Tracker (EPT) is the heart of the 67F687. It uses the conditioned crank and cam sensor signals from the PSI in conjunction with data stored in the EPT configuration RAM to determine engine angular position. This position is stored in the Angle Counter, a monotonic counter which tracks engine position with 0.25 degree resolution and is used to control the spark, fuel, tach and sync outputs.

EPT Page 0 Registers

Most of the memory used by the EPT is on page 1 because it will not be accessed by the host after initialization. The locations which the host needs to access during normal operation are located on page 0. These contain the angle count, interrupt status, reset, TACH and SYNC setup and test registers (used for factory testing).

NOTE: Accessing page 1 (setting GCR bit 0 = 1) inhibits the EPT from attaining sync, and will cause it to exit the sync mode if it had previously attained sync.

Angle Counter (ACNT)

The angle counter (ACNT) is a 12 bit representation of engine angular position stored in two 8 bit registers. The upper four bits (ac15-ac12) have no meaning and always return a 0 when read. The lower 11 bits (ac10-ac0) represent 0 to 359.75 degrees of engine rotation in 0.25 degree increments. It counts from 0 to 59F HEX (359.75 X 4) and then rolls over to 0 again. The MSB (ac11) is toggled every time this counter rolls over and is used to specify which half of a 720 degree cycle the engine is on (a four cycle engine requires 720 degrees to specify a unique position).

ACNT

0 0 0 0	ac11	ac10	ac9	ac8	ac7	ac6	ac5	ac4	ac3	ac2	ac1	ac0
	MSB	ENGINE POSITION										

MSB (ac11): 0 = first half of cycle (0 to 359.75 deg.)
1 = second half of cycle (360 to 719.75 deg.)

ENGINE POSITION: Engines degrees X 4 (in 0.25 degeree increments) 0 to 359.75 degrees (0 to 59F)
(ac10 - ac2): degrees in integer units
(ac1 - ac0): fraction of a degree
00 = 0
01 = .25
10 = .50
11 = .75

The EPT uses the crank input to determine engine position and engine speed to generate an interpolated count every 0.25 degrees. The interpolated count is corrected to the true count at each crank pulse input.

The angle counter (ACNT) is updated at a maximum rate of once every 2 µs. If the engine is in the steady state condition (no angular acceleration), the angle count is accurate to 0.25 degrees. Under positive or negative acceleration, the angle count interpolation between teeth will not exactly match true engine position. This error is dependent on the magnitude of the acceleration and the spacing between crank pulses (more pulses allow more frequent correction). The angle count is corrected at each crank pulse if the interpolated engine position does not match the true position for that pulse stored in EPT configuration RAM. If the interpolated value is too low (increase in engine speed) the angle count will be updated every 2 usec until it reaches the true position. If the angle count reaches the angular position of the next pulse before that pulse occurs (decrease in engine speed), the angle count will stop incrementing. When the pulse occurs, the angle count will be at the correct value and will begin counting again (at a new interpolation rate based on the spacing and time between the last two pulses). Notice that there are no missing angles in the angle count (monotonic) and once a new crank edge is received the angle count (ACNT) is immediately corrected.

Following a reset, ACNT is set to 07FF. This is not a valid angle count and inhibits any spark or fuel output pulses from occurring. ACNT remains at 07FF until synchronization with the engine is attained, at which time ACNT is initialized to the actual engine position.

ACNT cannot be read directly by the host. To read the angle count, the host must first write to location C0. This latches the present contents of ACNT into the 16 bit Angle Count Register (location C0 and C1). The Angle Count Register can then be read at any time, and will not change until another write to C0 occurs.

Synchronization

Synchronization (sync) is defined as the condition where the angle count (ACNT) reflects the actual engine position. For a four cycle engine, there can be two types or stages of sync. This is due to the fact that it takes two crankshaft revolutions (720 degrees) to complete one engine cycle.

Since the crankshaft rotates once every 360 degrees, the crank sensor pattern repeats this often. If the angle count attains sync to the crank (360 degree sync), the least significant 11 bits of ACNT accurately reflect the crankshaft position (0 to 360 degrees). This is sufficient for some engine control functions and in many cases can be attained sooner than 720 degree sync.

For other engine control functions (sequential injection, coil per cylinder DIS), crankshaft sync is not sufficient. Camshaft position is also required to indicate where in the engine cycle the crankshaft is. This is called cam or 720 degree sync. The MSB of ACNT (ac11) is used to indicate a unique angular position between 0 and 720 degrees. Some engines (such as 2 cycle) do not require 720 degree sync.

The 67F687 allows both types of sync to be used. Initially 360 degree sync can be attained and used to trigger the outputs and later, when 720 degree sync is attained, the EIP can be switched to that mode.

The mechanism by which either type of sync is attained is the detection of a unique pattern of crank and/or cam pulses, which corresponds to a particular crank or cam position. This unique pattern is then compared to patterns in the EPT configuration memory and if a match is found, the engine position corresponding to that pattern is loaded into ACNT. The EIP allows 8 unique patterns and each one can initiate either 360 or 720 degree sync.

Once sync is attained, the patterns are continuously detected and compared with the configuration memory. If ACNT does not match the expected value, the F687 sets an interrupt flag. Actions taken in this instance are determined by the initial setup by the host.

REGISTER DESCRIPTION (continued)

EPT Interrupts

Three interrupts can be generated by the EPT: attained 360 degree sync, attained 720 degree sync and lost either type of sync. These will set the appropriate bits in the Interrupt Register (location F3) and can generate an external interrupt to the host, depending on the value of the appropriate bit in the MASK Register (location F0).

If synchronization is lost, the cause is identified by a bit in the Sync Interrupt Status Register (SISR) at location C2. Normal operation is designated by a logic "0". A "1" indicates the reason that the EPT lost synchronization. Once set (to "1"), bits in SISR can only be cleared (reset to "0") by a read of the SISR register. This clears all the bits in the register.

SISR
Location C2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	TO	IP	AP	ACLSB	ST360	ST720	ACMSB

Bit 7	NOT USED.
TO	Timer Overflow: This is the timer that measures the time between crank pulses and is used to generate the interpolated 0.25 degree pulses. An overflow here means that there was too much time between pulses (crank sensor signal lost or engine cranking stopped or is too slow). The maximum time between two pulses is: Max time = 65535 • (degrees between pulses • 4 / 8,000,000) sec.
IP	Invalid pattern received: The pattern acquired does not match any of the patterns stored in PSREG.
AP	Address pointer error: The address stored in PRRAM for the acquired pattern does not match the address of the next expected tooth (CWRAM address).
ACLSB	Angle count error: Expected ACNT (bits 10-0) associated with the acquired pattern does not match true ACNT.
ST360	360 degree information stop: No 360 degree patterns were matched in two complete revolutions (720 degrees of ACNT).
ST720	720 degree information stop: No 720 degree patterns were matched in two complete revolutions (720 degrees of ACNT).
ACMSB	MSB error: Expected ACNT MSB (bit 11) associated with the acquired pattern does not match true ACNT MSB.

If the EPT is not reset (either automatically or by the host) after generating an out of sync interrupt, it will assume it is still in sync. In this case, if the condition that caused the interrupt reoccurs, another interrupt will be generated.

TACH and SYNC Outputs

A bit in EPTRST determines which signals are output to these pins. Either the conditioned CRANK and CAM (the output of the PSI) or the TACH and SYNC can be selected.

TACH and SYNC are one bit outputs used to relay specific engine positions to the host processor. These are both low frequency signals whose rising and falling edges indicate a particular engine position.

The SYNC signal output depends on the type of synchronization attained by the EPT. In 720 degree mode, it mirrors the MSB (bit 11) of the angle count (ACNT). The falling edge indicates a position of 0 (or 720) degrees. The rising edge indicates 360 degrees. The exception to this is the first rising edge after a reset. During reset the SYNC will go low (MSB of ACNT = 0) and a rising edge could occur anywhere between 360 and 720 degrees if the EPT attains 720 degree sync in this region. In 360 degree synchronization mode SYNC outputs a single low pulse per revolution with the falling edge at 0 degrees and a duration equal to the TACH pulsewidth.

The TACH output allows the host a finer resolution of angular position. It changes states every (TANG X 15) degrees. TANG is a number from 0 to 7 specified at location C3 (EPTRST) bits 4-2 (if TANG = 0 the multiplier is 8). In this way the host can receive angular position updates at angles of 15 to 120 degrees apart in multiples of 15 degrees. The TACH is reset to a low at 0 and 360 degrees. This means that after reset the TACH signal edges may not occur on 15 degree multiples of ACNT until ACNT reaches 0 or 360 degrees.

EPT Reset Register (EPTRST)

The EPTRST register (location C3) contains the bit to select the signals output on the TACH and SYNC pins, the TANG multiplier and the 720 and 360 degree reset bits. These enable the host to reset the EPT externally.

EPTRST
Location C3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	TSSEL	TANG			RST7	RST3

Bit 7	NOT USED. Always reads "0".
Bit 6	NOT USED. Always reads "0".
TSSEL	TACH and SYNC select bits. Determines signal which is output on TACH and SYNC pins. TSSEL = 0 - TACH and SYNC are output. TSSEL = 1 - Conditioned CRANK and CAM are output
TANG	Multiplier used to specify TACH output. TACH is reset to 0 on the rising or falling edge of SYNC and changes states every TANG X 15 degrees.
RST7	Writing a "1" to this bit will reset the ACNT 720 degree bit (bit 11). This must be followed by a "0" to this location to enable normal operation again.
RST3	Writing a "1" to this bit will reset ACNT to "7FF" (360 degree reset). This must be followed by a "0" to this location to enable normal operation again.

REGISTER DESCRIPTION (continued)

Test Registers (TMUX, TREG1, TREG2)

These registers are located at locations C4 through C6 and are used for factory testing. They should not be accessed during normal operation.

EPT Configuration (Page 1 Memory)

The EPT configuration memory is used by the host processor to configure the EPT for a specific sensor pattern. It specifies the crank sensor pulses and spacings (used to update ACNT) and the unique patterns and angular positions for attaining sync. The EPT cannot interpret position until the configuration memory is written to from the host processor. Because the data is supplied by the host, the host has no need to access this data after initialization, and should not do so without disabling the outputs. This memory is located on Page 1 of the memory map and to access it, a "1" must be written to the page select bit (bit0) of the GCR (location F6). This bit is set to a "1" by a reset.

The EPT configuration memory is divided into five sections: Crank Wheel RAM, Pattern Recognition RAM, Pattern Storage registers, Pattern Configuration registers and Pattern Acquisition registers. Each section is described in detail below.

Crank Wheel RAM (CWRAM)

CWRAM is 64 bytes located from 100 to 13F HEX. This RAM is used to define the crank wheel tooth (crank sensor pulse) spacing. The method chosen requires minimal RAM space for a large variety of wheel configurations.

To determine the proper data to load into CWRAM for a given wheel type, divide the wheel into sections of evenly spaced teeth. Arbitrarily choose one section and label the last tooth in this section as "00" HEX. Number the previous tooth "01", the one before it "02" and so on until all teeth are numbered. The tooth numbers should DECREASE as the engine rotates.

For a given section, the last tooth is defined as the one which precedes a change in tooth spacing. The last section is defined as the last section occuring in time as the engine rotates. The last tooth in the last section is the one numbered "00" (this is also the lead tooth in the first section).

The CWRAM consists of 32 pairs of 8 bit locations, each used to describe one section on the wheel. This means that the crank wheel can have up to 32 sections with each section having a unique tooth spacing. The information loaded for each section follows the format below.

CWSPxx	spacing between teeth (degrees X 4 or degrees depending on PMREG1 bit 7)
CWTHxx	number of next to last tooth in section

The information describing the last section is loaded into the first pair of locations (00 and 01), the next to last section is loaded into 02 and 03 and so forth until data for all sections of the wheel is loaded. If a particular wheel has N sections, then 2N locations will be loaded.

CWRAM Format

NAME	LOC	CONTENTS
CWSP00	100	spacing in section N
CWTH00	101	# of next to last tooth in section N
CWSP01	102	spacing in section N-1
CWTH01	103	# of next to last tooth in section N-1
.	.	.
.	.	.
.	.	.
CWSP (N-1)	1 (2N-3)	spacing in section 2
CWTH (N-1)	1 (2N-2)	# of next to last tooth in section 2
CWSP (N)	1 (2N-1)	spacing in section 1
CWTH (N)	1 (2N)	# of next to last tooth in section 1

Pattern Recognition RAM (PRRAM)

The Pattern Recognition RAM consists of 32 bytes starting at 140 HEX and containing information associated with each unique pattern used for sync. There are eight groups of four locations to correspond to the eight unique patterns specified in PSREG. The PRRAM contains the angle count for a particular crank pulse, the number of that pulse (tooth) and the address of CWRAM where the section of the wheel that contains that pulse is specified (the location where the next to last tooth in the section is specified). That address (minus the page bit) is divided by two and stored in PRRAM. There is a one to one correspondence of PRRAM to the patterns specified in PSREG (i.e. locations 140 - 143 refer to pattern 1 at location 160, locations 144 - 147 refer to pattern 2 at location 161, etc.).

PRRAM Format

NAME	LOC	CONTENTS
PRACH1	140	Pattern 1 angle count High
PRACL1	141	Pattern 1 angle count Low
PRTN01	142	Tooth number at that angle count
PRADD1	143	CWRAM address of section / 2
.	.	.
.	.	.
.	.	.
PRACH8	15C	Pattern 8 angle count High
PRACL8	15D	Pattern 8 angle count Low
PRTN08	15E	Tooth number at that angle count
PRADD8	15F	CWRAM address of section / 2

REGISTER DESCRIPTION (continued)

Pattern Storage Registers (PSREG)

The pattern storage registers are eight single byte registers located at 160 HEX to 167 HEX. The lower seven bits of each byte contain a sync pattern as it would be received by the Pattern Acquisition section of the EPT (specified by the Pattern Aquisition Registers-PAREG). The MSB is used to identify the pattern as occurring every 360 or every 720 degrees.

MSB = 0 Pattern occurs every 360 degrees
MSB = 1 Pattern occurs every 720 degrees

This bit is used by the EPT to determine which type of sync (360 or 720 degree) to enter when this pattern is matched.

CBIT (bit 6) is a special bit in the pattern which corresponds to bit 6 of the acquired pattern (as specified by the PAREG registers). This bit will be set by the Cam signal or a derivative of it as specified by bits 6 and 7 in the PAREG3 register. This feature allows differentiation of identical crank patterns if one is accompanied by a cam pulse and one is not.

CBIT = 0 If bit 6 of acquired pattern will not be set
CBIT = 1 If bit 6 of acquired pattern will be set

The lower 6 bits are the decoded pattern of the crank and cam sensors as defined by the Pattern Acquisition Registers.

There is a one to one correspondence between the patterns stored here and the data stored in PRRAM. If a pattern occurs every 360 degrees (MSB = 0), then the corresponding angle count in PRRAM should also have a "0" in the MSB (bit 11). If less than eight patterns are used, the data in the unused patterns is not critical; however, each location must have a unique 8 bit value (unused pattern locations cannot all have the same contents).

PSREG Format

NAME	LOC	CONTENTS		
PATRN1	160	MSB	CBIT	Pattern 1 (6 bits)
PATRN2	161	MSB	CBIT	Pattern 2
PATRN3	162	MSB	CBIT	Pattern 3
PATRN4	163	MSB	CBIT	Pattern 4
PATRN5	164	MSB	CBIT	Pattern 5
PATRN6	165	MSB	CBIT	Pattern 6
PATRN7	166	MSB	CBIT	Pattern 7
PATRN8	167	MSB	CBIT	Pattern 8

Pattern Acquisition Registers (PAREG)

The Pattern Acquisition section of the EPT contains four registers which define the format of the synchronization patterns and conditions (or "windows") under which they will be accepted as valid.

All patterns, to be recognized by the EPT, must have some common characteristics. Every pattern is preceded by a specified number of crank pulses. A start of pattern (SOP) pulse defines the beginning of the pattern and a specified number of end of pattern (EOP) pulses define its end. The pattern (as stored in the Pattern Storage Registers) is defined as beginning at the start of pattern pulse and ending on the last EOP pulse.

Synchronization patterns can be divided into two general groups: counted and decoded. Counted patterns are those where some specified pulses are counted as they are received. Decoded patterns are those where one signal is the data and is clocked into a shift register by another signal which is the clock. The 67F687 supports both types of patterns.

In addition to the conditioned crank and cam signals available from the PSI, other signals are generated by the EPT and can be used to either specify a pattern window or the pattern itself. These are generated in the EPT even if they are not used. Whether they are utilized depends on the individual application. A definition of these signals derived from the crank and cam pulses would be appropriate here.

Missing and extra crank pulses are detected by circuits in the EPT. These continuously monitor the time between successive crank input pulses. If this time increases or decreases drastically (faster than would be possible under normal acceleration or deceleration of the engine), then a missing or extra pulse detect signal is generated.

Crank - The conditioned crank signal which is generated by the PSI.

Cam - The conditioned cam signal generated by the PSI.

Missing Crank - Pulse generated by the missing crank pulse detection circuit.

Extra Crank - Pulse generated by the extra crank pulse detection circuit.

Qualified Crank - Crank signal with the extra pulses removed.

Crank Data - Signal generated by extra and missing pulses: rising edge on extra crank pulse, toggles on every crank pulse after that, and goes low (and stays low) when a missing pulse is encountered. This signal can be used for a coded pattern, when the data and the clock are both crank pulses.

Slow Cam - Rising edge on cam pulse and falling edge on next end of pattern.

Two additional signals are available but should not be used in normal operation. These are for factory testing only:

Crank Pin - Input directly from the CRANK pin (bypasses the PSI).

Cam Pin - Input directly from the CAM pin (bypasses the PSI).

REGISTER DESCRIPTION (continued)

Pattern Acquisition Registers (PAREG) (continued)

PAREG1 and PAREG4 (loc. 168 and 16B) define the window in which the pattern occurs. PAREG1 specifies the number of crank pulses before the EPT begins looking for a SOP pulse to begin the pattern and the number of EOP pulses to end the pattern.

PAREG1
Location 168

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EOPNUM				CRKNUM			

EOPNUM	The number of EOP pulses to end the pattern. Must be a number from 1 (0001) to 15 (1111) - 0000 is not valid.
CRKNUM	The number of crank pulses before looking for a SOP pulse. Must be a number from 1 (0001) to 15 (1111) - 0000 is not valid.

PAREG4 specifies the type or types of pulses used for SOP or EOP. They can be one or a combination of the allowable pulses.

PAREG4
Location 16B

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SOTYP				EOTYP			

SOPTYP	Any or all of the following types of signals can be an SOP pulse, enabled by setting the appropriate bit in SOPTYP: Bit 7 - Crank Bit 6 - Cam Bit 5 - Extra Crank Bit 4 - Missing Crank
EOPTYP	Any or all of the following types of signals can be an EOP pulse, enabled by setting the appropriate bit in EOPTYP: Bit 3 - Extra Crank Bit 2 - Missing Crank Bit 1 - Qualified Crank Bit 0 - Crank

PAREG2 and PAREG3 determine the type of pattern (counted or coded) and the signals used to generate the pattern. PAREG2 defines the type of pattern and the signal used for data if the pattern is a coded type. If the pattern is a counted type, then bits 5-0 have no meaning.

PAREG2
Location 169

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBE	TYP	CDEDAT					

PBE	Pattern bit 6 enable. This bit determines if bit 6 in the acquired pattern will be set by one of the signals defined in PATBT6 (PAREG3 bits 7 and 6). PBE = 0 - Pattern bit 6 set based on PATBT6. PBE = 1 - Pattern bit 6 always "0".
TYP	Specifies the type of pattern: TYP = 0 - Pattern is coded TYP = 1 - Pattern is counted
CDEDAT	Defines the signal or signals uses as data for a coded pattern. Not used (and contents have no effect) if data is counted (TYP = 1). The data can be any or all of the following types of signals, enabled by setting the appropriate bit in CDEDAT: Bit 5 - Crank Data Bit 4 - Always "0" Bit 3 - Cam Bit 2 - Missing Crank Bit 1 - Extra Crank Bit 0 - Cam Pin (FOR TEST ONLY)

REGISTER DESCRIPTION (continued)

Pattern Acquisition Registers (PAREG) (continued)

PAREG3 defines the clock for coded data (if PAREG2 bit 6 = 0) or the signal that is counted (if PAREG2 bit 6 = 1).

PAREG3
Location 16A

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PATBT6		CNTCLK					

PATBT6	If PAREG2 (loc. 169) bit 7 = "0", PATBT6 defines the signal which will set bit 6 of the acquired pattern. This corresponds to CBIT (bit 6) of the specified patterns stored in PATRN1 through PATRN8 in PSREG. One of the following types of signals is selected by setting the appropriate bits in PATBT6:

Bit7	Bit6	Signal
0	0	Cam
0	1	Not Used
1	0	Slow Cam
1	1	Cam Pin (TEST ONLY)

If PAREG2 bit 7 = "1", bit 6 of the acquired pattern will always be "0" and PATBT6 has no effect.

CNTCLK	Defines the signal or signals that are counted if the pattern type is counted (TYP = 1) or the clock if the pattern is coded (TYP = 0). The pulses can be any or all of the following types of signals, enabled by setting the appropriate bit in CNTCLK: Bit 5 - Crank Bit 4 - Cam Bit 3 - Extra Crank Bit 2 - Missing Crank Bit 1 - Qualified Crank Bit 0 - Crank Pin (FOR TEST ONLY)

Test Registers

Special test registers are located at locations 16E and 16F. These are used for factory testing of the part and should not be accessed during normal operation.

Pattern Match Registers (PMREG)

The Pattern Match registers are seven miscellaneous registers in the EPT, which contain crank wheel information, default information and EPT reset control.

PMREG1
Location 170

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RES	0		NUMSEC				

RES	Resolution of tooth spacing in CWSPxx. RES = 0 - CWSPxx is 0.25 degrees per bit (maximum 63.75 deg.) RES = 1 - CWSPXX is 1 degree per bit (maximum 255 deg.)
NUMSEC	Number of sections on crank wheel - 1 (as described in CWRAM. Must be a number from 0 through 31 (1 through 32 sections)

PMREG2
Location 171

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	IAE3	IAE7	0				

IAE3	Enables automatic reset of ACNT (locations C0 and C1) upon a 360 degree type out-of-sync error. ACNT is reset to 07FF. IAE3 = 1 - Automatic reset of ACNT IAE3 = 0 - Manual reset by host required.
IAE7	Enables automatic reset of MSB (720 degree bit) in ACNT (location C0) upon a 720 degree type out-of-sync error. IAE7 = 1 - Automatic reset of ACNT MSB IAE7 = 0 - Manual reset by host required.

PMREG3
Location 172

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PULNUM							

PULNUM	Number of pulses (teeth) on crank wheel - 1 (number from 0 to 255 (00 to FF HEX)).

REGISTER DESCRIPTION (continued)

Pattern Match Registers (PMREG) (continued)

PMREG5 contains a default tooth spacing (in degrees X 4) which is used before sync is attained. The value loaded here depends on the particular pattern and can affect how fast the EPT will attain sync with that particular pattern. PMREG5 is accessed at either location 174 or 175 (a write to either location will change PMREG5).

PMREG5
Location 174 or 175

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPSDFT							

SPSDFT	Spacing between crank teeth used as a default before sync is attained. Units are consistent with CWSPxx (0.25 deg/bit if PMREG1 bit 7 = 0 and 1 deg/bit if PMREG1 bit 7 = 1). Number from 01 to FF HEX.

PMREG4, PMREG6 and PMREG7 (locations 173, 176 and 177) are used for testing only and should not be written to during normal operation.

FUEL SPARK PULSE GENERATOR (FSPG)

The FSPG generates the digital pulses that are used by the Fuel Spark Output Controller (FSOC) to create the fuel and ignition output signals.

Eight spark pulses, each with a start and stop angle, can be programmed. These are mapped to the four ignition outputs. This allows an individual spark advance for up to eight cylinders when the ignition outputs control dual ended ignition coils (one coil for two cylinders).

Eight fuel pulses, each with a start angle and pulsewidth time, can also be programmed.

The FSPG uses the angle count (ACNT) from the EPT and an internal timer to generate these digital pulses at the correct engine positions. These pulses can also be initiated or terminated directly by the host.

Direct Output Control

The GCR (location F6) allows the host to choose either direct control or programmed control of the spark and fuel outputs. After reset, the GCR is configured for direct control.

If GCR bit 4 = 1, the spark pulses are generated under direct control by the host. Each spark pulse mirrors the associated bit in the Spark Pulse Register (location F1); bit 0 of the Spark Pulse Register (SPRK) corresponds to spark pulse 0, bit 7 corresponds to spark pulse 7. A "1" in each bit location will turn on the pulse and a "0" will turn it off. If GCR bit 4 = 0, the SPRK register has no effect on the outputs. Upon reset SPRK is set to "00", turning off all spark pulses.

If GCR bit 7 = 1, the fuel pulses are under direct host control. Each fuel pulse is initiated by a writing a "1" to the corresponding bit in the Fuel Pulse Register (location F2) followed by writing a "0" to that bit. Bit 0 of the Fuel Pulse Register (FUEL) corresponds to fuel pulse 0, bit 7 corresponds to fuel pulse 7. The duration of the pulse is determined by the programmed pulsewidth stored in Fuel RAM (FRAM), and cannot be turned on indefinitely (but if the bit in the Fuel Pulse Register is still set to a "1" when the pulse times out, it will be immediately turned on again). In this way the fuel pulses differ from the spark pulses. If GCR bit 7 = 0, the FUEL register has no effect on the outputs. Upon reset FUEL is set to "00", turning off all fuel pulses.

The FSPG also allows a hard shutdown of all spark and fuel pulses by the host. If bit 5 of the GCR is a "1", all eight spark and all eight fuel pulses will be turned off immediately and will stay off until that bit is changed to a "0". Upon reset bit 5 of the GCR is set to a "0", enabling the outputs.

GCR
Location F6

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FDC	0	SHTDN	SDC	TST3	TST2	TST1	PG

FDC	Fuel Direct Control bit FDC = 0 - Programmed control of fuel outputs FDC = 1 - Direct control of fuel using FUEL register
Bit 6	NOT USED (always returns a "0" when read)
SHTDN	Hard Shutdown bit SHTDN = 0 - Normal operation SHTDN = 1 - All fuel and spark outputs are turned off
SDC	Spark Direct Control bit SDC = 0 - Programmed control of spark outputs SDC = 1 - Direct control of spark using SPRK register
TST3	Test bit (factory testing only - should always be a "0").
TST2	Test bit (factory testing only - should always be a "0").
TST1	Test bit (factory testing only - should always be a "0").
PG	Page bit for addressing page 1 memory PG = 0 - Page 0 addressed PG = 1 - Page 1 addressed

At reset, the GCR is initialized to "91". This enables fuel and spark direct control and sets up page 1 addressing.

SPRK
Location F1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPK7	SPK6	SPK5	SPK4	SPK3	SPK2	SPK1	SPK0

If SDC = 1:
SPKx = 0 SPARKx pulse is off
SPKx = 1 SPARKx pulse is on

If SDC=0: SPKx has no effect

REGISTER DESCRIPTION (continued)

FUEL

Location F2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FUEL7	FUEL6	FUEL5	FUEL4	FUEL3	FUEL2	FUEL1	FUEL0

If FDC = 1:
FUELx = 0 no effect
FUELx = 1 FUELx output pulse is initiated

If FDC = 0:
FUELx has no effect

At reset SPRK and FUEL are both initialized to "00", turning off all outputs.

Programmed Output Control

Spark pulses

When GCR bit 4 (SDC) = 0, spark pulses are generated from a start angle to a stop angle. These start and stop angles are stored in Spark RAM (SRAM) at locations 00 through 1F HEX as 16 bit numbers. Start angles are stored in SSTRHx and SSTRLx and stop angles are stored in SSTPHx and SSTPLx. They have the same format as ACNT (0 to 359.75 degrees in 0.25 degree increments with bit 11 indicating an angle count between 360 and 720 degrees). In addition, the angles are concatenated with a bit in the most significant location (bit 15) that tells the FSPG if the angle is used every 720 or 360 degrees.

When ACNT is equal to the start or stop angle programmed, the spark pulse will either begin or end. If bit 15 is a "1", all twelve bits of ACNT are compared to SSTRHx, SSTRLx (SSTPHx, SSTPLx) to initiate (end) a pulse. This generates a pulse every 720 degrees. If this bit is a "0", bit 11 (MSB) of ACNT is ignored and only bits 10-0 are compared to SSTRHx, SSTRLx (SSTPHx, SSTPLx). This generates a pulse every 360 degrees.

NOTE: Care should be exercised to only set this bit if the EPT is in the 720 degree sync mode. If it is set, and the EPT is tracking in 360 degree mode, any angles with a "1" in bit 11 will not be recognized.

Two byte writes are required to update an angle. The most significant byte (MSB) must be written first, followed by the LSB. This is because the MSB is stored in a latch until the LSB is received, and both bytes of the angle value are updated simultaneously. Angles can be read in any order.

There are eight digital spark pulses in the FSPG. After the angle count (ACNT) changes, all the values in SRAM are compared to the current angle count. If a match(s) is found, the related pulse(s) will start or end 2 µs after the angle changed (at 10,000 RPM, 2 µs is equal to 0.125 crankshaft degrees).

SSTRHx					SSTRLx
b15	0	0	0	b11	ANGLE

b15	Indicates if pulse starts every 360 or 720 degrees. b15 = 0 - b11 is ignored (pulse every 360 deg.) b15 = 1 - b11 is compared (pulse every 720 deg.)
b11	Indicates which half of 720 cycle ANGLE is in (0 to 360 degrees or 360 to 720 degrees)
ANGLE	Start angle of pulse in degrees X 4. This is a number between 0 and 359.75 (same format as ACNT).

SSTPHx					SSTPLx
b15	0	0	0	b11	ANGLE

b15	Indicates if pulse stops every 360 or 720 degrees. b15 = 0 - b11 is ignored (pulse every 360 deg.) b15 = 1 - b11 is compared (pulse every 720 deg.)
b11	Indicates which half of 720 cycle ANGLE is in (0 to 360 degrees or 360 to 720 degrees)
ANGLE	Stop angle of pulse in degrees X 4. This is a number between 0 and 359.75 (same format as ACNT).

NOTE: SSTRHx and SSTPHx bit 15 should be the same or undesired operation may result.

Spark Mapping Register (SMAP)

The FSPG generates eight spark pulses. Each one corresponds to a spark occurrence in an individual cylinder. Because the 67F687 has four spark outputs, the spark pulses are grouped together and mapped to the proper output in the FSOC. This allows the EIP Spark outputs to be configured for a variety of engine and coil types.

Each FSPG spark pulse is directed to a particular FSOC spark output as shown below:

FSPG Spark Pulse	FSOC SPRK Output
0,4	0
1,5	1
2,6	2
3,7	3

Each SPRK output can be controlled by one spark pulse (coil per cylinder), two spark pulses (coil per two cylinders) or no spark pulses (turned off).

The SMAP register (location F7) enables the individual FSPG Spark pulses. Each bit corresponds to a pulse (bit 0 to pulse 0, bit 7 to pulse 7).

SMAP
Location F7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

ENx = 1: Spark pulse x is enabled to the proper FSOC SPRK output
ENx = 0: Spark pulse x is disabled.

REGISTER DESCRIPTION (continued)

Fuel Pulses

Fuel pulses start at a programmed angle and stop after a programmed duration has expired. Fuel start angles have the same format as spark angles. They are stored in FRAM (locations 20 to 3F) in the FSTRHx and FSTRLx registers.

The time duration is a 16 bit number with a resolution of 4 µs/bit. This allows fuel pulsewidths of up to 262.14 ms. These times are also stored for each output in FRAM in the FPTHx and FPTLx registers.

The read and write requirements of both start angles and duration times are identical to the spark angles (consecutive writes MSB first). Like the spark outputs, the fuel pulses will start 2 µs after ACNT changes and matches one or more of the start angle values.

Once the pulse has started, a delay timer counts up to the programmed duration time using a 4 µs clock. When the timer value reaches (or exceeds) the programmed value, the pulse stops. Pulses can be stretched after starting by writing a new value to FRAM before the timer has reached the old value. Pulses can be turned off immediately by writing a new value to FRAM that is less than the timer value.

The individual timer values are stored in read-only memory in the Timer RAM (TRAM) at locations 40 to 4F HEX. During normal operation, all eight can be indirectly read from TRAM. A host read of either the MSB or the LSB of the two byte value, will strobe both bytes into the Fuel Timer Read Registers (locations F4 and F5). The data on the external bus for this read is invalid. Both bytes can then be read from the Timer Read Registers 4 µs later.

The TRAM cannot be written into under normal operation.

FSTRHx					FSTRLx
b15	0	0	0	b11	ANGLE

b15	Indicates if pulse starts every 360 or 720 degrees. b15 = 0 - b11 is ignored (pulse every 360 deg.) b15 = 1 - b11 is compared (pulse every 720 deg.)
b11	Indicates which half of 720 cycle ANGLE is in (0 to 360 degrees or 360 to 720 degrees)
ANGLE	Start angle of pulse in degrees X 4. This is a number between 0 and 359.75 (same format as ACNT).

FPTHx	FPTLx
FUELPW	

FUELPW	Fuel pulse duration time in µs/4. Can be number from 0000 (pulse off) to FFFF HEX (262.14 ms).

FUEL SPARK OUTPUT CONTROLLER (FSOC)

The FSOC contains the digital logic that controls the analog output circuits, stores diagnostic information, and measures coil charge times. Also residing in the FSOC are the analog output circuits which drive the off chip power transistors and sense operating conditions. There are four spark drive outputs (SPRK3-0) and eight fuel injector drive outputs (FUEL7-0). Each of the outputs has a sense input associated with it. The spark sense (SSEN3-0) inputs monitor the current through the primary side of the ignition coil via an external sense resistor. The fuel sense (FSEN7-0) inputs monitor the voltage at the drive side of the fuel power transistor. An additional spark monitor (SPKMON) input monitors the high voltage inductive spike which occurs at the coil primary when it is turned off.

Spark Control

The 67F687 has four identical spark output circuits. Each circuit has a control input (from the FSPG), a drive output (SPRKx) and a current sense pin (SSENSx). The outputs are designed to drive either an external IGBT directly or a Darlington through an emitter follower. These in turn drive the ignition coil. The current sense pin measures the current through the ignition coil by measuring the voltage across a sense resistor (typically 0.05Ω). The SPKGND pin provides a ground reference to minimize the effects of offset between the sense resistor ground and the 67F687's ground. A single Spark Monitor (SPKMON) input is used for all four outputs. See Figure 8 for a typical external output circuit.

Different modes of operation for the spark outputs can be selected by the FSOC Control Register (FSOCTL) at location F8. These modes are direct operation, current limit, and auto fire. A bit is available for each output to indicate if the current reached a predetermined level before the coil was fired. Also a timer can be enabled to measure the time it took the current to reach a predetermined level for a particular output. The voltage at the sense inputs is used to control the operation of these different modes.

The voltage at the sense inputs is compared to three different threshold levels: TH1, TH2 and TH3. Nominal values of these (for Vdd = 5V) are:

TH1 = 300 mV
TH2 = 350 mV
TH3 = 500 mV

In the direct mode of operation, the SPRKx outputs follow the FSPG pulses directly. In the current limit mode, the SPRKx output is controlled by a feedback loop that maintains TH2 at the sense input until the FSPG pulse ends (coil fires). If current limit is not desired, the auto fire mode can be enabled. In this mode, the output will turn off when the voltage at the sense input reaches TH3.

Four bits are available to monitor each output. These are located in the read only Spark Status registers (SPKST1 and SPKST2).

The STATx bits reflect the state of the SPRKx output and can be read by the host at any time. They are updated when the state of the output changes.

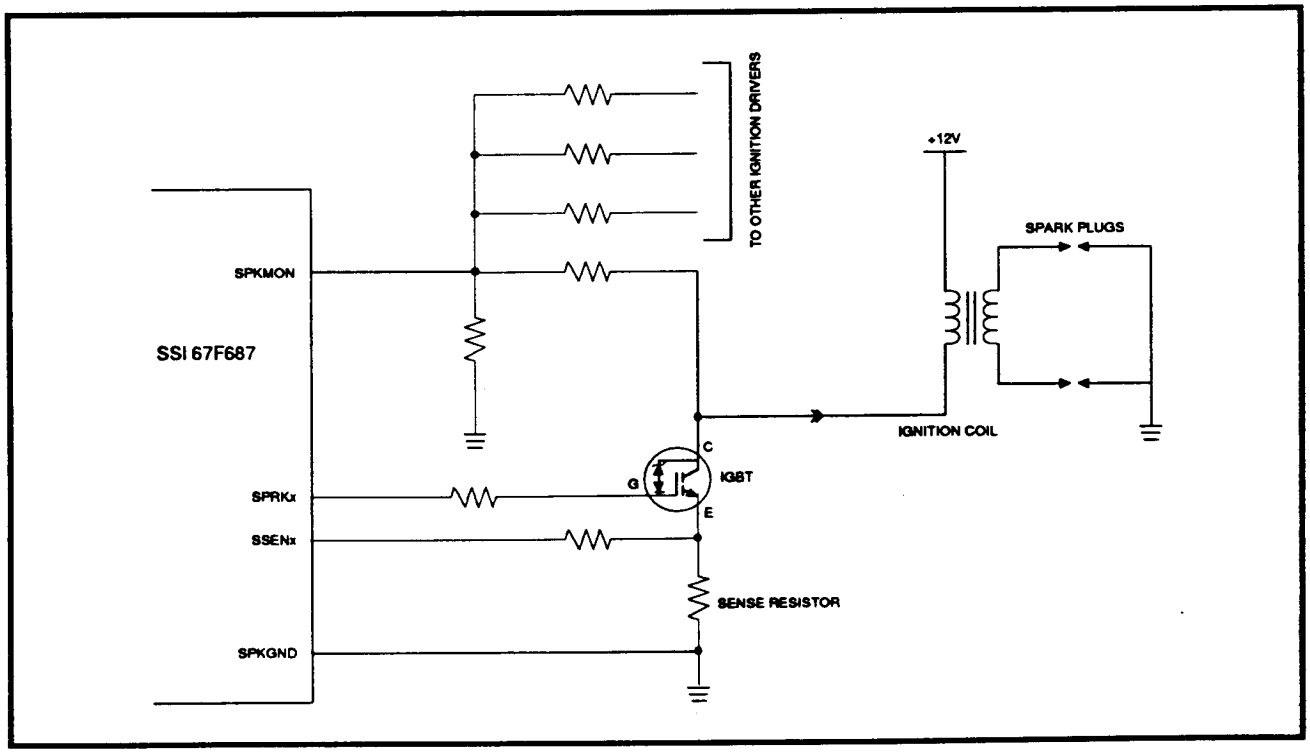


FIGURE 8: Typical EIP Spark Output External Circuit

REGISTER DESCRIPTION (continued)

Spark Control (continued)

The IDWLx bits indicate if the voltage at the corresponding sense input reached TH1. The ILIMx bits indicate one of two things depending on the operating mode. In the current limit mode, they indicate if current limit was active before turn off (if the sense voltage reached TH2). In the auto fire mode, the ILIMx bit indicates if TH3 was reached before turn off. If both current limit and auto fire are disabled, ILIMx will indicate if TH3 was reached, even though the output was not turned off. The ILIM and IDWL bits are updated every time a pulse is output and can be read at any time.

SPKMx bits indicate if a voltage greater than 2/3 Vdd was seen at the SPKMON input within 64 µs of the output turning off. If this voltage is not detected by the end of this window, the appropriate SPKMx bit will be latched to a "1". The occurrence of a spark monitor fault at one output does not prevent any other output from detecting its own spark monitor fault. Also a bit is set in the Interrupt Register (F3). If the SMSK bit in the Interrupt Mask Register (F0) is also set, an external interrupt will be generated. The SPKMx bits can only be cleared (reset to a "0") by a read of the SPKST1 register by the host. A read will clear all the SPKMx bits.

An additional feature available on the SPRKx outputs is a timer which measures the time from output turn on to the sense voltage reaching TH1. This can be used by the host in determining the proper dwell time for each coil. This timer is multiplexed among the four outputs. Two bits (TI1, TI0) in FSOCTL determine which output is to be measured. The timer is incremented every 32 usec and can measure a maximum time of 8.16 ms (8 bits).

A measurement is initiated by writing a "1" to the IIM bit of FSOCTL. The timer is started at the next rising edge of the selected output and stopped when the voltage at the sense input reaches TH1 or the output is turned off. It is latched into the Dwell Time Register (F9), the DMC bit in FSOCTL is set, and the IIM bit is reset to "0". The DMC bit cannot be written to and is reset by a write to the FSOCTL register. If the counter overflows (time > 8.16 ms) the result in the Dwell Time Register will be "00".

FSOCTL
Location F8

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IIM	DMC	ILE	AFE	FFE	0	TI1	TI0

IIM	Initiate dwell measurement IIM= 0 - no dwell measurement IIM = 1 - dwell measurement will begin upon turn on of specified output (TI1, TI0). (Reset when DMC is set to a "1")
DMC	Dwell measurement complete (read only). Set when dwell measurement is completed or pulse is turned off. Cleared by a write to FSOCTL.
ILE	Current limit enable ILE = 0 - no current limit ILE = 1 - current limit mode enabled for all outputs
AFE	Auto fire enable AFE = 0 - Auto fire disabled AFE = 1 - Auto fire mode enabled for all outputs NOTE: if both ILE and AFE are set, the current limit mode will override the auto fire feature.
FFE	Fuel fault enable FFE = 0 - FUELx outputs unaffected by Fuel sense inputs FFE = 1 - FUELx output will be turned off if corresponding sense input detects a short to battery.
Bit 2	NOT USED (always returns a "0")

TI1, TI0	Point to output to be measured by Dwell Timer TI1, TI0 = 00 - SPRK0 TI1, TI0 = 01 - SPRK1 TI1, TI0 = 10 - SPRK2 TI1, TI0 = 11 - SPRK3

DTIME
Location F9

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIME							

TIME	Dwell time measurement for specified output (32 µs/bit)

SPKST1
Location FA

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STAT3	STAT2	STAT1	STAT0	SPKM3	SPKM2	SPKM1	SPKM0

STATx	Output state STATx = 0 - Corresponding output is off STATx = 1 - Corresponding output is on
SPKMx	Spark monitor bits SPKMx = 1 - No spark detected (no voltage spike at SPKMON input after corresponding output turned off) SPKMx = 0 - Spark detected NOTE: SPKMx = 1 will be latched until a read of SPKST1 occurs

SPKST2
Location FB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IDWL3	IDWL2	IDWL1	IDWL0	ILIM3	ILIM2	ILIM1	ILIM0

IDWLx	TH1 threshold reached at sense input before turn off IDWLx = 0 - TH1 not reached IDWLx = 1 - TH1 reached
ILIMx	Current limit or autofire active (TH2 or TH3 reached at sense input). ILIMx = 0 - Current limit or autofire not active ILIMx = 1 - Current limit or autofire active at turn off

REGISTER DESCRIPTION (continued)

FUEL CONTROL

There are eight fuel control outputs (FUELx) each with a dedicated sense input (FSENSx) for diagnostics and fault protection. Each output is controlled by the corresponding fuel pulse from the FSPG and in normal operation will mirror that pulse.

The state of each output is reflected by the Fuel State Register (FST) at location FF and can be read at any time by the host.

The FSENSx inputs are used to detect a fault at the corresponding output. They monitor the output of each external power transistor. Figure 9 shows typical external components for each output. The faults that can be detected by the FSENSx inputs are: short to battery, short to ground and open load.

A short to battery is detected when the output is on. Under normal conditions the power output device will pull the load close to ground when it is turned on. If the load is shorted to the battery, the output will remain close to battery voltage. This is detected by a comparator at FSENSx and the bit corresponding to that output is set in Fuel Fault Register 1 (FF1 at location FC). If the FFE bit in FSOCTL is set, this will also immediately turn off that output to prevent damage to the output transistor.

A short to ground and an open load are detected when the output is turned off. Under normal conditions the FSENSx voltage should be close to battery voltage when the output is off. If a voltage close to ground is detected under these conditions, the appropriate bit is set in Fuel Fault Register 2 (FF2 at location FD).

To detect an open load, a there is a large internal resistor from the FSENSx input to 1/2 Vdd. If there is an open load, the voltage at FSENSx will be 1/2Vdd when the output is off. If this is detected, the corresponding bit will be set in the Fuel Fault Register 3 (FF3 at location FE).

Any of the detected faults (in FF1, FF2 or FF3) will be reflected in the Interrupt Register and can cause an external interrupt to the host. This is enabled by the Interrupt Mask Register. Once set, a fault can only be cleared by a read of the offending fault register by the host (this clears all faults in that register).

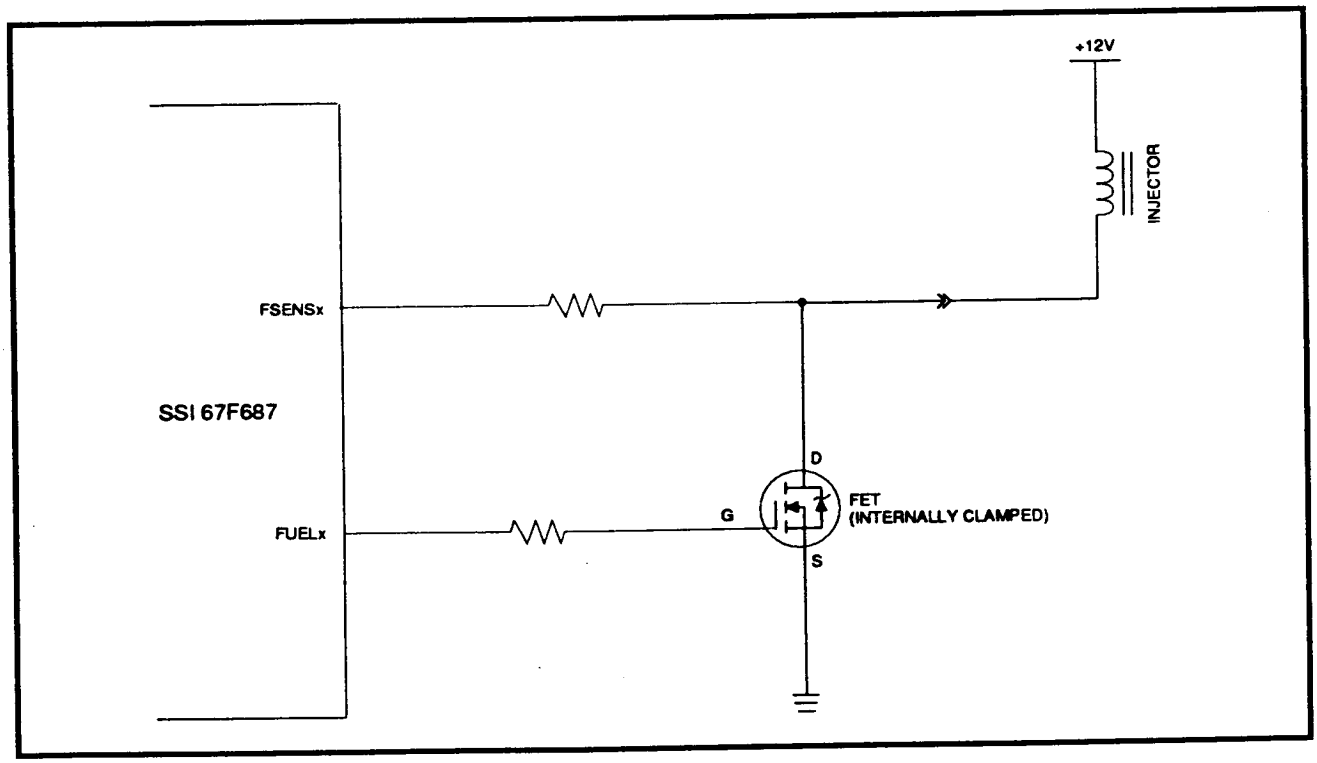


FIGURE 9: Typical EIP Fuel Injector Output External Circuit

FST
Location FF

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FST7	FST6	FST5	FST4	FST3	FST2	FST1	FST0

FSTx	State of corresponding FUELx output FSTx = 0 - Output is off FSTx = 1 - Output is on

FF1
Location FC

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHB7	SHB6	SHB5	SHB4	SHB3	SHB2	SHB1	SHB0

SHBx	Fuel output has short to battery SHBx = 0 - No fault SHBx = 1 - Short to battery at the corresponding output

FF2
Location FD

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHG7	SHG6	SHG5	SHG4	SHG3	SHG2	SHG1	SHG0

SHGx	Fuel output has short to ground SHBx = 0 - No fault SHBx = 1 - Short to ground at the corresponding output

FF3
Location FE

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FOL7	FOL6	FOL5	FOL4	FOL3	FOL2	FOL1	FOL0

FOLx	Fuel output has open load fault FOLx = 0 - No fault FOLx = 1 - Open load fault at the corresponding output

REGISTER DESCRIPTION (continued)

EXTERNAL INTERRUPT

Two registers control the external interrupt to the host. The Interrupt Register (INT at location F3) receives inputs from the EPT and the FSOC and has seven bits which could potentially generate an interrupt. This register is read only. The interrupt bits are set by specific conditions occurring in the FSOC or EPT and are all cleared by a read of this register by the host.

The Interrupt Mask Register (MASK at location F0) determines which of these bits will generate an external interrupt on the $\overline{INT}$ pin. There are four bits which mask types of interrupts. There is also a bit which will turn off all fuel and spark outputs if the EPT goes out of 360 degree sync, and if the 360 degree automatic reset bit (IAE3) in PMREG2 (location 171) is set. This bit is set automatically by the EPT if the above conditions are met. It can also be set by the host to turn off all pulses immediately. After being set, it can only be reset by writing a "0" to it. After reset, the MASK register is initialized to "1F". This means that this bit must be reset by the host before any fuel or spark outputs are enabled.

INT
Location F3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LSYNC	SYNC3	SYNC7	0	FI3	FI2	FI1	SPKI

LSYNC	Lost sync. Set by EPT if it looses either 360 or 720 degree sync. The host can then read SISR (location C2) to determine the cause of losing sync.
SYNC3	In 360 degree sync. Set by the EPT when it attains 360 degree sync.
SYNC7	In 720 degree sync. Set by the EPT when it attains 720 degree sync.
FI3	Fuel interrupt 3. Set when one or more bits in FF3 (location FE) are set indicating a fuel output open load fault. FF3 can then be read to determine which output(s) is faulted.
FI2	Fuel interrupt 2. Set when one or more bits in FF2 (location FD) are set indicating a fuel output short to ground fault. FF2 can then be read to determine which output(s) is faulted.
FI1	Fuel interrupt 1. Set when one or more bits in FF1 (location FC) are set indicating a fuel output short to battery fault. FF1 can then be read to determine which output(s) is faulted.
SPKI	Spark interrupt. Set if any of the SPKMx bits in SPKST1 (location FA) are a "0". This indicates that a voltage spike was not detected by the Spark monitor at coil turn off for one or more spark outputs. SPKST1 can be read to determine which coil(s) did not fire.

MASK
Location F0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	EPTES	OSMSK	ISMSK	SMSK	FMSK

EPTES	EPT error stop bit. Turns off all fuel and spark pulses. Set by the EPT (if IAE3 in PMREG2 is set) or by the host. Reset by the host. Must be reset to enable fuel or spark outputs. EPTES = 0 - Fuel and spark pulses enabled. EPTES = 1 - Fuel and spark pulses disabled.
OSMSK	Out of sync interrupt mask. Enables LSYNC to cause an external interrupt. OSMSK = 1 - LSYNC inhibited from causing an external interrupt. OSMSK = 0 - LSYNC will generate an external interrupt.

ISMSK	In sync interrupt mask. Enables SYNC7 or SYNC3 to cause an external interrupt. ISMSK = 1 - SYNC7 and SYNC3 inhibited from causing an external interrupt. ISMSK = 0 - SYNC7 or SYNC3 will generate an external interrupt.
SMSK	Spark interrupt mask. Enables SPKI to cause an external interrupt. SMSK = 1 - SMSK inhibited from causing an external interrupt. SMSK = 0 - SMSK will generate an external interrupt.
FMSK	Fuel interrupt mask. Enables FI1, FI2 or FI3 to cause an external interrupt. FMSK = 1 - FI1, FI2 and FI3 inhibited from causing an external interrupt. FMSK = 0 - FI1, FI2 or FI3 will generate an external interrupt.

PULSE WIDTH MODULATOR (PWM)

The PWM generates four pulse width modulated outputs (PW3 - PW0) which can be used to drive four of the GPIO pins. The outputs are paired: PW3 with PW2 and PW1 with PW0. Each pair has a programmable output frequency. The frequency can be one of sixteen possible values, specified in the PWM Control Register (PWMCTL).

Each output also has an associated Duty Cycle Register (PWMDC3 - PWMDC0), where the on time of the output can be specified from 0 to 255/256 of the output period.

PWMCTL
Location E0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRSC32				PRSC10			

PRSC32	Prescale value for PWM3 and PWM2 frequency
PRSC10	Prescale value for PWM1 and PWM0 frequency

Output Freq. (Hz)	Prescale Value
20	8 (1000)
40	0 (0000)
65	9 (1001)
113	A (1010)
129	1 (0001)
166	B (1011)
206	C (1100)
226	2 (0010)
244	D (1101)
279	E (1110)
326	F (1111)
332	3 (0011)
411	4 (0100)
488	5 (0101)
558	6 (0110)
651	7 (0111)

REGISTER DESCRIPTION (continued)

PULSE WIDTH MODULATOR (PWM) (continued)

PWMDC0
Location E1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0 Duty Cycle							

PWMDC1
Location E2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1 Duty Cycle							

PWMDC2
Location E3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2 Duty Cycle							

PWMDC3
Location E4

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3 Duty Cycle							

PWMx Duty Cycle	(On time / Period) x 256

All PWMDC registers can be written to and read from by the host at any time. Rewriting the same duty cycle or prescale value will not cause a reset or transient at the PWM outputs. A change in the duty cycle or frequency will be immediately reflected in the outputs.

When in reset, PWMCTL and PWMDCx registers are all set to "00". This inhibits any pulses from being generated.

GENERAL PURPOSE I/O (GPIO)

The GPIO consists of eight ports (pins), GPIO0 through GPIO7, that can be configured as either digital inputs or digital outputs. These are individually configurable.

When used as inputs, GPIO4 - GPIO7 can be configured as level, rising edge or falling edge sensitive. GPIO0 - GPIO3 provide only level sensitive input capability.

When used as outputs, GPIO0 - GPIO3 can be configured as either direct digital outputs or as pulsewidth modulated outputs from the PWM block. GPIO4 - GPIO7 provide only direct digital outputs.

There are five registers which control the operation of the GPIO. They are Input Data (GINP), Output Data (GOUT), Output Enable (GOER), Mode Select (GMSR) and Edge Select (GESR). They are located at locations E5 through E9. Each bit in the registers is associated with the corresponding I/O port (bit 0 with GPIO0, bit 1 with GPIO1, etc.).

The Output Enable register controls the direction of each port. If a bit is a "1", the corresponding port is an output, if it is a "0", the port is an input.

GOER - GPIO Output Enable Register
Location E7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0

DRx = 0 - GPIOx pin is an input

DRx = 1 - GPIOx pin is an output

The Mode Select register determines the type of output or input for each individual pin. Bits 7 - 4 specify either a level or edge sensitive input for GPIO7 - GPIO4. These bits have no effect if the corresponding port is configured as a output. Bits 3 - 0 select the output type for GPIO3 - GPIO0: either the corresponding bit in the Output Data register or the corresponding PWM output. These bits also have no effect if the corresponding port is configured as an input in GOER.

GMSR - GPIO Mode Select Register
Location E8

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN7	IN6	IN5	IN4	OT3	OT2	OT1	OT0

If DRx = 0:
INx = 0 - GPIOx pin is a level sensitive input
INx = 1 - GPIOx pin is an edge sensitive input
OTx has no effect

If DRx = 1:
OTx = 0 - GPIOx outputs the corresponding bit in GOUT
OTx = 1 - GPIOx outputs corresponding PWM output
INx has no effect

The Edge Select register is only used for inputs (GPIO7 - GPIO4) which are configured as edge select inputs. These determine if the inputs are triggered by rising or falling edges. Bits 3 - 0 are not used and always return a "0" when read.

GESR - GPIO Edge Select Register
Location E9

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ES7	ES6	ES5	ES4	0	0	0	0

f DRx = 0 AND INx = 1:
ESx = 0 - input port captures rising edge
ESx = 1 - input port captures falling edge

If DRx = 1 OR INx = 0:
ESx has no effect

REGISTER DESCRIPTION (continued)

GENERAL PURPOSE I/O (GPIO) (continued)

The Input and Output Data Registers allow the host to set the output state for level type output ports and read the state of level sensitve input ports. Whenever a port is configured as an output, its actual output level will be reflected in the Input Data register (the input is automatically configured as level sensitive regardless of the state if INx). This means that the host can read the Input Data register to confirm actual output levels.

If an input is configured as edge sensitive, the Input Data register indicates if the edge has occured (corresponding bit = 1). In order to use an edge detect input, the corresponding Output Data register bit must initially be set to a "0". The edge detector is cleared by writing a "1" to the corresponding bit in the Output Data register followed by writing a "0". This allows individual resets of the edge detectors.

GINP - GPIO Input Data Register
Location E5

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

If port is level sensitive input or output:
DIx = level at GPIOx pin

If port is edge sensitive input:
DIx = 0 - edge has not occurred
DIx = 1 - edge has occurred

GOUT - GPIO Output Data Register
Location E6

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

If port is level output:
DOx is output level control for GPIOx

If port is edge sensitive input:
DOx MUST = 0
Edge detector is reset by DOx = 1, followed by DOx = 0.

MEMORY MAP

FSPG RAM (GCR bit0 = 0)

Location	Name	Bit Description							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

SRAM - Spark Pulse RAM

00	SSTRH0	b15	0	0	0	Spark 0 start angle MSB
01	SSTRL0	Spark 0 start angle LSB				
02	SSTPH0	b15	0	0	0	Spark 0 stop angle MSB
03	SSTPL0	Spark 0 stop angle LSB				
04	SSTRH1	b15	0	0	0	Spark 1 start angle MSB
05	SSTRL1	Spark 1 start angle LSB				
06	SSTPH1	b15	0	0	0	Spark 1 stop angle MSB
07	SSTPL1	Spark 1 stop angle LSB				
08	SSTRH2	b15	0	0	0	Spark 2 start angle MSB
09	SSTRL2	Spark 2 start angle LSB				
0A	SSTPH2	b15	0	0	0	Spark 2 stop angle MSB
0B	SSTPL2	Spark 2 stop angle LSB				
0C	SSTRH3	b15	0	0	0	Spark 3 start angle MSB
0D	SSTRL3	Spark 3 start angle LSB				
0E	SSTPH3	b15	0	0	0	Spark 3 stop angle MSB
0F	SSTPL3	Spark 3 stop angle LSB				
10	SSTRH4	b15	0	0	0	Spark 4 start angle MSB
11	SSTRL4	Spark 4 start angle LSB				
12	SSTPH4	b15	0	0	0	Spark 4 stop angle MSB
13	SSTPL4	Spark 4 stop angle LSB				
14	SSTRH5	b15	0	0	0	Spark 5 start angle MSB
15	SSTRL5	Spark 5 start angle LSB				
16	SSTPH5	b15	0	0	0	Spark 5 stop angle MSB
17	SSTPL5	Spark 5 stop angle LSB				
18	SSTRH6	b15	0	0	0	Spark 6 start angle MSB
19	SSTRL6	Spark 6 start angle LSB				
1A	SSTPH6	b15	0	0	0	Spark 6 stop angle MSB
1B	SSTPL6	Spark 6 stop angle LSB				

REGISTER DESCRIPTION (continued)

MEMORY MAP (continued)

FSPG RAM (GCR bit0 = 0) (continued)

Location	Name	Bit Description							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

SRAM - Spark Pulse RAM (continued)

1C	SSTRH7	b15	0	0	0	Spark 7 start angle MSB
1D	SSTRL7	Spark 7 start angle LSB				
1E	SSTPH7	b15	0	0	0	Spark 7 stop angle MSB
1F	SSTPL7	Spark 7 stop angle LSB				

FRAM - Fuel Pulse RAM

20	FSTRH0	b15	0	0	0	Fuel 0 start angle MSB
21	FSTRL0	Fuel 0 start angle LSB				
22	FPTH0	Fuel 0 pulse time MSB				
23	FPTL0	Fuel 0 pulse time LSB				

24	FSTRH1	b15	0	0	0	Fuel 1 start angle MSB
25	FSTRL1	Fuel 1 start angle LSB				
26	FPTH1	Fuel 1 pulse time MSB				
27	FPTL1	Fuel 1 pulse time LSB				

28	FSTRH2	b15	0	0	0	Fuel 2 start angle MSB
29	FSTRL2	Fuel 2 start angle LSB				
2A	FPTH2	Fuel 2 pulse time MSB				
2B	FPTL2	Fuel 2 pulse time LSB				

2C	FSTRH3	b15	0	0	0	Fuel 3 start angle MSB
2D	FSTRL3	Fuel 3 start angle LSB				
2E	FPTH3	Fuel 3 pulse time MSB				
2F	FPTL3	Fuel 3 pulse time LSB				

30	FSTRH4	b15	0	0	0	Fuel 4 start angle MSB
31	FSTRL4	Fuel 4 start angle LSB				
32	FPTH4	Fuel 4 pulse time MSB				
33	FPTL4	Fuel 4 pulse time LSB				

Location	Name	Bit Description							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

FRAM - Fuel Pulse RAM (continued)

34	FSTRH5	b15	0	0	0	Fuel 5 start angle MSB
35	FSTRL5	Fuel 5 start angle LSB				
36	FPTH5	Fuel 5 pulse time MSB				
37	FPTL5	Fuel 5 pulse time LSB				

38	FSTRH6	b15	0	0	0	Fuel 6 start angle MSB
39	FSTRL6	Fuel 6 start angle LSB				
3A	FPTH6	Fuel 6 pulse time MSB				
3B	FPTL6	Fuel 6 pulse time LSB				

3C	FSTRH7	b15	0	0	0	Fuel 7 start angle MSB
3D	FSTRL7	Fuel 7 start angle LSB				
3E	FPTH7	Fuel 7 pulse time MSB				
3F	FPTL7	Fuel 7 pulse time LSB				

Location	Name	Description
40	FTMRH0	Fuel 0 duration timer MSB
41	FTMRL0	Fuel 0 duration timer LSB
42	FTMRH1	Fuel 1 duration timer MSB
43	FTMRL1	Fuel 1 duration timer LSB
44	FTMRH2	Fuel 2 duration timer MSB
45	FTMRL2	Fuel 2 duration timer LSB
46	FTMRH3	Fuel 3 duration timer MSB
47	FTMRL3	Fuel 3 duration timer LSB
48	FTMRH4	Fuel 4 duration timer MSB
49	FTMRL4	Fuel 4 duration timer LSB
4A	FTMRH5	Fuel 5 duration timer MSB
4B	FTMRL5	Fuel 5 duration timer LSB
4C	FTMRH6	Fuel 6 duration timer MSB
4D	FTMRL6	Fuel 6 duration timer LSB
4E	FTMRH7	Fuel 7 duration timer MSB
4F	FTMRL7	Fuel 7 duration timer LSB

TRAM - Fuel Pulse Duration Timer RAM (Read Only)

50 - BF		RESERVED

REGISTER DESCRIPTION (continued)

MEMORY MAP (continued)

EPT Configuration Memory (GCR bit0 = 1)

Location	Name	Description

CWRAM - Crank Wheel RAM

100	CWSP00	Spacing between teeth
101	CWTH00	Number of next to last tooth
102	CWSP01	Spacing between teeth
103	CWTH01	Number of next to last tooth
104	CWSP02	Spacing between teeth
105	CWTH02	Number of next to last tooth
106	CWSP03	Spacing between teeth
107	CWTH03	Number of next to last tooth
108	CWSP04	Spacing between teeth
109	CWTH04	Number of next to last tooth
10A	CWSP05	Spacing between teeth
10B	CWTH05	Number of next to last tooth
10C	CWSP06	Spacing between teeth
10D	CWTH06	Number of next to last tooth
10E	CWSP07	Spacing between teeth
10F	CWTH07	Number of next to last tooth
110	CWSP08	Spacing between teeth
111	CWTH08	Number of next to last tooth
112	CWSP09	Spacing between teeth
113	CWTH09	Number of next to last tooth
114	CWSP10	Spacing between teeth
115	CWTH10	Number of next to last tooth
116	CWSP11	Spacing between teeth
117	CWTH11	Number of next to last tooth
118	CWSP12	Spacing between teeth
119	CWTH12	Number of next to last tooth
11A	CWSP13	Spacing between teeth
11B	CWTH13	Number of next to last tooth
11C	CWSP14	Spacing between teeth
11D	CWTH14	Number of next to last tooth
11E	CWSP15	Spacing between teeth
11F	CWTH15	Number of next to last tooth

EPT Configuration Memory (GCR bit0 = 1) (continued)

Location	Name	Description

CWRAM - Crank Wheel RAM (continued)

120	CWSP16	Spacing between teeth
121	CWTH16	Number of next to last tooth
122	CWSP17	Spacing between teeth
123	CWTH17	Number of next to last tooth
124	CWSP18	Spacing between teeth
125	CWTH18	Number of next to last tooth
126	CWSP19	Spacing between teeth
127	CWTH19	Number of next to last tooth
128	CWSP20	Spacing between teeth
129	CWTH20	Number of next to last tooth
12A	CWSP21	Spacing between teeth
12B	CWTH21	Number of next to last tooth
12C	CWSP22	Spacing between teeth
12D	CWTH22	Number of next to last tooth
12E	CWSP23	Spacing between teeth
12F	CWTH23	Number of next to last tooth
130	CWSP24	Spacing between teeth
131	CWTH24	Number of next to last tooth
132	CWSP25	Spacing between teeth
133	CWTH25	Number of next to last tooth
134	CWSP26	Spacing between teeth
135	CWTH26	Number of next to last tooth
136	CWSP27	Spacing between teeth
137	CWTH27	Number of next to last tooth
138	CWSP28	Spacing between teeth
139	CWTH28	Number of next to last tooth
13A	CWSP29	Spacing between teeth
13B	CWTH29	Number of next to last tooth
13C	CWSP30	Spacing between teeth
13D	CWTH30	Number of Inext to ast tooth
13E	CWSP31	Spacing between teeth
13F	CWTH31	Number of next to last tooth

REGISTER DESCRIPTION (continued)

MEMORY MAP (continued)

EPT Configuration Memory (GCR bit0 = 1)

Location	Name	Description

PRRAM - Pattern Recognition RAM

140	PRACH1	Pattern 1 Angle Count High
141	PRACL1	Pattern 1 Angle Count Low
142	PRTNO1	Tooth number at that Angle Count
143	PRADD1	CWRAM address/2 of that tooth
144	PRACH2	Pattern 2 Angle Count High
145	PRACL2	Pattern 2 Angle Count Low
146	PRTNO2	Tooth number at that Angle Count
147	PRADD2	CWRAM address/2 of that tooth
148	PRACH3	Pattern 3 Angle Count High
149	PRACL3	Pattern 3 Angle Count Low
14A	PRTNO3	Tooth number at that Angle Count
14B	PRADD3	CWRAM address/2 of that tooth
14C	PRACH4	Pattern 4 Angle Count High
14D	PRACL4	Pattern 4 Angle Count Low
14E	PRTNO4	Tooth number at that Angle Count
14F	PRADD4	CWRAM address/2 of that tooth
150	PRACH5	Pattern 5 Angle Count High
151	PRACL5	Pattern 5 Angle Count Low
152	PRTNO5	Tooth number at that Angle Count
153	PRADD5	CWRAM address/2 of that tooth
154	PRACH6	Pattern 6 Angle Count High
155	PRACL6	Pattern 6 Angle Count Low
156	PRTNO6	Tooth number at that Angle Count
157	PRADD6	CWRAM address/2 of that tooth
158	PRACH7	Pattern 7 Angle Count High
159	PRACL7	Pattern 7 Angle Count Low
15A	PRTNO7	Tooth number at that Angle Count
15B	PRADD7	CWRAM address/2 of that tooth
15C	PRACH8	Pattern 8 Angle Count High
15D	PRACL8	Pattern 8 Angle Count Low
15E	PRTNO8	Tooth number at that Angle Count
15F	PRADD8	CWRAM address/2 of that tooth

EPT Configuration Memory (GCR bit0 = 1) (continued)

Location	Name	Bit Description							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Pattern Storage Registers

160	PATRN1	MSB	CBIT	Pattern 1 (6 bits)
161	PATRN2	MSB	CBIT	Pattern 2
162	PATRN3	MSB	CBIT	Pattern 3
163	PATRN4	MSB	CBIT	Pattern 4
164	PATRN5	MSB	CBIT	Pattern 5
165	PATRN6	MSB	CBIT	Pattern 6
166	PATRN7	MSB	CBIT	Pattern 7
167	PATRN8	MSB	CBIT	Pattern 8

Pattern Acquisition Registers

Pattern Aquisition Register 1

168	PAREG1	EOPNUM	CRKNUM

Pattern Acquisition Register 2

169	PAREG2	PBE	TYP	CDEDAT

Pattern Acquisition Register 3

16A	PAREG3	PATBT6	CNTCLK

Pattern Acquisition Register 4

16B	PAREG4	SOPTYP	EOPTYP

PSI Configuration Registers

Crank Input Configuration

16C	CRKCFG	INV	DEC	VTLOW	VTHIGH

Cam Input Configuration

16D	CAMCFG	INV	DEC	VTLOW	VTHIGH

REGISTER DESCRIPTION (continued)

MEMORY MAP (continued)

EPT Configuration Memory (GCR bit0 = 1)

Location	Name	Bit Description							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Test Registers									
16E	TEST1	TEST ONLY							
16F	TEST2	TEST ONLY							
Pattern Match Registers									
Pattern Match Register 1									
170	PMREG1	RES	0			NUMSEC			
Pattern Match Register 2									
171	PMREG2	0	IAE3	IAE7	0				
Pattern Match Register 3									
172	PMREG3	PULNUM							
Test Register									
173	PMREG4	TEST ONLY							
Pattern Match Register 5									
174 (175)	PMREG5	SPSDFT							
Test Registers									
176	PMREG6	TEST ONLY							
177	PMREG7	TEST ONLY							

EIP Control Register (GCR bit0 = X)

Loc.	Name	RESET Value	Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Angle Count Register

C0	ACNTH	07	0	0	0	0	AC11	AC10	AC9	AC8
C1	ACNTL	FF	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Sync Interrupt Status Register

C2	SISR	00	0	TO	IP	AP	ACLSB	ST360	ST720	ACMSB

EPT Sync Reset Register

C3	EPTRST	00	0	0	TSSEL	TANG	RST7	RST3

TEST Registers

C4	TMUX	00	TEST ONLY
C5	TREG1	00	TEST ONLY
C6	TREG2	00	TEST ONLY
C7 - DF			RESERVED

PWM Control Register

E0	PWMCTL	00	PRSC32	PRSC10

REGISTER DESCRIPTION (continued)

MEMORY MAP (continued)

EIP Control Register (GCR bit0 = X)

Loc.	Name	RESET Value	Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

PWM Output Duty Cycle Registers

E1	PWMDC0	00	PWM0 Duty Cycle
E2	PWMDC1	00	PWM1 Duty Cycle
E3	PWMDC2	00	PWM2 Duty Cycle
E4	PWMDC3	00	PWM3 Duty Cycle

GPIO Input Data Register

E5	GINP	00	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

GPIO Output Data Register

E6	GOUT	00	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

GPIO Output Enable Register

E7	GOER	00	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0

GPIO Mode Select Register

E8	GMSR	00	IN7	IN6	IN5	IN4	OT3	OT2	OT1	OT0

GPIO Edge Select Register

E9	GESR	00	ES7	ES6	ES5	ES4	0	0	0	0

EA - EF	RESERVED

EIP Control Register (GCR bit0 = X) (continued)

Loc.	Name	RESET Value	Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Interrupt Mask Register

F0	MASK	1F	0	0	0	EPTES	OSMSK	ISMSK	SMSK	FMSK

FSPG Spark Pulse Register

F1	SPRK	00	SPK7	SPK6	SPK5	SPK4	SPK3	SPK2	SPK1	SPK0

FSPG Fuel Pulse Register

F2	FUEL	00	FUEL7	FUEL6	FUEL5	FUEL4	FUEL3	FUEL2	FUEL1	FUEL0

Interrupt Register

F3	INT	00	LSYNC	SYNC3	SYNC7	0	FI3	FI2	FI1	SPKI

Fuel Timer Read Register

F4	TMRH	00	Fuel Time Elapsed MSB
F5	TMRL	00	Fuel Time Elapsed LSB

Global Configuration Register

F6	GCR	91	FDC	0	SHTDN	SDC	TST3	TST2	TST1	PG

Spark Mapping Register

F7	SMAP	00	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

FSOC Control Register

F8	FSOCTL	40	IIM	DMC	ILE	AFE	FFE	0	TI1	TI0

REGISTER DESCRIPTION (continued)

MEMORY MAP (continued)

EIP Control Register (GCR bit0 = X)

Loc.	Name	RESET Value	Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Dwell Timer Register

F9	DTIME	00	TIME

Spark Status Register 1

FA	SPKST1	00	STAT3	STAT2	STAT1	STAT0	SPKM3	SPKM2	SPKM1	SPKM0

Spark Status Register 2

FB	SPKST2	00	IDWL3	IDWL2	IDWL1	IDWL0	ILIM3	ILIM2	ILIM1	ILIM0

Fuel Fault 1 Register (Short to Battery)

FC	FF1	00	SHB7	SHB6	SHB5	SHB4	SHB3	SHB2	SHB1	SHB0

Fuel Fault 2 Register (Short to Ground)

FD	FF2	00	SHG7	SHG6	SHG5	SHG4	SHG3	SHG2	SHG1	SHG0

Fuel Fault 3 Register (Open Load)

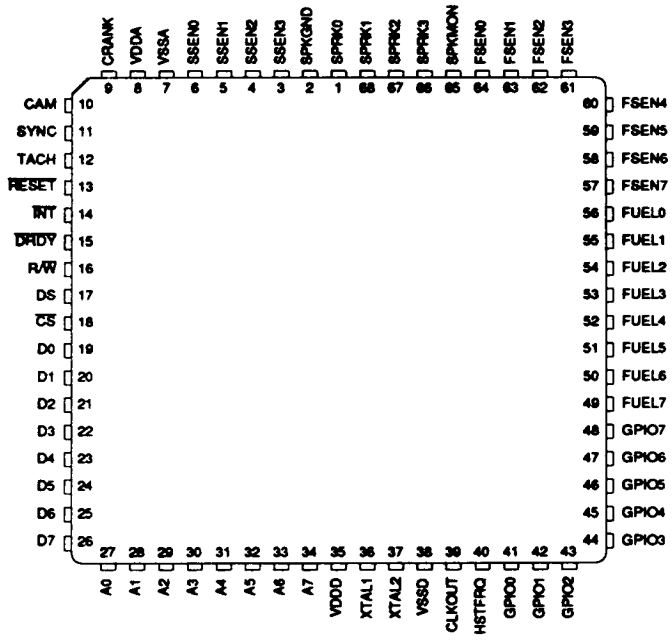
FE	FF3	00	FOL7	FOL6	FOL5	FOL4	FOL3	FOL2	FOL1	FOL0

Fuel State Register

FF	FST	00	FST7	FST6	FST5	FST4	FST3	FST2	FST1	FST0

PACKAGE PIN DESIGNATIONS

(Top View)



68-Pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 67F687 - 68-pin PLCC	67F687-IH	67F687-IH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX (714) 573-6914

