

54ACTQ533

Quiet Series Octal Transparent Latch with TRI-STATE® Outputs

General Description

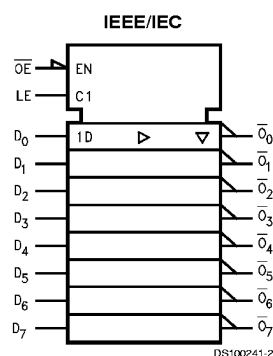
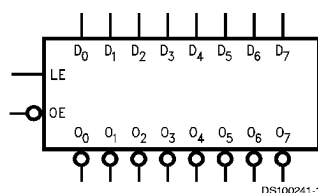
The ACTQ533 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

The ACTQ533 utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch up immunity
- Eight latches in a single package
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Inverted version of the ACTQ373
- 4 kV minimum ESD immunity

Logic Symbols

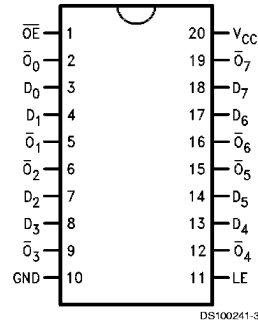


Pin Names	Description
D_0 – D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
$\overline{O}_0$ – $\overline{O}_7$	TRI-STATE Latch Outputs

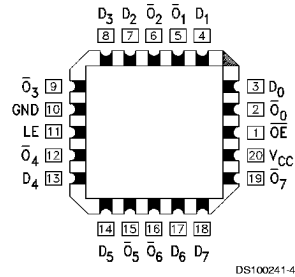
GTO™ is a trademark of National Semiconductor Corporation.
 TRI-STATE® is a registered trademark of National Semiconductor Corporation.
 FACT® is a registered trademark of Fairchild Semiconductor Corporation.
 FACT Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

Connection Diagrams

Pin Assignment
for DIP and Flatpak



Pin Assignment
for LCC



Functional Description

The ACTQ533 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	$\overline{O}_n$
X	H	X	Z
H	L	L	H
H	L	H	L
L	L	X	$\overline{O}_0$

H = HIGH Voltage Level

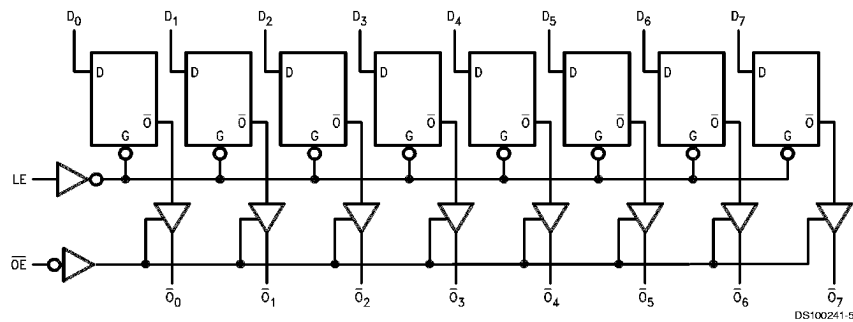
L = LOW Voltage Level

Z = High Impedance

X = Immaterial

$\overline{O}_0$ = Previous $\overline{O}_0$ before HIGH to Low transition of Latch Enable

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	–20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	–0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	–20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	–0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	–65°C to +150°C

DC Latchup Source

or Sink Current

±300 mA

Junction Temperature (T_J)

CDIP

175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54ACTQ	–55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

Note 2: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from –40°C to +125°C.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V _{CC} (V)	54ACTQ	Units	Conditions
			T _A = –55°C to +125°C		
			Guaranteed Limits		
V _{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V _{OUT} = 0.1V or V _{CC} – 0.1V
		5.5	2.0		
V _{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V _{OUT} = 0.1V or V _{CC} – 0.1V
		5.5	0.8		
V _{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I _{OUT} = –50 μA
		5.5	5.4		
		4.5	3.70	V	(Note 3) V _{IN} = V _{IL} or V _{IH} I _{OH} = –24 mA I _{OH} = –24 mA
		5.5	4.70		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I _{OUT} = 50 μA
		5.5	0.1		
		4.5	0.50	V	(Note 3) V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA
		5.5	0.50		
I _{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V _I = V _{CC} , GND
I _{OZ}	Maximum TRI-STATE Leakage Current	5.5	±5.0	μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	1.6	mA	V _I = V _{CC} – 2.1V

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	54ACTQ	Units	Conditions
			T _A = –55°C to +125°C		
			Guaranteed Limits		
I _{OLD}	Minimum Dynamic Output Current (Note 4)	5.5	50	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5	–50	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	80.0	μA	V _{IN} = V _{CC} or GND (Note 5)
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	1.7	V	(Notes 6, 7)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	–1.2	V	(Notes 6, 7)

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{CC} for 54ACTQ @ 25°C is identical to 74ACQ @ 25°C.

Note 6: Plastic DIP package.

Note 7: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 8)	54ACTQ		Units	Fig. No.
			T _A = –55° C to +125° C C _L = 50 pF			
			Min	Max		
t _{PHL} , t _{PLH}	Propagation Delay D _n to O _n	5.0	1.5	9.0	ns	
t _{PHL} , t _{PLH}	Propagation Delay LE to O _n	5.0	1.5	10.5	ns	
t _{PZL} , t _{PZH}	Output Enable Time	5.0	1.5	10.5	ns	
t _{PHZ} , t _{PLZ}	Output Disable Time	5.0	1.5	10.5	ns	

Note 8: Voltage Range 5.0 is 5.0V ±0.5V.

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

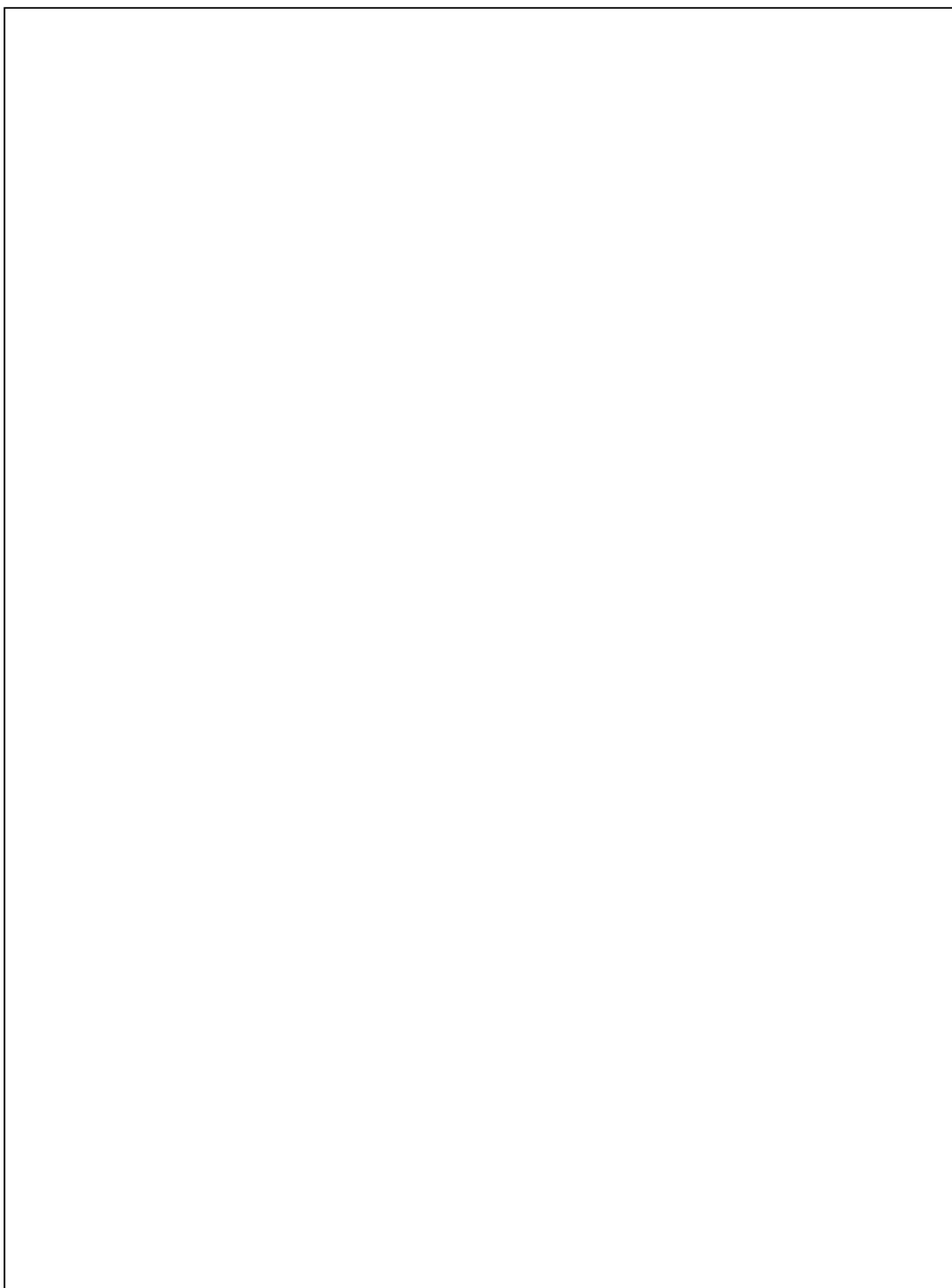
AC Operating Requirements

Symbol	Parameter	V _{CC} (V) (Note 10)	54ACTQ	Units	Fig. No.
			T _A = –55°C to +125°C C _L = 50 pF		
			Guaranteed Minimum		
t _S	Setup Time, HIGH or LOW D _n to LE	5.0	3.0	ns	
t _H	Hold Time, HIGH or LOW D _n to LE	5.0	1.5	ns	
t _W	LE Pulse Width, HIGH	5.0	5.0	ns	

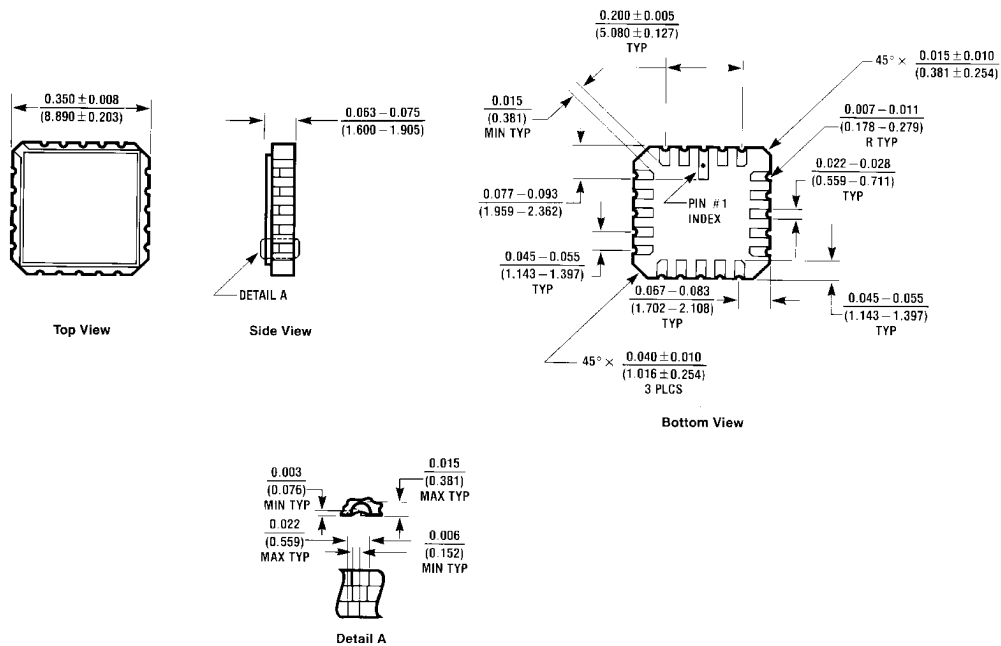
Note 10: Voltage Range 5.0 is 5.0V ±0.5V.

Capacitance

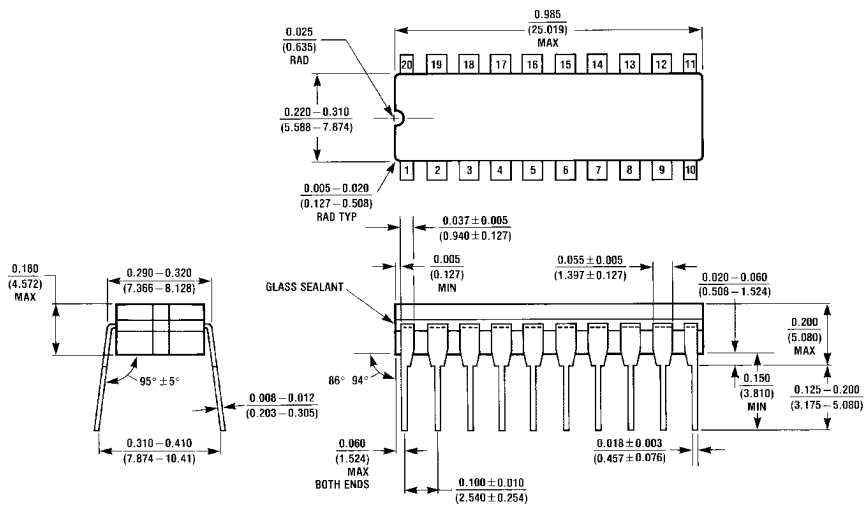
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	40	pF	V _{CC} = 5.0V



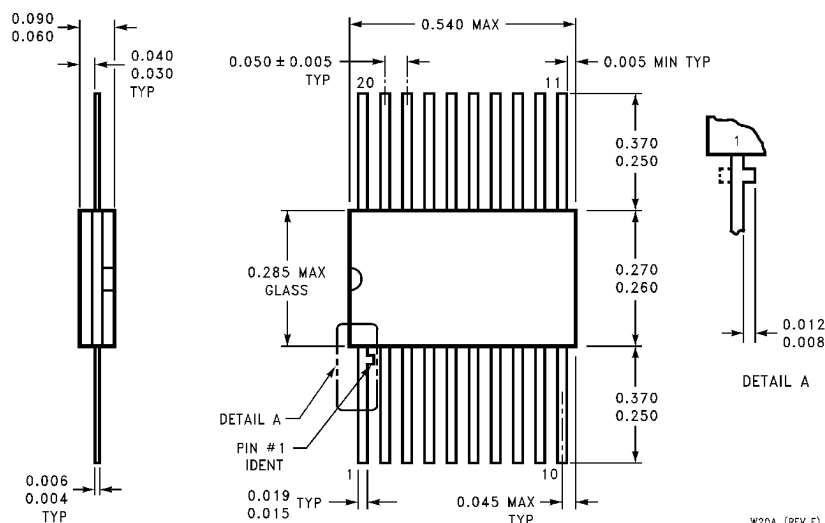
Physical Dimensions inches (millimeters) unless otherwise noted



**20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A**



**20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

20-Lead Ceramic Flatpak (F)
NS Package Number W20A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor
Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor
Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor
Asia Pacific Customer
Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor
Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.