Octal buffer/line driver with parity, inverting (3-State) 54F455

FEATURES

- High impedance NPN base inputs for reduced loading (20μA in High and Low states)
- 54F455 combines 54F240 and 54F280A functions in one package
- 54F455A is a center pin version of the 54F655A.
- 54F455 Inverting
- 3-State outputs sink 48mA and source 12mA
- 24-pin slim DIP (300 mil) package
- Inputs on one side and outputs on the other side simplify PC board layout
- Center power and ground to reduce ground bounce and system noise

DESCRIPTION

The 54F455 is an octal buffers and line driver with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. This part includes parity generator/checker to improve PC board density.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24-Pin Ceramic DIP	54F455/BLA	GDIP3-T24
24-Pin Ceramic Flat Pack	54F455/BKA	GDFP2-F24

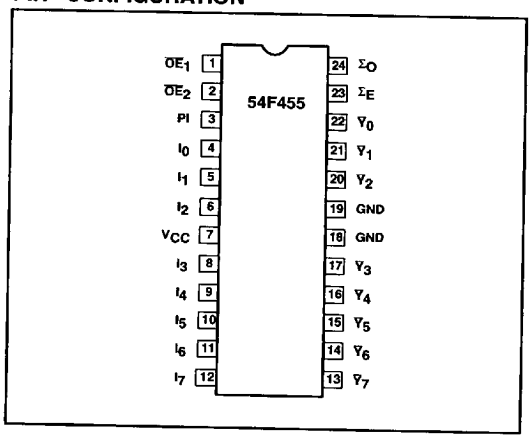
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

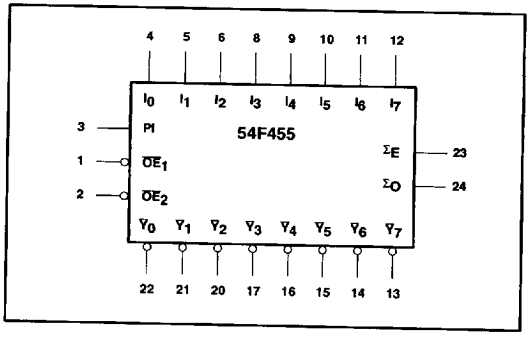
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_n	Data inputs	1.0/0.033	20μA/20μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_1$, $\overline{OE}_2$	3-State output enable inputs (active Low)	1.0/0.033	20μA/20μA
$\overline{Y}_n$	Data outputs (54F455)	600/80	12mA/48mA
Σ_E, Σ_O	Parity outputs	600/80	12mA/48mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

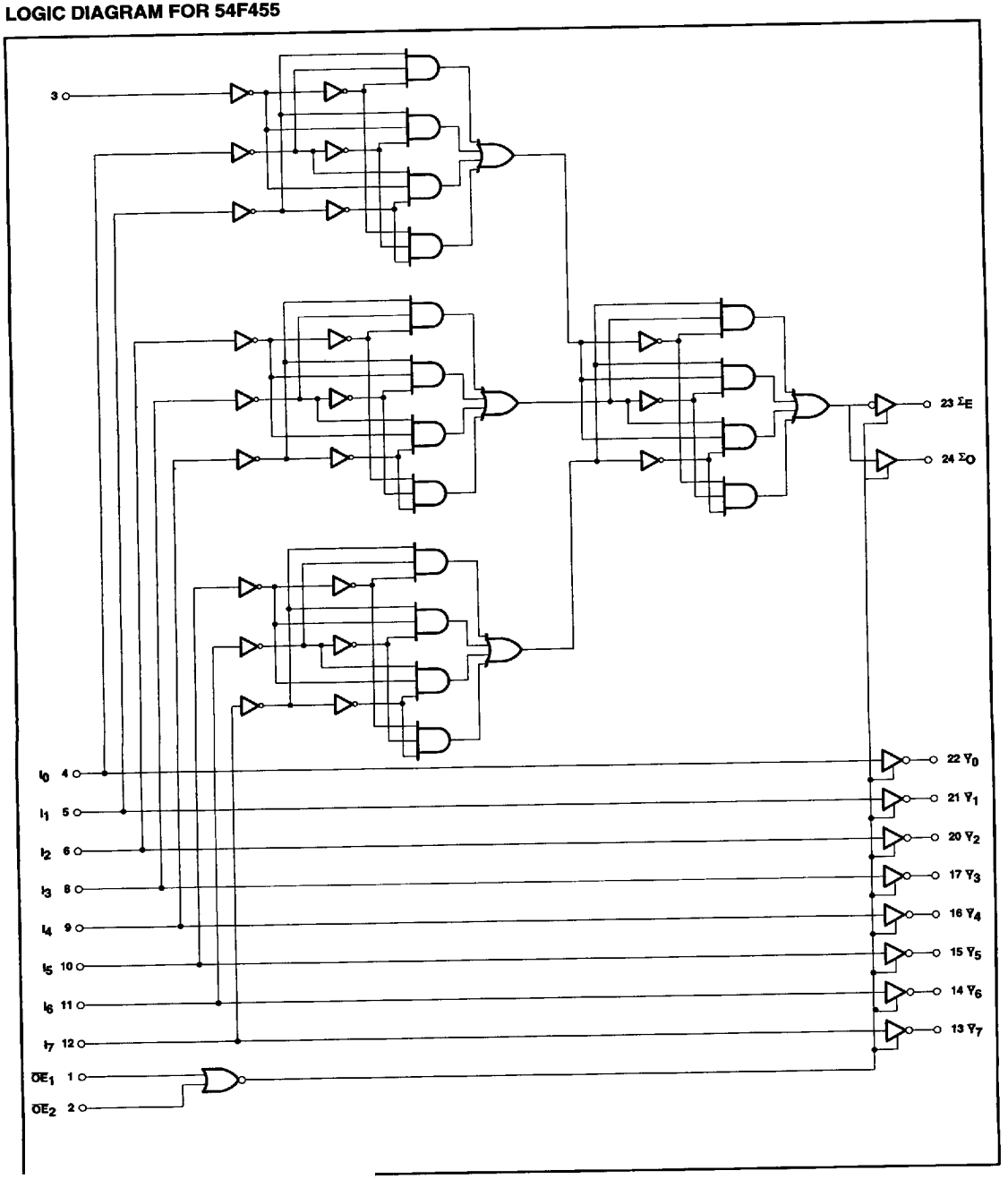
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC DIAGRAM FOR 54F455



FUNCTION TABLES

INPUTS			DATA OUTPUTS
$\overline{OE}_1$	$\overline{OE}_2$	I_N	54F455
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance level

INPUTS	PARITY OUTPUTS	
Number of inputs, High (PI, I_0 - I_7)	Σ_E	Σ_O
Even - 0, 2, 4, 6, 8	H	L
Odd - 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = High	Z	Z

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	96	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH1}	High-level output current			-1	mA
I_{OH2}	High-level output current			-3	mA
I_{OH3}	High-level output current			-12	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH2} = -3mA	2.4			V
				I_{OH1} = -1mA	2.5			V
				I_{OH3} = -12mA	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = 48mA			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V				-20	µA
I_{OZH}	Off-state current High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				50	µA
I_{OZL}	Off-state current Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			50	80	mA
		I_{CCL}				78	110	mA
		I_{CCZ}				63	90	mA

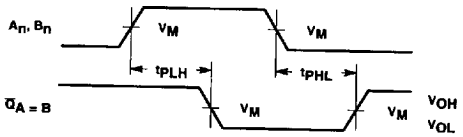
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n (54F455)	Waveform 1	2.0 1.0	4.5 2.0	6.5 4.0	2.0 1.0	8.0 5.5	ns ns
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_E, Σ_O	Waveform 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	15.0 18.0	ns ns
t_{PZH} t_{PZL}	Enable time to High level Enable time to Low level	Waveform 2 Waveform 3	4.0 4.5	7.0 8.0	9.5 10.5	3.0 4.5	11.5 13.5	ns ns
t_{PLH} t_{PHL}	Disable time from High level Disable time from Low level	Waveform 2 Waveform 3	1.5 2.0	4.0 5.0	6.5 7.5	1.5 2.0	8.0 9.0	ns ns

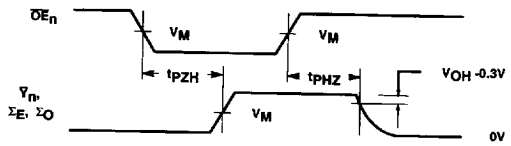
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

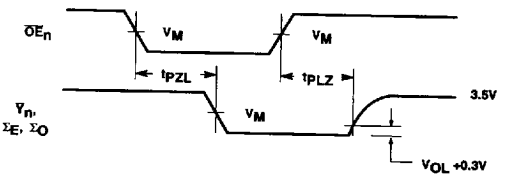
AC WAVEFORMS



Waveform 1. Propagation Delay for I_n to Σ_E, Σ_O, $\forall_n$



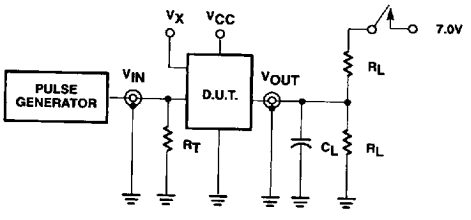
Waveform 2. 3-State Output Enable time to High level and Output Disable time from High level



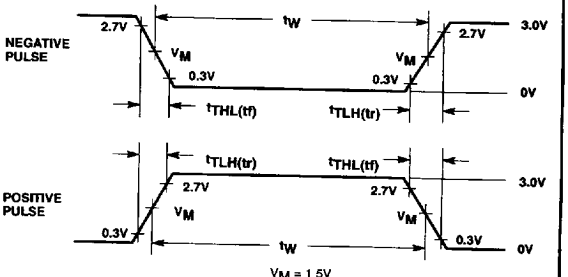
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.