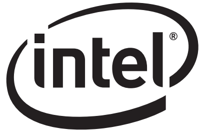

82562EZ(EX)/82547GI(EI) Dual Footprint

Design Guide

Networking Silicon

317520-002
Revision 2.2

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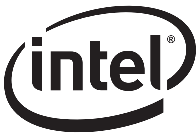
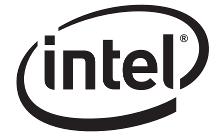


Revision History

Revision	Revision Date	Description
0.25	Jul 2002	Initial publication of preliminary design guide information.
0.75	Sep 2002	Published revised design guide information: • Added information on EEPROM settings • Added design checklist • Revised reference design schematic • Revised Ball Number to signal mapping Table to conform to changes in 82547EI datasheet rev 0.75
1.0	Oct 2002	Published revised design guide information: • Added layout checklist • Updated LAN disable circuit • Removed EEPROM information due to publication of separate guides
1.5	Sep 2003	Published revised design guide information: • Added 82547GI coverage • Removed Confidential status • Updated schematics, removed redundant caps • Revised LAN disable circuit
1.6	Nov 2004	Added crystal start-up information. Information includes: • New crystal parameters • Crystal selection guidelines • Crystal validation methods • Crystal testing methods Changed signal name FL_SO to the correct signal name FLSH_SO. Added 82562EX applicability. Added new values for TX and RX terminations (next to LAN silicon). New values are now 110 Ω for both TX and RX terminations. Added new starting values for RBIAS100 and RBIAS10. New starting values are now 649 Ω for RBIAS100 and 619 Ω for RBIAS10. Updated reference schematics to reflect new Tx and Rx termination values, new LAN disable circuit, and RBIAS100/RBIAS10 values. Removed excess capacitors and changed pins F12 and H12 to no connects. Added a 1K Ω resistor to pin A13 output.
1.7	Jan 2005	• Changed text in the Catalyst EEPROM revision H table note from “Revision H or higher not supported” to “Revision H is not supported”. • Removed the Design and Layout Checklists. These checklists are now separate Microsoft* Excel spreadsheets.
1.8	Jan 2005	Updated reference schematics to reflect current differential pair termination resistor values for the 82547GI/EI. Updated section 4.2.1 “Termination Resistors for Designs Based on 82562EZ/EX PLC Device” to reflect current resistor and RBIAS values. Updated section 4.3.1 “Termination Resistors for Designs Based on 8257GI(EI) Gigabit Ethernet Controller” to reflect current resistor values.
1.9	June 2006	Updated reference schematics for signals EE_MODE and JTAG_TRST# (changed resistor values from 1 K Ω to 100 Ω).
2.0	Feb 2007	Updated sections 3.1.3, 3.1.1.8, and Table 5 in section 3.1.1 (changed max ESR rate from 20 Ω to 10 Ω for the 82547GI/EI).
2.1	June 2007	Updated reference schematics: sheets 4 and 6.
2.2	Jan 2008	Added Table 6; approved crystals for the 82547GI(EI).



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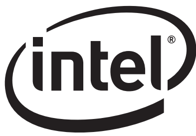

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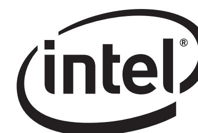

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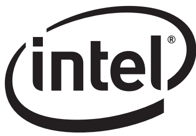

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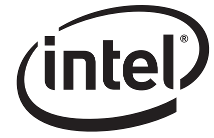

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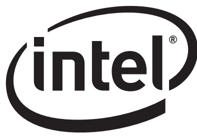


1.0 Introduction

Intel currently supports several footprint compatible Ethernet options depending upon the target application. The term “footprint compatible” means that the silicon devices are all manufactured in a 15 mm x 15 mm, 196-ball grid array package with the same ball pattern. Many of the critical signal pin locations are identical, allowing designers to create a single LAN on Motherboard (LOM) design that accommodates all devices. This is a flexible, cost-effective, multipurpose design technique that allowing maximized value while matching performance needs.

Note: Since some of the signal pins have different usages, the term “pin-compatible” is not applicable.

Available LAN components with the same footprint include the 82547GI(EI) Gigabit Ethernet Controller and the 82562EZ(EX) Platform LAN Connect components.

The LAN component used on a specific platform depends on the end user’s need for connection speed and manageability. As the requirements change, footprint compatibility makes it possible to re-focus the platform without the need to redesign a new a motherboard.

Table 1. LAN Component Connections/Features

LAN Component	Interface	Connection	Features
Intel® 82547GI(EI)	CSA	Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting	Gigabit Ethernet, ASF 2.0 alerting
Intel® 82562EX (196 BGA)	LCI	10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting
Intel® 82562EZ (196 BGA)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

1.1 Scope

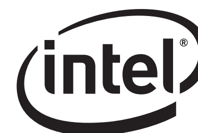
This application note contains Ethernet design guidelines applicable to LOM designs based on the Intel® 865 Chipset and Intel® 875 Chipset. The document identifies similarities and differences between the 82562EZ(EX) Platform LAN Connect device and the 82547GI(EI) Gigabit Ethernet Controller.

Section 2 describes the port interfaces specific to each device.

Section 3 explains what you need to know to hook up an Ethernet device to the system.

Section 4 describes board layout techniques applicable to these devices.

Section 5 provides a reference to the design and layout checklists.



Section 6 compares pin names and numbers between the two components.

Section 7 concludes with a reference design schematic of the full dual footprint configuration.

Note: It is assumed that the reader is acquainted with high-speed design and board layout techniques. Additional documents may be referred to for further information.

1.2 Reference Documents

- 82547GI(EI) Gigabit Ethernet Controller Datasheet. Intel Corporation.
- 82562EZ 10/100 Mbps Platform LAN Connect (PLC) Networking Silicon Datasheet. Intel Corporation.
- 82562ET/EM Platform LAN Connect Printed Circuit Board Design Guide. Intel Corporation.
- 82547GI(EI)/82541(PI/GI/EI)/82541ER EEPROM Map and Programming Information. Intel Corporation.
- ICH2 Integrated LAN Controller Function Disable and Power Control. Intel Corporation.
- PCI Bus Power Management Interface Specification, Rev. 1.1, PCI Special Interest Group.
- IEEE Standard 802.3, 2000 Edition. Incorporates various IEEE standards previously published separately.
- I/O Control Hub 2, 3, and 4 EEPROM Map and Programming Information. Intel Corporation.
- I/O Control Hub 5, 6, and 7 EEPROM Map and Programming Information. Intel Corporation.

Programming information can be obtained through your local Intel representative.

1.3 Product Codes

Table 2 lists the product ordering codes for the 82562EZ(EX)and 82547GI(EI).

Table 2. Product Ordering Codes

Device	Product Code	Product Code (Lead Free)
82562EZ	GD82562EZ	LU82562EZ
82562EX	GD82562EX	LU82562EX
82547GI	GD82547GI	LU82547GI
82547EI	GD82547EI	LU82547EI

2.0 System Data Port Interfaces

The 82562EZ(EX) Platform LAN Connect Device and the 82547GI(EI) Gigabit Ethernet controller employ different system interfaces, as illustrated in Figure 1.

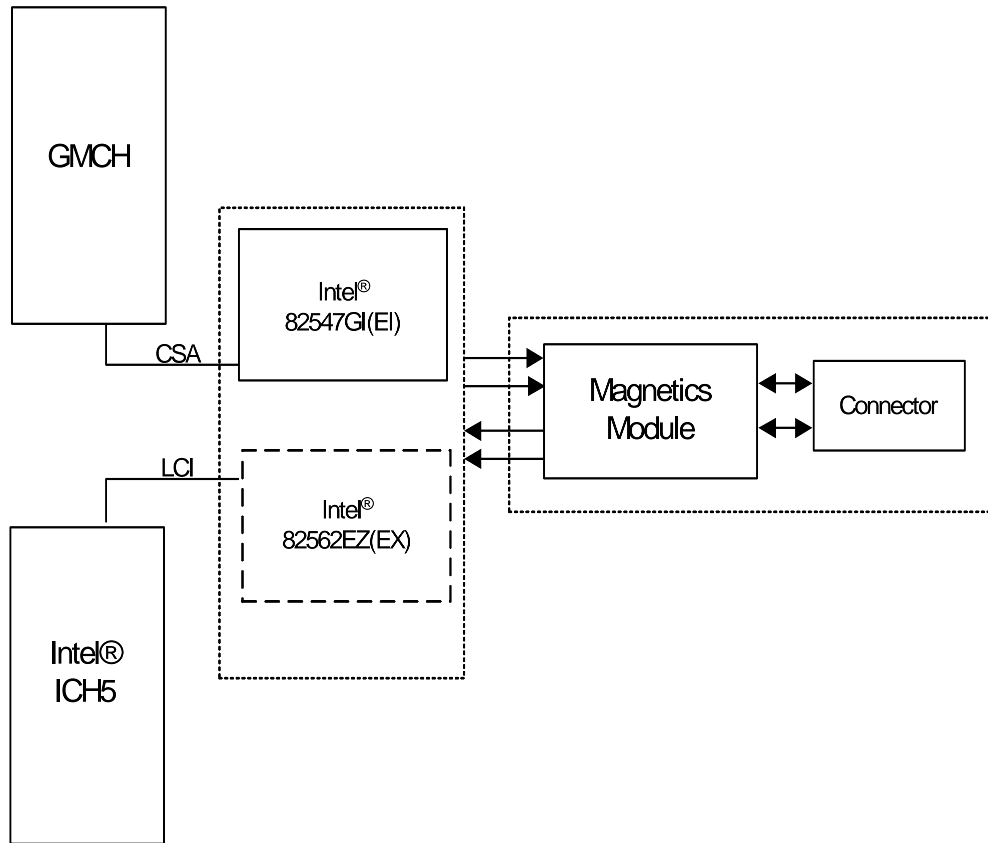


Figure 1. ICH5 Platform LAN Connect Sections

2.1 LCI Connection to 82562EZ(EX) Platform LAN Connect Device

The 82562EZ(EX) Platform LAN Connect device uses the LAN Connect Interface (LCI) to connect to the I/O Control Hub 5 (ICH5). LCI is a point-to-point interface optimized to support one device.

Line termination mechanisms are not specified for the LCI. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, undershoot and ringing.

For details about how to connect the LCI interface between the 82562EZ(EX) Platform LAN Connect device and ICH5, please refer to the 82562ET/EM Platform LAN Connect Printed Circuit Board (PCB) Design Guide, the Intel® 865 Chipset design guide, or the Intel® 875 Chipset design guide.

2.2 CSA Port Connection to 82547GI(EI) Gigabit Ethernet Controller

The 82547GI(EI) Gigabit Ethernet Controller uses the Communications Streaming Architecture (CSA) port to connect to the Memory Control Hub (MCH). CSA is a point-to-point interface supporting one device.

CSA has a theoretical bandwidth of 266 MB/s, sufficient to support Gigabit Ethernet speeds. The connection to the MCH places the Ethernet controller close to system memory for minimum latency.

The CSA interface uses IGTL buffers to achieve very high data speeds while controlling transmission line characteristics. For details on connecting the CSA interface between the 82547GI(EI) Gigabit Ethernet Controller and the MCH, please refer to the Intel® 865 Chipset design guide, or the Intel® 875 Chipset design guide.

2.2.1 Generation/Distribution of Reference Voltages

The 11-bit CSA port on the 82547GI(EI) controller has a dedicated CI_VREF pin to sample the reference voltage. The nominal CSA port reference voltage is 0.35 V ± 3%. In addition to the reference voltage, a reference swing voltage, CI_SWING must be supplied to control buffer voltage swing characteristics. The nominal CSA port reference voltage swing must be 0.8 V ± 3%.

Table 3. CSA Port Reference Circuit Specifications

Reference Voltage Specification (V)	Reference Swing Voltage Specification (V)	1.2 V Voltage Divider Circuit Recommended Resistor Values (Ω)
0.350 ± 3%	0.8 ± 3%	R1 = 523 ± 1% R2 = 665 ± 1% R3 = 604 ± 1%

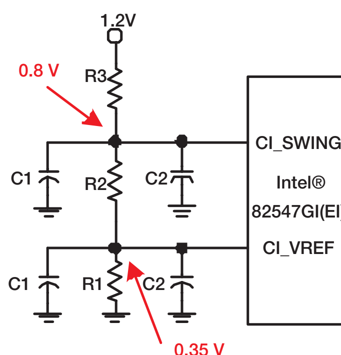
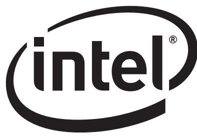


Figure 2. CSA Port Locally Generated Reference Divider Circuits



The values of R1, R2 and R3 must be rated at ±1% tolerance. The selected resistor values must also ensure that the reference voltage and reference swing voltage tolerance are maintained over the input leakage specification. A 0.1 µF capacitor (C1 in Figure 2) should be placed within 0.5 inches to each resistor divider, and a 0.01 µF bypass capacitor (C2 in Figure 2) should be placed within 0.25 inches of reference voltage pins. If the length of the trace from the voltage divider to the pin is greater than 1 inch, place more than one 0.01 µF capacitor near the reference voltage pin. The trace length from the voltage divider circuit to the CI_REF pins must be no longer than 3.5 inches.

Both the voltage reference and voltage swing reference signals should be routed at least 10mils wide and spaced at least 20 mils from all other signals.

2.2.2 CSA Port Resistive Compensation

The CSA port uses a resistive compensation signal (CI_RCOMP) to compensate buffer characteristics for temperature, voltage, and process.

Table 4. CSA Port CI_RCOMP Resistor Values

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied To
Intel® 82547GI(EI)	60 Ω ± 15%	R1 = 30.1 Ω ± 1%	VCC1.2

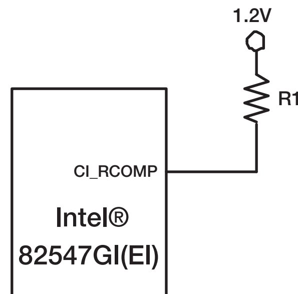
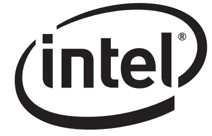


Figure 3. CSA port CI_RCOMP Circuits



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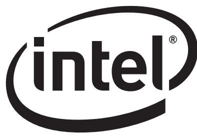


3.0 Ethernet Component Design Guidelines

These sections provide recommendations for selecting components and connecting special pins. The main design elements are the 82562EZ(EX) Platform LAN Connect device or the 82547GI(EI) Gigabit Ethernet Controller, an integrated magnetics module with RJ-45 connector, and a crystal clock source.

3.1 General Design Considerations for Ethernet Controllers

These recommendations apply to all designs, 10/100 or 10/100/1000 Mb/s.

Follow good engineering practices with respect to unused inputs by terminating them with pull-up or pull-down resistors, unless the data sheet, design guide or reference schematic indicates otherwise. Do not attach pull-up or pull-down resistors to any balls identified as No Connect. These devices may have special test modes that could be entered inadvertently.

3.1.1 Crystal Selection Parameters

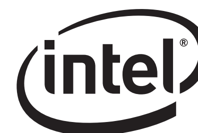
Quartz crystals are generally considered to be the mainstay of frequency control components due to their low cost and ease of implementation. They are available from numerous vendors in many package types and with various specification options.

All crystals used with Intel® Ethernet controllers are described as “AT-cut”, which refers to the angle at which the unit is sliced with respect to the long axis of the quartz stone.

Table 5 lists the crystal electrical parameters and provides suggested values for typical designs. The parameters listed are described in the following subsections.

Table 5. Crystal Parameters

Parameter	Suggested Value
Vibration Mode	Fundamental
Nominal Frequency	25,000 MHz at 25° C (required)
Frequency Tolerance	• ±30 ppm recommended; ±50 ppm across the entire operating temperature range as required by IEEE specifications • ±30 ppm required for the 82547GI(EI)
Temperature Stability	• ±50 ppm at 0° C to 70° C • ±30 ppm at 0° C to 70° C required for the 82547GI(EI)
Calibration Mode	Parallel
Load Capacitance	• 16 pF to 20 pF • 18 pF required for the 82547GI(EI)
Shunt Capacitance	6 pF maximum
Equivalent Series Resistance	• 50 Ω maximum • 10 Ω maximum required for the 82547GI(EI)
Drive Level	0.5 mW maximum
Aging	±5 ppm per year maximum



.Table 6 lists the approved crystals for use with the 83547GI(EI) B1 steppings.

Table 6. 82547GI(EI) Recommended Crystals

Manufacturer	Manufacturer's Part Number
Raltron (<20 Ω ESR and +/-30 ppm)	AS-25.000-20-F-SMD-TR
TXC	6C25000355

3.1.1.1 Vibration Mode

Crystals in the frequency range listed in Table 5 are available in both fundamental and third overtone. Unless there is a special need for third overtone, use fundamental mode crystals.

At any given operating frequency, third overtone crystals are thicker and more rugged than fundamental mode crystals. Third overtone crystals are more suitable for use in military or harsh industrial environments. Third overtone crystals require a trap circuit (extra capacitor and inductor) in the load circuitry to suppress fundamental mode oscillation as the circuit powers up. Selecting values for these components is beyond the scope of this document.

3.1.1.2 Nominal Frequency

Intel® Ethernet controllers use a crystal frequency of 25.000 MHz. The 25 MHz input is used to generate a 125 MHz transmit clock for 100BASE-TX and 1000BASE-TX operation; 10 MHz and 20 MHz transmit clocks, for 10BASE-T operation.

3.1.1.3 Frequency Tolerance

The frequency tolerance for an Ethernet physical layer device is dictated by the IEEE 802.3 specification as ±50 parts per million (ppm). This measurement is referenced to a standard temperature of 25° C.

Note: Intel recommends a frequency tolerance of ±30 ppm.

3.1.1.4 Temperature Stability and Environmental Requirements

Temperature stability is a standard measure of how the oscillation frequency varies over the full operational temperature range (and beyond). Several optional temperature ranges are currently available, including -40° C to +85° C for industrial environments. Some vendors separate operating temperatures from temperature stability. Manufacturers may also list temperature stability as 50 ppm in their data sheets.

Note: Crystals also carry other specifications for storage temperature, shock resistance, and reflow solder conditions. Crystal vendors should be consulted early in the design cycle to discuss the application and its environmental requirements.

3.1.1.5 Calibration Mode

The terms “series-resonant” and “parallel-resonant” are often used to describe crystal circuits. Specifying parallel mode is critical to determining how the crystal frequency is calibrated at the factory.

A crystal specified and tested as series resonant oscillates without problem in a parallel-resonant circuit, but the frequency is higher than nominal by several hundred parts per million. The purpose of adding load capacitors to a crystal circuit is to establish resonance at a frequency higher than the crystal's inherent series resonant frequency.

Figure 4 illustrates a simplified schematic of the 82562EZ(EX) and the 82547GI(EI) controller's crystal circuit. The crystal and the capacitors form a feedback element for the internal inverting amplifier. This combination is called parallel-resonant, because it has positive reactance at the selected frequency. In other words, the crystal behaves like an inductor in a parallel LC circuit.

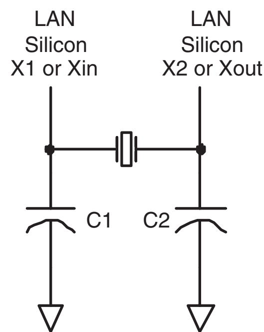


Figure 4. Crystal Circuit

3.1.1.6 Load Capacitance

The formula for crystal load capacitance is as follows:

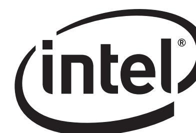
$$C_L = \frac{(C1 \cdot C2)}{(C1 + C2)} + C_{stray}$$

where C1 = C2 = 22 pF (as suggested in most Intel reference designs)

and C_{stray} = allowance for additional capacitance in pads, traces and the chip carrier within the Ethernet controller package

An allowance of 3 pF to 7 pF accounts for lumped stray capacitance. The calculated load capacitance is 16 pF with an estimated stray capacitance of about 5 pF.

Individual stray capacitance components can be estimated and added. For example, surface mount pads for the load capacitors add approximately 2.5 pF in parallel to each capacitor. This technique is especially useful if Y1, C1 and C2 must be placed farther than approximately one-half (0.5) inch from the controller. It is worth noting that thin circuit boards generally have higher stray capacitance than thick circuit boards.



Standard capacitor loads used by crystal manufacturers include 16 pF, 18 pF and 20 pF. Any of these values will generally operate with the controller. However, a difference of several picofarads between the calibrated load and the actual load will pull the oscillator slightly off frequency.

Note: C1 and C2 may vary by as much as 5% (approximately 1 pF) from their nominal values.

3.1.1.7 Shunt Capacitance

The shunt capacitance parameter is relatively unimportant compared to load capacitance. Shunt capacitance represents the effect of the crystal's mechanical holder and contacts. The shunt capacitance should equal a maximum of 6 pF (7 pF is also acceptable).

3.1.1.8 Equivalent Series Resistance

Equivalent Series Resistance (ESR) is the real component of the crystal's impedance at the calibration frequency, which the inverting amplifier's loop gain must overcome. ESR varies inversely with frequency for a given crystal family. The lower the ESR, the faster the crystal starts up. Use crystals with an ESR value of 50 Ω or better.

Note: Check the specific controller documentation carefully; some devices may have tighter ESR requirements. For example, Intel recommends that 82547GI(EI) devices use crystals with an ESR value of 10 Ω or less.

3.1.1.9 Drive Level

Drive level refers to power dissipation in use. The allowable drive level for a Surface Mounted Technology (SMT) crystal is less than its through-hole counterpart, because surface mount crystals are typically made from narrow, rectangular AT strips, rather than circular AT quartz blanks.

Some crystal data sheets list crystals with a maximum drive level of 1 mW. However, Intel® Ethernet controllers drive crystals to a level less than the suggested 0.5 mW value. This parameter does not have much value for on-chip oscillator use.

3.1.1.10 Aging

Aging is a permanent change in frequency (and resistance) occurring over time. This parameter is most important in its first year because new crystals age faster than old crystals. Use crystals with a maximum of ±5 ppm per year aging.

3.1.2 Reference Crystal

The normal tolerances of the discrete crystal components can contribute to small frequency offsets with respect to the target center frequency. To minimize the risk of tolerance-caused frequency offsets causing a small percentage of production line units to be outside of the acceptable frequency range, it is important to account for those shifts while empirically determining the proper values for the discrete loading capacitors, C1 and C2.

Even with a perfect support circuit, most crystals will oscillate slightly higher or slightly lower than the exact center of the target frequency. Therefore, frequency measurements (which determine the correct value for C1 and C2) should be performed with an ideal reference crystal. When the capacitive load is exactly equal to the crystal's load rating, an ideal reference crystal will be perfectly centered at the desired target frequency.

3.1.3 Reference Crystal Selection

There are several methods available for choosing the appropriate reference crystal:

- If a Saunders and Associates (S&A) crystal network analyzer is available, then discrete crystal components can be tested until one is found with zero or nearly zero ppm deviation (with the appropriate capacitive load). A crystal with zero or near zero ppm deviation will be a good reference crystal to use in subsequent frequency tests to determine the best values for C1 and C2.
- If a crystal analyzer is not available, then the selection of a reference crystal can be done by measuring a statistically valid sample population of crystals, which has units from multiple lots and approved vendors. The crystal, which has an oscillation frequency closest to the center of the distribution, should be the reference crystal used during testing to determine the best values for C1 and C2.
- It may also be possible to ask the approved crystal vendors or manufacturers to provide a reference crystal with zero or nearly zero deviation from the specified frequency when it has the specified CLoad capacitance.

Note: For 82547GI(EI) devices, Intel® recommends choosing a crystal with a ESR value of 10 Ω or less, an equivalent Cload of 18 pF, and a maximum of 30 ppm frequency shift. Cload is defined to be the load capacitance of the crystal, specified by the crystal vendor.

When choosing a crystal, customers must keep in mind that to comply with IEEE specifications for 10/100 and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be precise within ±50 ppm. Intel® recommends customers to use a transmitter reference frequency that is accurate to within ±30 ppm to account for variations in crystal accuracy due to crystal manufacturing tolerance. For information about measuring transmitter reference frequency, refer to Appendix A, “Measuring LAN Reference Frequency Using a Frequency Counter”.

3.1.4 Circuit Board

Since the dielectric layers of the circuit board are allowed some reasonable variation in thickness, the stray capacitance from the printed board (to the crystal circuit) will also vary. If the thickness tolerance for the outer layers of dielectric are controlled within ±17 percent of nominal, then the circuit board should not cause more than ±2 pF variation to the stray capacitance at the crystal. When tuning crystal frequency, it is recommended that at least three circuit boards are tested for frequency. These boards should be from different production lots of bare circuit boards.

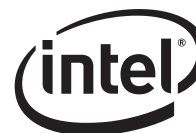
Alternatively, a larger sample population of circuit boards can be used. A larger population will increase the probability of obtaining the full range of possible variations in dielectric thickness and the full range of variation in stray capacitance.

Next, the exact same crystal and discrete load capacitors (C1 and C2) must be soldered onto each board, and the LAN reference frequency should be measured on each circuit board.

The circuit board, which has a LAN reference frequency closest to the center of the frequency distribution, should be used while performing the frequency measurements to select the appropriate value for C1 and C2.

3.1.5 Temperature Changes

Temperature changes can cause the crystal frequency to shift. Therefore, frequency measurements should be done in the final system chassis across the system’s rated operating temperature range.



3.1.6 Integrated Magnetics Module

The magnetics module has a critical effect on overall IEEE and regulatory conformance. The device should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Occasionally, components that meet basic specifications may cause the system to fail IEEE testing because of interactions with other components or the printed circuit board itself. Carefully qualifying new magnetics modules can go a long way toward preventing this type of problem.

The steps involved in magnetics module qualification are similar to those for oscillator qualification:

1. Verify that the vendor's published specifications in the component datasheet meet the required IEEE specifications.
2. Independently measure the component's electrical parameters on the test bench, checking samples from multiple lots. Check that the measured behavior is consistent from sample to sample as well as meeting the published specifications.
3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems. Vary temperature and voltage while performing system level tests (for IEEE only).

Magnetics modules for 1000BASE-T Ethernet are similar to those designed solely for 10/100 Mbps, with the exception of four differential signal pairs instead of two for 10/100 Mbps.

3.2 Designing with the 82562EZ(EX) Platform LAN Connect Device

This section provides design guidelines specific to the PLC device.

3.2.1 82562EZ/EX PLC Device LAN Disable Guidelines

Note: ICHx Integrated LAN Controller resides on the ICHx VccSus3_3 and VccSus1_8 power wells (typically referred to as “auxiliary” (“aux”) or “standby” supplies at the platform level).

The ICHx Integrated LAN’s RST# is the ICHx Resume-well input. It can be held low indefinitely to keep the ICHx Integrated LAN Controller in a reset state. The LAN Reset (RST#) signal must not be deasserted sooner than 10 ms after the Resume power supply reaches its nominal voltage. This ensures that the ICHx Integrated LAN Controller is initialized. Figure 5 illustrates a possible solution for ICHx Integrated LAN disable.

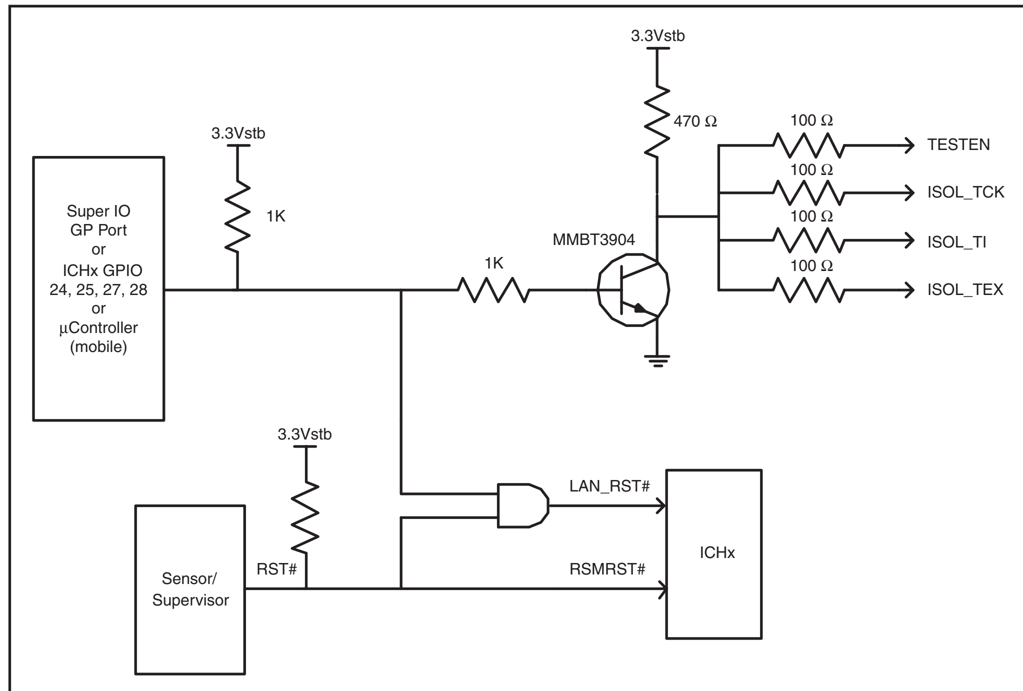


Figure 5. LAN Disable Circuitry

Note: The 100 Ω resistors for the Test Mode signals are required for the Exclusive OR (XOR) Tree and Isolate Mode.

3.2.2 Serial EEPROM for 82562EZ(EX) Implementations

Serial EEPROM for LAN implementations based on 82562EZ(EX) devices connects to the ICH5. Depending upon the size of the EEPROM, the 82562EZ(EX) may or may not support legacy manageability. Table 7 and Table 8 list the EEPROM map for the 82562EZ(EX) PLC device. For details on the EEPROM, refer to the appropriate *I/O Control Hub 2, 3, 4, 5, 6, and 7 EEPROM Map and Programming Information*.

Table 7. 82562EZ(EX) Memory Layout (128 Byte EEPROM)

00h **3Fh**	HW/SW Reserved Area

NOTE: No manageability provided.

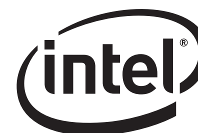


Table 8. 82562EZ(EX) Memory Layout (512 Byte EEPROM)

Address	Contents
00h 3Fh	HW/SW Reserved Area
40h FFh	ASF and Legacy Manageability

NOTE: Legacy manageability only.

3.2.3 Magnetics Modules for 82562EZ(EX) PLC Device

A 5-core magnetics module should be carefully selected for your design. Table 9 lists suggested integrated magnetics modules for use with the 82562EZ(EX) PLC device. These modules also contain integrated USB jacks.

Note: These components are pin-compatible with the magnetics modules listed in Table 13 for the 82547GI(EI) controller.

Table 9. 82562EZ(EX) Recommended Magnetics Modules

Manufacturer	Manufacturer's Part Number
Pulse	JW0A1P01R-E
Stewart	SI-70027
Foxconn	UBC11123-J51

3.2.4 Power Supplies for 82562EZ(EX) PLC Implementations

The 82562EZ(EX) PLC device uses a single 3.3 V power supply. The 3.3 V supply must provide approximately 90 mA current for full speed operation. Standby power must be furnished in order to wake up from powerdown.

3.2.5 82562EZ(EX) Device Test Capability

The device contains an XOR test tree mechanism for simple board tests. Details of the XOR tree operation are contained in the *82562ET LAN on Motherboard Design Guide*.

3.3 Designing with the 82547GI(EI) Gigabit Ethernet Controller

This section provides design guidelines specific to the 82547GI(EI) controller.

3.3.1 82547GI(EI) Ethernet Controller LAN Disable Guidelines

The 82547GI(EI) Controller has a LAN_DISABLE# function that is present on FLSH_SO ball P9. This pin can be connected to a GPIO pin on the ICH5 component to allow the BIOS to disable the Ethernet port (see Figure 6). If the serial FLASH interface is populated, make sure the FLASH serial output pin does not interfere with this function.

For best results, do not attempt to use the LAN_POWER_GOOD signal for a LAN disable input. This pin is intended to operate as a power-on reset connected to a power monitor circuit.

The input of FLSH_SO (ball P9) is the LAN_DISABLE signal. It is sampled on the rising edge of LAN_PWR_GOOD and/or RST#. The signal must be held valid for 80 ns after either rising edge.

If sampled high, the LAN functions normally. If sampled low, then the following occurs:

1. The LAN is disabled.
2. The PHY is powered down.
3. Most MAC clock domains are gated.
4. Most functional blocks are held in reset.
5. The device is in a low power state – equivalent to D3 w/ no wake or manageability.

Note: To use this configuration for the 82562EZ(EX) Platform LAN Connect device, be sure the AND gate U1 is populated. Depopulate the 0 Ω resistor R2.

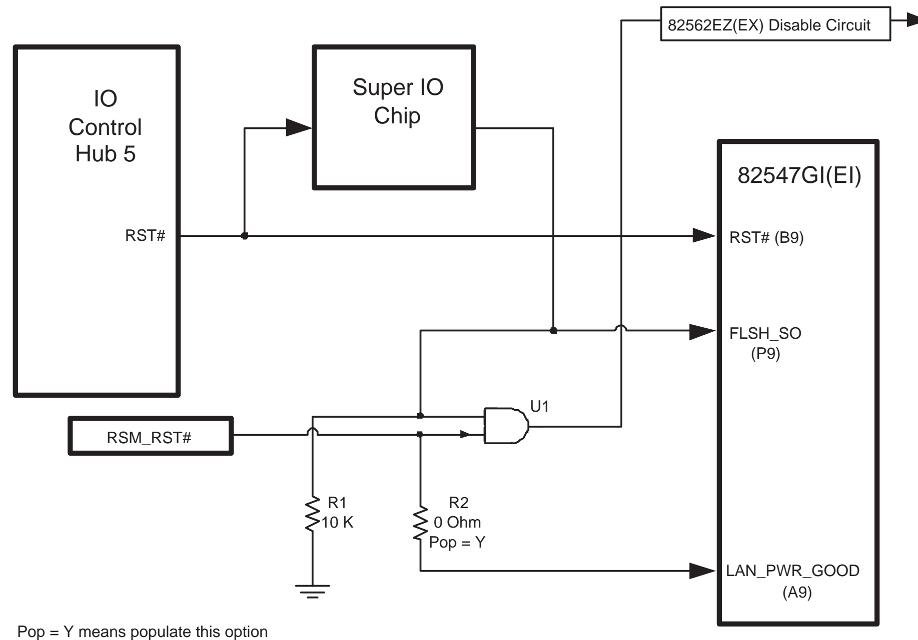
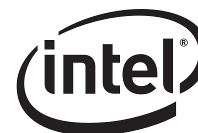


Figure 6. 82547GI(EI) LAN Disable Circuitry

3.3.2 Serial EEPROM for 82547GI(EI) Controller Implementations

The 82547GI(EI) Gigabit Ethernet Controller can use either a Microwire* or an SPI* serial EEPROM. The EEPROM mode is selected on the EEMODE input (ball C4). A pull-up resistor to Vcc denotes SPI*. A pull-down resistor to ground denotes Microwire. Several words of the EEPROM are accessed automatically by the device after reset to provide pre-boot configuration data before it is accessed by host software. The remainder of the EEPROM space is available to software for storing the MAC address, serial numbers, and additional information.



For non-ASF applications, use a 64 register by 16-bit Microwire serial EEPROM. For ASF 1.0 applications, use larger 93C66 Microwire or AT25040 SPI* Serial EEPROM. ASF 2.0 requires an 8K SPI* Serial EEPROM.

Intel has an MS-DOS* software utility called EEUPDATE, which can be used to program EEPROM images in development or production line environments. To obtain a copy of this program, contact your Intel representative.

The EEPROM access algorithm programmed into the 82547GI(EI) controller is compatible with most, but not all, commercially available 3.3 V Microwire interface, serial EEPROM devices, with 64 x 16 (or 256 x 16) organization and a 1 MHz speed rating. The 82547GI(EI)'s EEPROM access algorithm drives extra pulses on the shift clock at the beginnings and ends of read and write cycles. The extra pulses may violate the timing specifications of some EEPROM devices. In selecting a serial EEPROM, choose a device that specifies “don't care” shift clock states between accesses.

Microwire EEPROMs that have been found to work satisfactorily with the 82547GI(EI) Gigabit Ethernet Controller are listed in the following table:

Table 10. Microwire 64 x 16 Serial EEPROMs

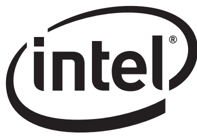
Manufacturer	Manufacturer's Part Number
Atmel	AT93C46
Catalyst	CAT93C46[1]

1. Revision H is not supported. Product die revision letter is marked on top of the package as a suffix to the production data code (e.g., AYWW**H**.)

SPI* EEPROMs that have been found to work satisfactorily with the 82547GI(EI) device are listed in Table 11. SPI EEPROMs must be rated for a clock rate of at least 2 MHz.

Table 11. SPI Serial EEPROMs for 82547GI(EI) Controller

Application	Manufacturer	Manufacturer's Part Number
ASF 1.0 or IPMI Pass Through	Atmel	AT25040
ASF 2.0 or IPMI Advanced Pass Through	Atmel	AT25080



3.3.3 EEPROM Map Information

Table 12 summarizes the EEPROM map for the 82547GI(EI) Gigabit Ethernet Controller.

Table 12. 82547GI(EI) EEPROM Memory Layout

Address	Content
00h **3Fh**	HW/SW Reserved Area
40h **FFh**	ASF and Legacy Manageability
100h **19F**	Manageability Packet Filter Data
1A0 **...** **EEPROM END**	Loadable Manageability Firmware Code

Note: Full manageability provided.

3.3.4 Magnetics Modules for 82547GI(EI) Controller Applications

Carefully select a Gigabit magnetics module for your design. Table 13 lists suggested integrated magnetics modules for use with the 82547GI(EI) device. These modules also contain integrated USB jacks. A good quality Gigabit Ethernet controller can also be used with the 82562EZ(EX) PLC device.

Note: These components are pin-compatible with the magnetics modules shown in Table 9 for the 82562EZ(EX) Platform LAN Connect device.

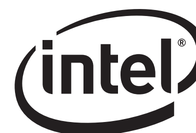
Table 13. 82547GI(EI) Recommended Magnetics Modules

Manufacturer	Manufacturer's Part Number
Pulse	JW0A2P019D
Others	TBD

3.3.5 Power Supplies for the 82547GI(EI) Device

The 82547GI(EI) controller requires three power supplies. The 1.2 V supply must provide approximately 550 mA current. The 1.8 V supply must provide approximately 230 mA current. The 3.3 V supply must provide only 5 mA current.

A central power supply can provide all the required voltage sources, or the power can be derived and regulated locally near the Ethernet control circuitry. Keep in mind that all voltage sources must remain present during powerdown in order to use the 82547GI(EI) Ethernet controller's LAN wake up capability. This consideration makes it more likely that at least some of the voltage sources will be local.



Instead of using external regulators to supply 1.2 V and 1.8 V, the designer can use power transistors in conjunction with on-chip regulation circuitry. See the reference schematic for an implementation example.

The 82547GI(EI) controller has a LAN_PWR_GOOD input. Treat this signal as an external device reset which works in conjunction with the internal power-on reset circuitry. In the situation where a central power supply furnishes all the voltage sources, LAN_PWR_GOOD can possibly be tied to the POWER_GOOD output of the power supply. Designs that generate some of the voltages locally can connect LAN_PWR_GOOD to a power monitor chip. Ensure that the system drives LAN_PWR_GOOD inactive for at least 80 ms after power-up.

The power sources are all expected to ramp up during a brief power-up interval (approximately 20 ms.) with LAN_PWR_GOOD de-asserted. Do not leave the 82547GI(EI) controller in a prolonged state where some, but not all, voltages are applied.

3.3.6 82547GI(EI) Controller Power Supply Filtering

Provide several bypass capacitors for each power rail, selecting values in the range of 0.01µF to 0.01 µF. If possible, orient the capacitors close to the device and adjacent to power pads. Decoupling capacitors should connect to the power planes with short, thick (15 mils - 0.4mm or more) traces and 14 mil (0.35 mm) vias.

Furnish approximately 20 µF of bulk capacitance for each of the main 1.2 V and 1.8 V levels. A convenient way to do this is to use about two 10 µF capacitors, placing them as close to the device power connections as possible.

3.3.7 82547GI(EI) Controller Power Management and Wake Up

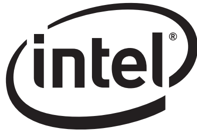
The 82547GI(EI) Gigabit Ethernet Controller supports low power operation as defined in the PCI Bus Power Management Specification. There are two defined power states, D0 and D3. The D0 state provides full power operation and is divided into two sub-states: D0u (uninitialized) and D0a (active). The D3 state provides low power operation and is also divided into two sub-states: D3hot and D3cold.

To enter the low power state, the software driver must stop data transmission and reception. Either the operating system or the driver must program the Power Management Control/Status Register (PMCSR) and the Wakeup Control Register (WUC). If wakeup is desired, the appropriate wakeup LAN address filters must also be set. The initial power management settings are specified by EEPROM bits.

When the 82547GI(EI) controller transitions to either of the D3 low power states, the 1.2 V, 1.8 V, and 3.3 V sources must continue to be supplied to the device. Otherwise, it will not be possible to use a wakeup mechanism. The AUX_POWER signal is a logic input to the 82547GI(EI) controller that denotes auxiliary power is available. If AUX_POWER is asserted, the 82547GI(EI) device will advertise that it supports wake up from a D3cold state.

The 82547GI(EI) device supports both Advanced Power Management (APM) wakeup and Advanced Configuration and Power Interface (ACPI) wakeup. APM wakeup has also been known in the past as “Wake on LAN”.

Wakeup uses the PME# signal to wake the system up. PME# is an active low signal connected to a GPIO port on the ICH5 that goes active in response to receiving a “Magic Packet”, a network wakeup packet, or link status change indication. PME# remains asserted until it is disabled through the Power Management Control/Status Register.

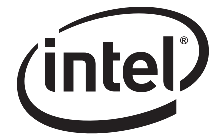


3.3.8 82547GI(EI) Device Test Capability

The 82547GI(EI) Gigabit Ethernet Controller contains a test access port conforming to the IEEE 1149.1a-1994 (JTAG) Boundary Scan specification. To use the test access port, connect these balls to pads accessible by your test equipment. Be sure to connect the TRST# input to ground through a pull-down resistor (approximately 1k value) so that the test capability cannot be invoked by mistake.

A BSDL (Boundary Scan Definition Language) file describing the 82547GI(EI) device is available for use in your test environment.

The controller also contains an XOR test tree mechanism for simple board tests. Details of XOR tree operation may be obtained through your Intel representative.



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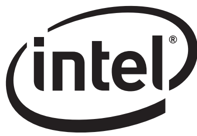


4.0 Ethernet Component Layout Guidelines

These sections provide recommendations for performing printed circuit board layouts. Good layout practices are essential to meet IEEE PHY conformance specifications and EMI regulatory requirements.

4.1 General Layout Considerations for Ethernet Controllers

Critical signal traces should be kept as short as possible to decrease the likelihood of being affected by high frequency noise from other signals, including noise carried on power and ground planes. Keeping the traces as short as possible can also reduce capacitive loading.

Since the transmission line medium extends onto the printed circuit board, special attention must be paid to layout and routing of the differential signal pairs.

Designing for Gigabit operation is very similar to designing for 10 and 100 Mbps. For the 82547GI(EI) Gigabit Ethernet controller, system level tests should be performed at all three speeds.

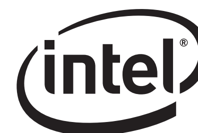
4.1.1 Guidelines for Component Placement

Component placement can affect signal quality, emissions, and component operating temperature. This section provides guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because other interfaces will compete for physical space on a motherboard near the connector. The Ethernet LAN circuits need to be as close as possible to the connector (see Figure 5).



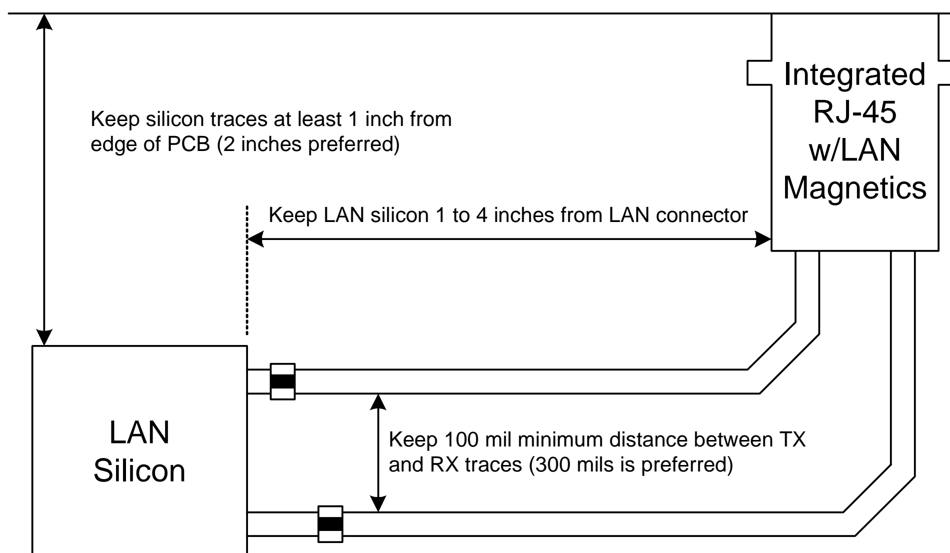


Figure 5. General Placement Distances

Figure 5 shows some basic placement distance guidelines. The figure shows two differential pairs, but can be generalized for a Gigabit system with four analog pairs. The ideal placement for the Ethernet silicon would be approximately one inch behind the magnetics module.

While it is generally a good idea to minimize lengths and distances, this figure also illustrates the need to keep the LAN silicon away from the edge of the board and the magnetics module for best EMI performance.

4.1.2 Crystals

Crystals should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference. Traces should be referenced to a continuous low impedance plane.

Place the crystal and load capacitors on the printed circuit boards as close to the Ethernet component as possible, within 0.75 inch. Keep other potentially noisy traces away from the crystal traces.

4.1.3 Board Stack Up Recommendations

Printed circuit boards for these designs typically have four, six, eight, or more layers. Here is a description of a typical six-layer board stackup:

- Layer 1 is a signal layer. It can contain the differential analog pairs from the Ethernet device to the magnetics module.
- Layer 2 is a signal ground layer. Chassis ground may also be fabricated in Layer 2 under the connector side of the magnetics module.

- Layer 3 is used for power planes.
- Layer 4 is a signal layer. For Gigabit designs, it is common to route two of the differential pairs on this layer.

This board stack up configuration can be adjusted to conform to your company's design rules.

4.1.4 Differential Pair Trace Routing

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Observe the following suggestions to help optimize board performance:

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under four inches. Designs with differential traces longer than 5 inches are much more likely to have degraded receive Bit Error Rate (BER) performance, IEEE PHY conformance failures, and/or excessive Electromagnetic Interference (EMI) radiation
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation within differential pairs to seven mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. See Figure 6.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

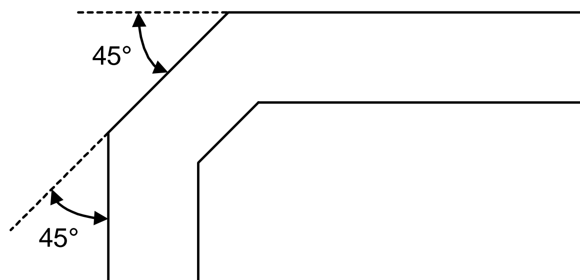
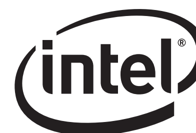


Figure 6. Trace Routing



- The reference plane for the differential pairs should be continuous and low impedance. It is recommended that the reference plane be either ground or 1.8 V (the voltage used by the PHY). This provides an adequate return path for and high frequency noise currents.
- Do not route differential pairs over splits in the associated reference plane.
- Differential termination components should be placed as close as possible to the LAN silicon.

4.1.5 Signal Trace Geometry

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane.

Each pair of signal should have a differential impedance of 100 Ω. +/- 20%. If a particular tool cannot design differential traces, it is permissible to specify 55-65 Ω single-ended traces as long as the spacing between the two traces is minimized. As an example, consider a differential trace pair on Layer 1 that is eight mils (0.2 mm) wide and two mils (0.05 mm) thick, with a spacing of eight mils (0.2mm). If the fiberglass layer is eight mils (0.2 mm) thick with a dielectric constant, E_R, of 4.7, the calculated single-ended impedance would be approximately 61 Ω and the calculated differential impedance would be approximately 100 Ω.

When performing a board layout, do not allow the CAD tool auto-router to route the differential pairs without intervention. In most cases, the differential pairs will have to be routed manually. The components should be laid out in the following order of priority:

1. Differential traces
2. Termination resistors
3. Bypass capacitors
4. Other components

This allows placing those components in the best locations and avoids using critical space by non-critical components.

Note: Measuring trace impedance for layout designs targeting 100 Ω often results in lower actual impedance. Designers should verify actual trace impedance and adjust the layout accordingly. If the actual impedance is consistently low, a target of 105 to 110 Ω should compensate for second order effects.

It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge to edge).

4.1.6 Trace Length and Symmetry

As indicated earlier in Section 4.1.4, the overall length of differential pairs should be less than four inches measured from the Ethernet device to the magnetics.

The differential traces should be equal within 50 mils (1.25 mm) within each pair and as symmetrical as possible. Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. Common mode noise can degrade the receive circuit’s performance and contribute to radiated emissions.

4.1.7 Impedance Discontinuities

Impedance discontinuities cause unwanted signal reflections. Avoid vias (signal through holes) and other transmission line irregularities. If vias must be used, a reasonable budget is two per differential trace. Unused pads and stub traces should also be avoided.

4.1.8 Reducing Circuit Inductance

Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Because signals with fast rise and fall times contain many high frequency harmonics, which can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

4.1.9 Signal Isolation

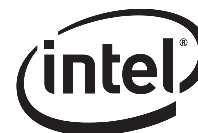
To maintain best signal integrity, keep digital signals far away from the analog traces. A good rule of thumb is no digital signal should be within 300 mils (7.5 mm) of the differential pairs. If digital signals on other board layers cannot be separated by a ground plane, they should be routed at right angles with respect to the differential pairs. If there is another LAN controller on the board, take care to keep the differential pairs from that circuit away.

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

4.1.10 Power and Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.



The following guidelines help reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions. Do not route over a split power or ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- The ground plane beneath the magnetics module should be split. The RJ-45 connector side of the transformer module should have chassis ground beneath it. Split Ground Planes for Magnetics Modules

4.1.11 Traces for Decoupling Capacitors

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance.

4.1.12 Ground Planes Under the Magnetics Module

The magnetics module chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum. Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the magnetics. This arrangement also improves the common mode choke functionality of magnetics module.

Table 7 illustrates the split plane layout for a discrete magnetics module. Capacitors are used to interconnect chassis ground and signal ground.

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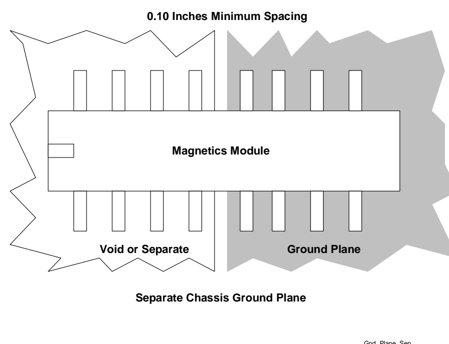


Figure 7. Ground Plane Separation

Figure 8 below shows the preferred method for implementing a ground split under an integrated magnetics module/RJ-45 connector. The capacitor stuffing options (C1 – C6) are used to reduce/ filter high frequency emissions. The value(s) of the capacitor stuffing options may be different for each board. Experiments will need to be performed to determine which value(s) provide best EMI performance.

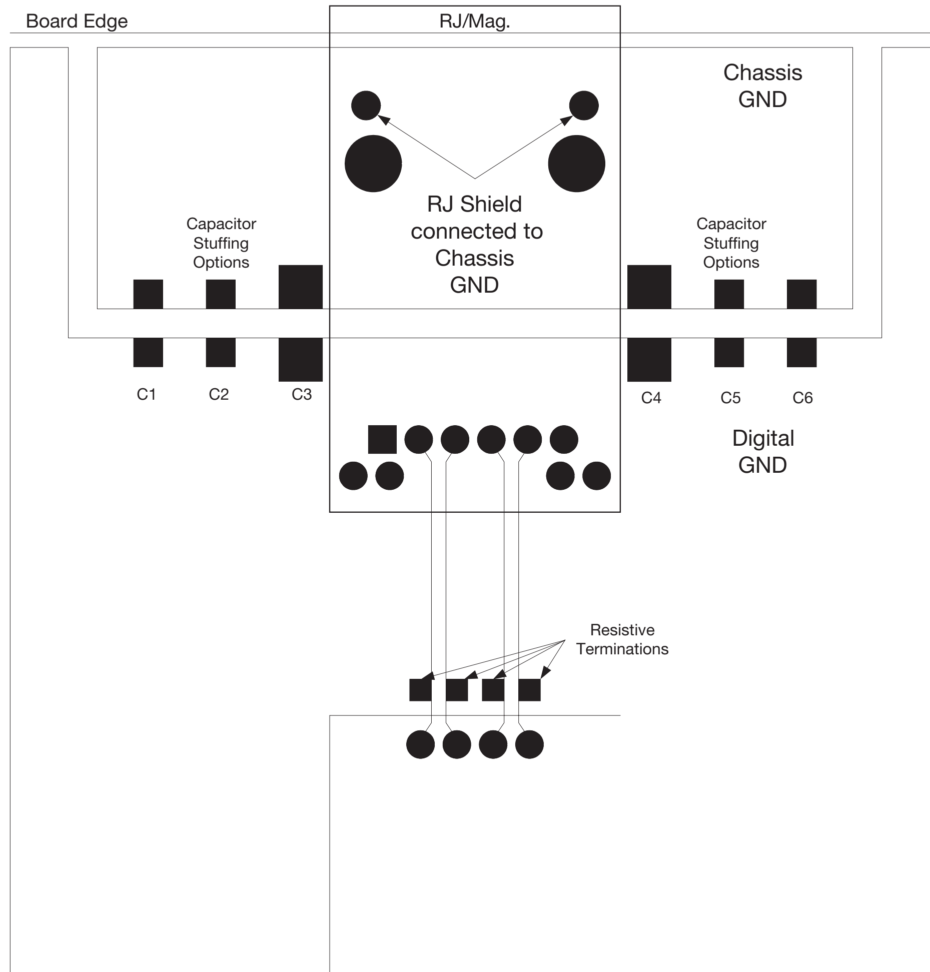


Figure 8. Ideal Ground Split Implementation

The table below gives some starting values for these capacitors.

Capacitors	Value
C3, C4	4.7µF or 10 µF
C1, C2, C5, C6	470 pF to 0.1 µF

The placement of C1 – C6 may also be different for each board design (i.e., not all of the capacitors may need to be populated). Also, the capacitors may not be needed on both sides of the magnetic module.

4.1.13 Special Considerations for Non-Integrated Magnetics Modules and RJ-45 Connectors

It is possible to employ discrete (non-integrated) magnetics modules and RJ-45 connectors. Similar rules will apply to design and layout. The differential pairs should be routed to be as short and symmetrical as possible and the overall lengths of the differential pairs (including the width of the magnetics module) should not exceed approximately four inches.

Additional design and layout steps will be required to add a dedicated board termination plane parallel to chassis ground, 75 Ω termination resistors, and a 1500 pF capacitor. This "Bob Smith" termination scheme is normally contained inside an integrated magnetics module.

In Ethernet designs, it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. In the "Bob Smith" termination method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs from the unused pairs of the RJ-45 connector. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termination plane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

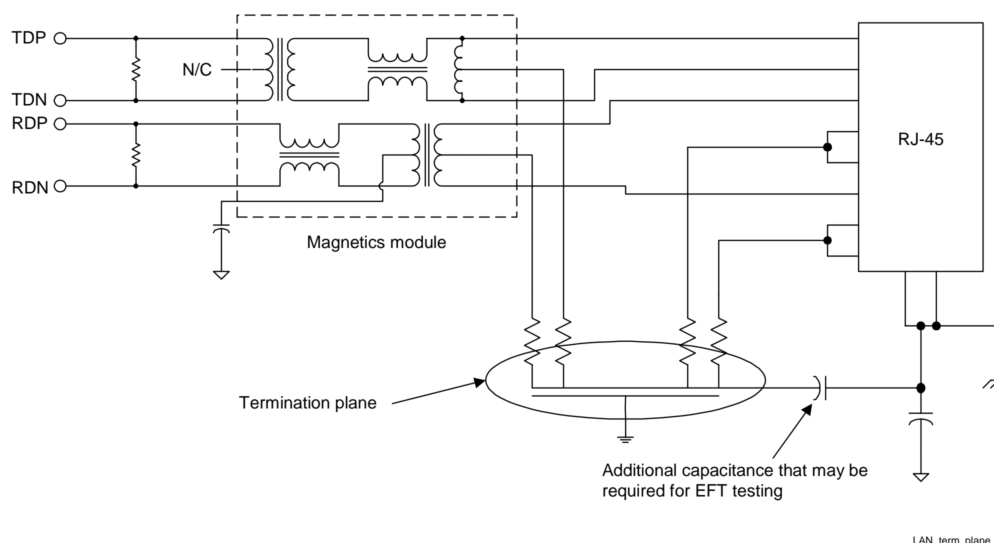


Figure 9. Termination Plane Example for 82562EZ(EX) PLC Device and Discrete Magnetics

4.2 Layout for the 82562EZ(EX) Platform LAN Connect Device

This section provides layout guidelines specific to the 82562EZ(EX) PLC device.

4.2.1 Termination Resistors for Designs Based on 82562EZ(EX) PLC Device

Two differential pairs are terminated using 54.9 Ω (1% tolerance) resistors, placed near the LAN controller. One resistor connects to the MDI+ (MDI positive) signal trace and another resistor connects to the MDI- (MDI negative) signal trace (see Figure 10).

Termination resistor values were recently increased from 49.9 Ω to 54.9 Ω to improve return loss. However, on some designs, this change caused the PCB's output amplitude to be slightly above the peak-to-peak center of the IEEE specification. As a result, RBIAS resistor values were increased (RBIAS10 549 to 619 Ω and RBIAS100 619 to 649 Ω) to reduce the PCB's output amplitude to better meet the IEEE peak-to-peak center specification.

For 100Base-TX designs, the IEEE specification allows a -950 mVpk to -1050 mVpk for the negative peak and +950 mVpk to +1050 mVpk for the positive peak. Ideally, a typical PCB output amplitude should be within -975 mVpk to -1025 mVpk for the negative peak and +975 mVpk to +1025 mVpk for the positive peak.

For 10Base-T designs, the IEEE specification allows a -2.2 mVpk to -2.8 mVpk for the negative peak and +2.2 mVpk to +2.8 mVpk for the positive peak. Ideally, a typical PCB output amplitude should be within -2.35 mVpk to -2.55 mVpk for the negative peak and +2.35 mVpk to +2.55 mVpk for the positive peak.

The RBIAS values previously listed should be considered starting values. Intel recommends that board designers measure each of their PCB's output amplitude and then adjust the RBIAS values as required.

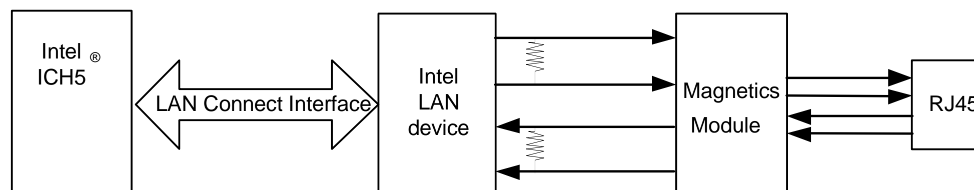
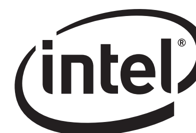


Figure 10. 82562EZ(EX) PLC Device Differential Signal Termination

4.2.2 Light Emitting Diodes for Designs Based on 82562EZ(EX) PLC Device

The 82562EZ(EX) PLC device has three high-current outputs to directly drive LEDs for link, activity and speed indication. Since LEDs are likely to be integral to a magnetics module, take care to route the LED traces away from potential sources of EMI noise. In some cases, it may be desirable to attach filter capacitors.



4.3 Layout for the 82547GI(EI) Gigabit Ethernet Controller

4.3.1 Termination Resistors for Designs Based on 82547GI(EI) Gigabit Ethernet Controller

The four differential pairs are terminated with 49.9 Ω (1% tolerance) resistors, placed near the 82547GI(EI) controller. One resistor connects to the MDI+ signal trace and another resistor connects to the MDI- signal trace. The opposite ends of the resistors connect together and to ground through a single 0.1 µF capacitor. The capacitor should be placed as close as possible to the 49.9 Ω resistors, using a wide trace.

Do not vary the suggested component values. Be sure to lay out symmetrical pads and traces for these components such that the length and symmetry of the differential pairs are not disturbed.

4.3.2 Light Emitting Diodes for Designs Based on 82547GI(EI) Controller

The 82547GI(EI) controller provides four programmable high-current outputs to directly drive LEDs for link activity and speed indication. Since the LEDs are likely to be integral to a magnetics module, take care with care to route the LED traces away from potential sources of EMI noise. In some cases, it may be desirable to attach filter capacitors.

4.4 Physical Layer Conformance Testing

Physical layer conformance testing (also known as IEEE testing) is a fundamental capability for all companies with Ethernet LAN products. PHY testing is the final determination that a layout has been performed successfully. If your company does not have the resources and equipment to perform these tests, consider contracting the tests to an outside facility.

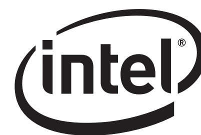
Crucial tests are as follows, listed in priority order:

- Bit Error Rate (BER). Good indicator of real world network performance. Perform bit error rate testing with long and short cables and many link partners. The test limit is 10-11 errors.
- Output Amplitude, Rise and Fall Time (10/100 Mbps), Symmetry and Droop (1000 Mbps). For the 82547GI(EI) controller, use the appropriate PHY test waveform.
- Return Loss. Indicator of proper impedance matching, measured through the RJ-45 connector back toward the magnetics module.
- Jitter Test (10/100 Mbps) or Unfiltered Jitter Test (1000 Mbps). Indicator of clock recovery ability (master and slave for Gigabit controller).

4.5 Troubleshooting Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. Asymmetry can create common-mode noise and distort the waveforms. For each component and/or via that one trace encounters, the other trace should encounter the same component or a via at the same distance from the Ethernet silicon.
3. Excessive distance between the Ethernet silicon and the magnetics. Long traces on FR4 fiberglass epoxy substrate will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer than the four inch rule.
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive EMI emissions and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
5. Routing one pair of differential traces too close to another pair of differential traces. After exiting the Ethernet silicon, the trace pairs should be kept 0.3 inches or more away from the other trace pairs. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45 connector, and the Ethernet silicon.
6. Use of a low quality magnetics module.
7. Re-use of an out-of-date physical layer schematic in a Ethernet silicon design. The terminations and decoupling can be different from one PHY to another.
8. Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling can lower the effective differential impedance by 5 Ω to 20 Ω. Short traces will have fewer problems if the differential impedance is slightly off target.
9. For 82562EZ(EX) PLC designs, use of capacitor that is too large between the transmit traces and/or too much capacitance on the magnetic module's transmit center tap to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. If a capacitor is used, it should almost certainly be less than 22 pF.



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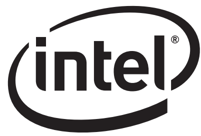
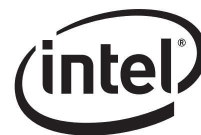


5.0 Design and Layout Checklists

The Design and Layout checklists are in Portable Data Format (PDF) and available to aid designers via:

http://developer.intel.com.



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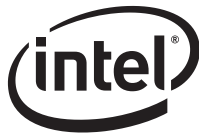


6.0 Ball Number to Signal Mapping with Population Options

Table 14 lists the ball names for both devices corresponding to the shared ball number. Please note that signal names may vary slightly from the names on the reference schematic in Section 7.0. The schematic names follow conventions used by Intel design engineers on their design tools.

Table 14. Ball Number to Signal Mapping (Sheet 1 of 7)

Ball Ref	82562EZ(EX) Pin Name	82547GI(EI) Pin Name	Signal Name Difference?	82562EZ(EX) Connection?	Pop Option Required?	Comment
A1	NC	NC				
A2	NC	NC	X			
A3	3.3 V	3.3 V		X		
A4	NC	NC	X			
A5	NC	NC	X			
A6	NC	PME#	X			
A7	3.3 V	3.3 V		X		
A8	NC	NC	X			
A9	NC	LAN_PWR_GOOD	X			
A10	NC	SMBCLK	X			
A11	VCCT	3.3 V		X		
A12	LILED#	LED0/LINK_UP#	X	X	X	Same signal different name
A13	TESTEN	TEST	X	X	X	Same signal different name
A14	NC	NC				
B1	NC	NC	X			
B2	NC	NC	X			
B3	VSS	VSS		X		
B4	NC	NC	X			
B5	NC	NC	X			
B6	NC	NC	X			
B7	VSS	VSS		X		
B8	NC	NC	X			
B9	NC	RST#	X			
B10	NC	SMB_ALERT#	X			

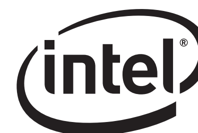


Table 14. Ball Number to Signal Mapping (Sheet 2 of 7) (Continued)

Ball Ref	82562EZ(EX) Pin Name	82547GI(EI) Pin Name	Signal Name Difference?	82562EZ(EX) Connection?	Pop Option Required?	Comment
B11	SPDLED#	LED2/LINK100#	X	X	X	Same signal different name
B12	TOUT	LED3/LINK1000#	X	X	X	82562EZ: NC 82547GI(EI): LED
B13	RBIAS100	CTRL18	X	X	X	82562EZ: 649 ohm external pull-down 82547GI(EI): Voltage Transistor connection
B14	RBIAS10	IEEE_TEST+	X	X	X	82562EZ: 619 ohm external pull-down 82547GI(EI): IEEE PHY Test
C1	NC	NC	X			
C2	NC	NC	X			
C3	NC	NC	X			
C4	NC	EEMODE	X			
C5	NC	NC	X			
C6	NC	NC	X			
C7	NC	NC	X			
C8	NC	NC	X			
C9	NC	SMBDATA	X			
C10	VSS	VSS		X		
C11	ACTLED#	LED/ACTIVITY#	X	X	X	Same signal different name
C12	VSS	ANALOG_VSS		X		
C13	TDP	MDI[0]+	X	X	X	Connected to magnetics.
C14	TDN	MDI[0]-	X	X	X	Connected to magnetics.
D1	NC	NC	X			
D2	NC	NC	X			
D3	NC	NC	X			
D4	VSS	VSS	X	X	X	Connected to VSS
D5	VSS	VSS		X		
D6	VSS	VSS	X	X	X	Connected to VSS
D7	VSS	VSS		X		
D8	VSS	VSS		X		
D9	NC	NC	X			

Table 14. Ball Number to Signal Mapping (Sheet 3 of 7) (Continued)

Ball Ref	82562EZ(EX) Pin Name	82547GI(EI) Pin Name	Signal Name Difference?	82562EZ(EX) Connection?	Pop Option Required?	Comment
D10	ISOL_EXEC	NC	X	X	X	82562EZ: No Connect. Internal Pull-Down. 82547GI(EI): No Connect.
D11	NC	1.8 V	X			
D12	ISOL_TI	1.8 V	X	X	X	82562EZ: No Connect. Internal Pull-Down. 82547GI(EI): 1.8 V.
D13	VSSA	ANALOG_VSS		X		
D14	ISOL_TCK	IEEE_TEST-	X	X	X	82562EZ: No Connect. Internal Pull-Down. 82547GI(EI): IEEE PHY Test.
E1	VCC	3.3 V		X		
E2	VSS	VSS		X		
E3	NC	NC	X			
E4	VSS	VSS	X	X	X	Connected to VSS
E5	VSS	VSS		X		
E6	VSS	VSS		X		
E7	VSS	VSS		X		
E8	VSS	VSS		X		
E9	VSS	VSS		X		
E10	VSS	VSS	X	X	X	Connected to VSS
E11	VCCT	ANALOG_1.2V	X	X	X	3.3 V / 1.2 V Plane
E12	VCCT	ANALOG_1.2V	X	X	X	3.3 V / 1.2 V Plane
E13	RDP	MDI[1]+	X	X	X	Connected to magnetics.
E14	RDN	MDI[1]-	X	X	X	Connected to magnetics.
F1	NC	NC	X			
F2	NC	NC	X			
F3	NC	NC	X			
F4	VSS	VSS		X		
F5	VSS	VSS	X	X	X	Connected to VSS
F6	VSS	VSS		X		
F7	VSS	VSS		X		
F8	VSS	VSS		X		
F9	VSS	VSS		X		
F10	VSS	VSS		X		

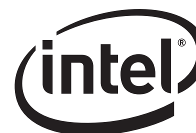


Table 14. Ball Number to Signal Mapping (Sheet 4 of 7) (Continued)

Ball Ref	82562EZ(EX) Pin Name	82547GI(EI) Pin Name	Signal Name Difference?	82562EZ(EX) Connection?	Pop Option Required?	Comment
F11	VSS	VSS		X		
F12	NC	NC	X			
F13	NC	MDI[2]+	X			
F14	NC	MDI[2]-	X			
G1	NC	CI_CLK	X			
G2	NC	CI[9]	X			
G3	NC	NC	X			
G4	NC	CSA_1.2V	X			
G5	VCCR	1.2 V	X	X	X	3.3 V / 1.2 V Plane
G6	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
G7	VSS	VSS		X		
G8	VSS	VSS		X		
G9	VSS	VSS		X		
G10	VSS	VSS		X		
G11	VSS	VSS		X		
G12	NC	1.8 V	X			
G13	VCC	ANALOG_1.2V	X	X	X	3.3 V / 1.2 V Plane
G14	VSS	ANALOG_VSS		X		
H1	NC	CI[10]	X			
H2	NC	CSA_VSS	X			
H3	NC	CI[8]	X			
H4	NC	CSA_1.2V	X			
H5	VCCR	1.2 V	X	X	X	3.3 V / 1.2 V Plane
H6	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
H7	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
H8	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
H9	VSS	VSS		X		
H10	VSS	VSS		X		
H11	3.3 V	ANALOG_1.2V	X	X	X	3.3 V / 1.2 V Plane
H12	NC	NC	X			
H13	NC	MDI[3]+	X			
H14	NC	MDI[3]-	X			
J1	NC	CI[0]	X			

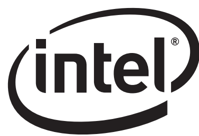


Table 14. Ball Number to Signal Mapping (Sheet 5 of 7) (Continued)

Ball Ref	82562EZ(EX) Pin Name	82547GI(EI) Pin Name	Signal Name Difference?	82562EZ(EX) Connection?	Pop Option Required?	Comment
J2	NC	CI[1]	X			
J3	NC	CI[2]	X			
J4	NC	CSA_1.2V	X			
J5	VCCR	1.2 V	X	X	X	3.3 V / 1.2 V Plane
J6	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
J7	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
J8	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
J9	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
J10	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
J11	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
J12	NC	AUX_PWR	X			
J13	NC	1.8 V	X			
J14	X2	XTAL2		X		
K1	NC	CI[3]	X			
K2	VSS	CSA_VSS		X		
K3	VCC	3.3 V		X		
K4	VCC	3.3 V	X	X	X	Connected to 3.3 V
K5	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
K6	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
K7	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
K8	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
K9	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
K10	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
K11	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
K12	VSS	ANALOG_VSS		X		
K13	VCC	3.3 V		X		
K14	X1	XTAL1		X		
L1	NC	CI_STRS	X			
L2	NC	CI_STRF	X			
L3	NC	CI[4]	X			
L4	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
L5	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
L6	VSS	VSS	X	X	X	Connected to VSS

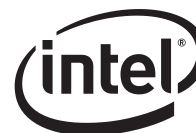


Table 14. Ball Number to Signal Mapping (Sheet 6 of 7) (Continued)

Ball Ref	82562EZ(EX) Pin Name	82547GI(EI) Pin Name	Signal Name Difference?	82562EZ(EX) Connection?	Pop Option Required?	Comment
L7	ADV10	NC	X	X	X	82562EZ: No Connect. Internal Pull-Down. 82547GI(EI): No Connect.
L8	NC	NC	X			
L9	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
L10	VCC	1.2 V	X	X	X	3.3 V / 1.2 V Plane
L11	VSS	VSS		X		
L12	NC	JTAG_TMS	X			
L13	JTXD[1]	JTAG_TRST#	X	X	X	82562EZ: ICH LAN Connect. 82547GI(EI): JTAG Connect.
L14	JTXD[2]	JTAG_TCK	X	X	X	82562EZ: ICH LAN Connect. 82547GI(EI): JTAG Connect.
M1	NC	CI[6]	X			
M2	NC	CI[5]	X			
M3	NC	CSA_VSS	X			
M4	NC	CSA_1.2V	X			
M5	NC	1.2 V	X			
M6	VSS	VSS		X		
M7	NC	NC	X			
M8	NC	NC	X			
M9	NC	FLSH_CE#	X			
M10	NC	EESK	X			
M11	NC	FLSH_SI	X			
M12	JRXD[2]	SDP[3]	X	X	X	82562EZ: ICH LAN Connect. 82547GI(EI): No Connect.
M13	JRSTSYNC	JTAG_TDI	X	X	X	82562EZ: ICH LAN Connect. 82547GI(EI): JTAG Connect.
M14	JTXD[0]	JTAG_TDO	X	X	X	82562EZ: ICH LAN Connect. 82547GI(EI): JTAG Connect.
N1	VSS	CSA_VSS		X		

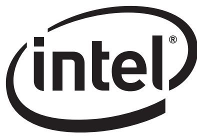
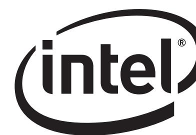


Table 14. Ball Number to Signal Mapping (Sheet 7 of 7) (Continued)

Ball Ref	82562EZ(EX) Pin Name	82547GI(EI) Pin Name	Signal Name Difference?	82562EZ(EX) Connection?	Pop Option Required?	Comment
N2	NC	CI[7]	X			
N3	NC	CI_RCOMP	X			
N4	NC	CI_VREF	X			
N5	NC	1.2 V	X			
N6	VCC	3.3 V		X		
N7	NC	NC	X			
N8	VCC	3.3 V		X		
N9	NC	FLSH_SCK	X			
N10	NC	EEDO	X			
N11	NC	NC	X			
N12	VSSP	VSS		X		
N13	JRXD[1]	SDP[2]	X	X	X	82562EZ: ICH LAN Connect. 82547GI(EI): No Connect.
N14	JCLK	SDP[0]	X	X	X	82562EZ: ICH LAN Connect. 82547GI(EI): No Connect.
P1	NC	NC				
P2	VCC	3.3 V		X		
P3	NC	CI_SWING	X			
P4	NC	NC	X			
P5	NC	NC	X			
P6	NC	NC	X			
P7	NC	EECS	X			
P8	VSS	VSS		X		
P9	NC	FLSH_SO/ LAN_DISABLE#	X			
P10	NC	EEDI	X			
P11	NC	CTRL12	X			
P12	3.3 V	3.3 V		X		
P13	JRXD[0]	SDP[1]	X	X	X	82562EZ: ICH LAN Connect. 82547GI(EI): No Connect.
P14	NC	NC				



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7.0 Dual Footprint Reference Schematic

The following pages illustrate a dual purpose 10/100 and 10/100/1000 design using the 82562EZ(EX) Platform LAN Connect device and the 82547GI(EI) Gigabit Ethernet Controller.

82562EZ/EX - 82547GI/EI REFERENCE DESIGN

Rev. 2.6
6/23/06

PAGE INDEX

1 - Title Page
2 - 82547GI/EI HI1.5, SMBus, Ethernet, Flash, EEprom & JTAG Interfaces.
82562EZ/EX Ethernet, EEprom and LAN Connect Interfaces.
3 - 82547GI/EI - 82562EZ/EX Power, VRef, Test Mode and Reserved pins.
4 - LAN AFE (MagJack RJ-45 Connector)
5 - Linear Regulators and by-pass caps.
6. - Alternate LAN AFE (MJ3 Connector)

A *Install this component only when using the 82547GI/EI Controller*

B *Install this component only when using the 82562EZ/EX Controller*

REVISIONS		
REV	DESCRIPTION	DATE

PBA NO.	
APPROVALS	DATE
DRAWN	
CHECKED	
ENGR APVD	
APVD	
APVD	

Intel® 2111 N. E. 25th Avenue Hillsboro, OR 97124-5961

TITLE 82562EZ/EX - 82547GI/EI Ref. Design

SIZE C DWG. NO. REV 01

SCALE DATE 12/21/2004 SHEET 01

82562EZ/EX - 82547GI/EI

10/100/1000 Mbps Ethernet Controller with Communications Streaming Architecture (CSA)

15mm x 15mm BGA
1mm Pitch

Pin Name Decode = 82562EZ/EX Signal Name - 82547GI/EI Signal Name

1 of 2

Populate only one EEprom device: Microwire for non-management or SPI for ASF2.0 support.

Do not populate EEprom when using the 82562EZ/EX. Use EEprom associated with the ICH device.

Microwire EEPROM

SPI EEPROM

Install R93 if using Microwire protocol EEPROM devices. Install R57 if using SPI EEPROM devices.

Route to ICH5 GPIO8 Signal

Route to JTAG Logic

Route LAN Connect Interface to ICH5 controller.

Route CSA Interface to MCH Controller

Pin B10 is a multi-function pin: Open drain SMB Alert in SMB mode. PCI_PWR_GOOD signal in ASF mode.

Ensure that the SMBDATA and SMBCLK traces are pulled to logic high with weak pullup resistors somewhere on the NIC or planar.

RSM_RST# should not be asserted until 50 ms after the LAN power rails are stable.

A Install this component only when using the 82547GI/EI Controller

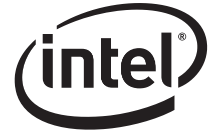
B Install this component only when using the 82562EZ/EX Controller

D/T Install only for special debug or testing purposes

Intel® 2111 N. E. 25th Avenue Hillsboro, OR 97124-5961

TITLE: 82562EZ/EX - 82547GI/EI Ref. Design

SIZE C | DATE 12/21/2004 | SHEET 02



82562EZ/EX - 82547GI/EI

10/100/1000 Mbps Ethernet Controller with Communications Streaming Architecture (CSA)

15mm x 15mm BGA

1mm Pitch

Pin Name Decode =

82562EZ/EX Signal Name - 82547GI/EI Signal Name

2 of 2

A Install this component only when using the 82547GI/EI Controller

B Install this component only when using the 82562EZ/EX Controller

D/T Install only for special debug or testing purposes

Place this capacitor close to it's respective pin of the 82547GI(EI).

Place these capacitors close to their respective pins of the 82547GI(EI).

Place these capacitors close to the divider network.

Internal PHY clock test point. IEEE conformance testing.

Intel, 2111 N. E. 25th Avenue, Hillsboro, OR 97124-5961

TITLE: 82562EZ/EX - 82547GI/EI Ref. Design

SIZE: C | DATE: 12/21/2004 | SHEET: 03

10/100/1000 PHY Interface with Integraded Magnetics & RJ45

REVISIONS

REV	DESCRIPTION	DATE

For the 82562EZ/EX, differential pairs are terminated using 54.9 ohm 1% resistors.

Common-mode filter

LINK/ACTIVITY LED

LINK	GREEN
ACTIVITY	BLINK

10/100/1000 Mbps Compatible Connector

1 GbE version (USB Ports not shown)

Connector also includes 2 USB ports. Pins not shown on this symbol.

COPPER LAN

MDI_0+ / TDP

MDI_0- / TDN

MDI_1+ / RDP

MDI_1- / RDN

MDI_2+

MDI_2-

MDI_3+

MDI_3-

LINK_UP_N

ACTIVITY_N

LINK1000_N

LINK100_N

VCC1.8

3.3V_AUX

BI-COLOR SPEED LED

10 Mbps	OFF
100 Mbps	GREEN
1000 Mbps	YELLOW

These three capacitors across the CHASSIS_GND to GND split, are located above the magnetics module. Place as close as possible to the magnetics module.

These three capacitors across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.

A *Install this component only when using the 82547GI/EI Controller*

B *Install this component only when using the 82562EZ/EX Controller*

D/T *Install only for special debug or testing purposes*

PBA NO.		Intel 2111 N. E. 25th Avenue Hillsboro, OR 97124-5961
APPROVALS	DATE	TITLE 82562EZ/EX - 82547GI/EI Ref. Design
DRAWN		
CHECKED		
ENGR APVD		SIZE C DWG. NO. REV
APVD		
APVD		SCALE DATE12/21/2004 SHEET 04

REVISIONS

REV	DESCRIPTION	DATE

VCC3_3 Supply Note:

If Alerting is supported, VCC3_3 is sourced from either PCI_AUX_3.3v or the planar 3.3v_STBY. Otherwise VCC3_3 can be sourced from a non-standby 3.3v power rail.

Bypass Caps for 1.2V COREVDD
Place Close To LAN silicon

VCC1_2 C70 0.01uF C25 0.1uF C28 0.1uF

VCC1_8 VCC1_2 C69 0.01uF D/T C67 0.01uF

VCC1_8 C72 0.01uF C71 0.01uF

VCC3_3 C34 0.1uF C16 0.1uF C66 0.01uF C65 0.01uF

Linear Regulators:
Stuff only for 82547GI(EI)

VCC3_3 C59 4.7uF C32 0.1uF CTRL1_8 Q1 ABCP69T1 VCC1_8 C48 10uF C45 10uF D/T

VCC3_3 R99 1.33 5W 1% C58 4.7uF C15 0.1uF CTRL1_2 Q2 ABCP69T1 VCC1_2 C46 10uF C44 10uF D/T

This LAN_DISABLE circuit is
for the 82562EZ(EX) only.

3.3V_AUX 470 PMBT3904 1K 100 LDSBL_D12 LDSBL_D14 LDSBL_D10 LDSBL_A13 SUPER_IO_GP_DISABLE LAN_RST#

VCC3_3 1K B SUPER_IO_GP_DISABLE 1K A RSM_RST#

Choose Super IO pin that defaults to input on power up and is powered from the Resume (AUX) well

RSM_RST# should not be asserted until 50 ms after the LAN power rails are stable.

Note: For the 82562EZ(EX) the BIOS must delay driving LAN_RST# for 20ms after resetting the ICH. Use the AND gate shown if this timing is not already accounted for in your design.

A — *Install this component only when using the 82547GI/EI Controller*

B — *Install this component only when using the 82562EZ/EX Controller*

D/T — *Install only for special debug or testing purposes*

PBA NO.		Intel 2111 N. E. 25th Avenue, Hillsboro, OR 97124-5961
APPROVALS	DATE	TITLE: 82562EZ/EX - 82547GI/EI Ref. Design
DRAWN		
CHECKED		
ENGR APVD		SIZE C · DWG. NO. · REV
APVD		
APVD		SCALE · DATE 12/21/2004 · SHEET 05

Alternate AFE Using MJ3

Note: For the 82547/GI/EI, differential pairs are terminated using 49.9 ohm 1% resistors.

Common-mode filter

C9 0.1uF, C10 0.1uF, C11 0.1uF, C12 0.1uF

R73 54.9 1%, R69 54.9 1%, R75 54.9 1%, R70 54.9 1%

R79 54.9 1%, R71 54.9 1%, R72 54.9 1%, R77 54.9 1%

Place these components close to the LAN Controller

MDI_0+ / TDP
MDI_0- / TDN
MDI_1+ / RDP
MDI_1- / RDN
MDI_2+
MDI_2-
MDI_3+
MDI_3-

LINK_UP_LED_N
ACTIVITY_LED_N
LINK_1000_N
LINK_100_N
LNK1K_PU_ALT

VCC3_3
R90 0
R89 0

ACTIVITY LED
Green = LINK UP
BLINKING = TX/RX ACTIVITY

VCC1_8
C29 0.1uF
JA2

Center taps of connector magnetics must be connected to VCC 1.8v power rail when using the 82547GI(EI) controller.

10/100/1000 Mbps Compatible Connector
1Gig version (USB Ports not shown)
(For 10/100 designs do not use a MAGJACK that has center tap capacitors)

Connector also includes 2 USB ports. Pins not shown on this symbol.

LED1 GREEN
LED2 BI-COLOR
GRN
YEL
250 ohm

19 LED1C
20 LED1A
10 TD0+
11 TD0-
12 TD1+
13 TD1-
14 TD2+
15 TD2-
16 TD3+
17 TD3-
22 LED2A
21 LED2B
9 VCC_CT
18 GND
MJ3_Gbe

RJ45-1
RJ45-2
RJ45-3
RJ45-6
RJ45-4
RJ45-5
RJ45-7
RJ45-8

RTermination
75 ohms each
150 pf, 2kv
LGND1 23, LGND2 26, LGND3 27, LGND4 30

COPPER LAN

Off = Link 10 Mbps
Green = Link 100 Mbps
Orange = Link 1000 Mbps

CGND
C43 10uF
C36 0.001uF
C35 0.001uF

A — Install this component only when using the 82547GI/EI Controller

B — Install this component only when using the 82562EZ/EX Controller

D/T — Install only for special debug or testing purposes

REVISIONS		
REV	DESCRIPTION	DATE

PBA NO.

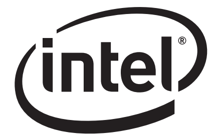
APPROVALS	DATE
DRAWN	
CHECKED	
ENGR APVD	
APVD	
APVD	

Intel 2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961

TITLE **82562EZ/EX - 82547GI/EI Ref. Design**

SIZE C | DWG. NO. | REV

SCALE | DATE12/21/2004 | SHEET 06



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Appendix A Measuring LAN Reference Frequency Using a Frequency Counter

A.1 Background

To comply with IEEE specifications for 10/100 Mbps and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be correct and accurate within ±50 parts per million (ppm).

Note: Intel recommends a frequency tolerance of ±30 (ppm).

Most Intel LAN devices will operate properly with a 25.000 MHz reference crystal, provided it meets the recommended requirements for frequency stability, equivalent series resistance at resonance (ESR), and load capacitance.

Most circuits for series resonant crystals include two discrete capacitors (typically C1 and C2), with values between 5 pF and 36 pF.

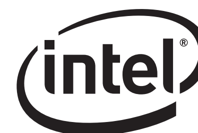
The most accurate way to determine the appropriate value for the discrete capacitors is to install the approximately correct values for C1 and C2. Next, a frequency counter should be used to measure the transmitter reference frequency (or transmitter reference clock).

- If the transmitter reference frequency is more than 20 ppm below the target frequency, then the values for C1 and C2 are too big and should be decreased.
- If the transmitter reference frequency is more than 20 ppm above the target frequency, then the values for C1 and C2 are too small and should be increased.

This Appendix provides instructions and illustrations that explain how to use a frequency counter and probe to determine the Ethernet LAN device transmit center frequency. An example describing how to calculate the frequency accuracy of the measured and averaged center frequency with respect to the target center frequency is also included.

A.2 Required Test Equipment

- Tektronix CMC-251, or similar high resolution, digital counter
- Tektronix P6246, or similar high bandwidth, low capacitance (less than 1 pF) probe
- Tektronix 1103, or similar probe power supply or probe amplifier
- BNC, 50-ohm coaxial cable (less than 6 feet long)
- System with power supply and test software for the LAN circuit to be tested



A.3 Indirect Probing Method

The indirect probing test method is applicable foremost devices that support 100BASE-T. Since probe capacitance can load the reference crystal and affect the measured frequency, the preferred method is to use the indirect probing test method when possible.

Almost all Intel LAN silicon that support 1000BASE-T Ethernet can provide a buffered 125 MHz clock, which can be used for indirect probing of the transmitter reference clock. The buffered 125 MHz clock will be a 5X multiple of the crystal circuit's reference frequency (Figure 11).

Different LAN devices may require different register settings, to enable the buffered 125 MHz reference frequency. Please obtain the settings or instructions that are appropriate for the LAN controller you are using.

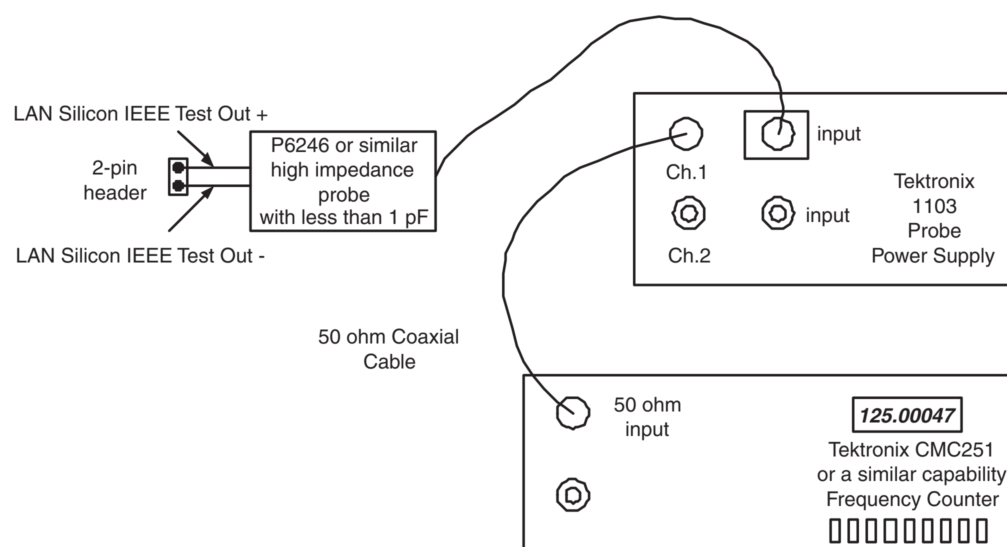
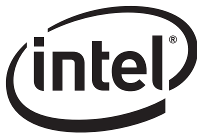


Figure 11. Indirect Probing Setup



A.4 Indirect Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN controller enabled.
2. Connect the test equipment as shown in Figure 11.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~125.0000 MHz with at least four decimal places frequency resolution.
4. Enable the 125 MHz buffered reference clock. An example can be found in Appendix B, “GigConf.exe Register Settings for 82547GI(EI) Devices”.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 125.0000 MHz reference frequency.

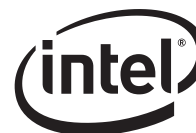
$$FrequencyAccuracy(ppm) = \frac{(x - y)}{(y / 1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 1.

Given: The measured averaged center frequency is 124.99942 MHz (or 124,999,420 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(124999420 - 125000000)}{(125000000 / 1000000)} = -4.64ppm$$



Example 2.

Given: The measured averaged center frequency is 125.00087 MHz (or 125,000,870 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(125000870 - 125000000)}{(125000000 / 1000000)} = 6.96ppm$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.

A.5 Direct Probing Test Method, Applicable for Most 10/100 Devices (Devices that do NOT support 1000Base-T)

Because probe capacitance can load the reference crystal affecting the measured frequency, it is preferable to use a probe with less than 1 pF capacitance.

Note: Direct probing is not recommended for the 82547GI(EI) LAN silicon.

The probe should be connected between the X2 (or Xout) pin of the LAN device and a nearby ground. Typically, it is possible to connect the probe pins across one of the discrete load capacitors (C2 in Figure 12).

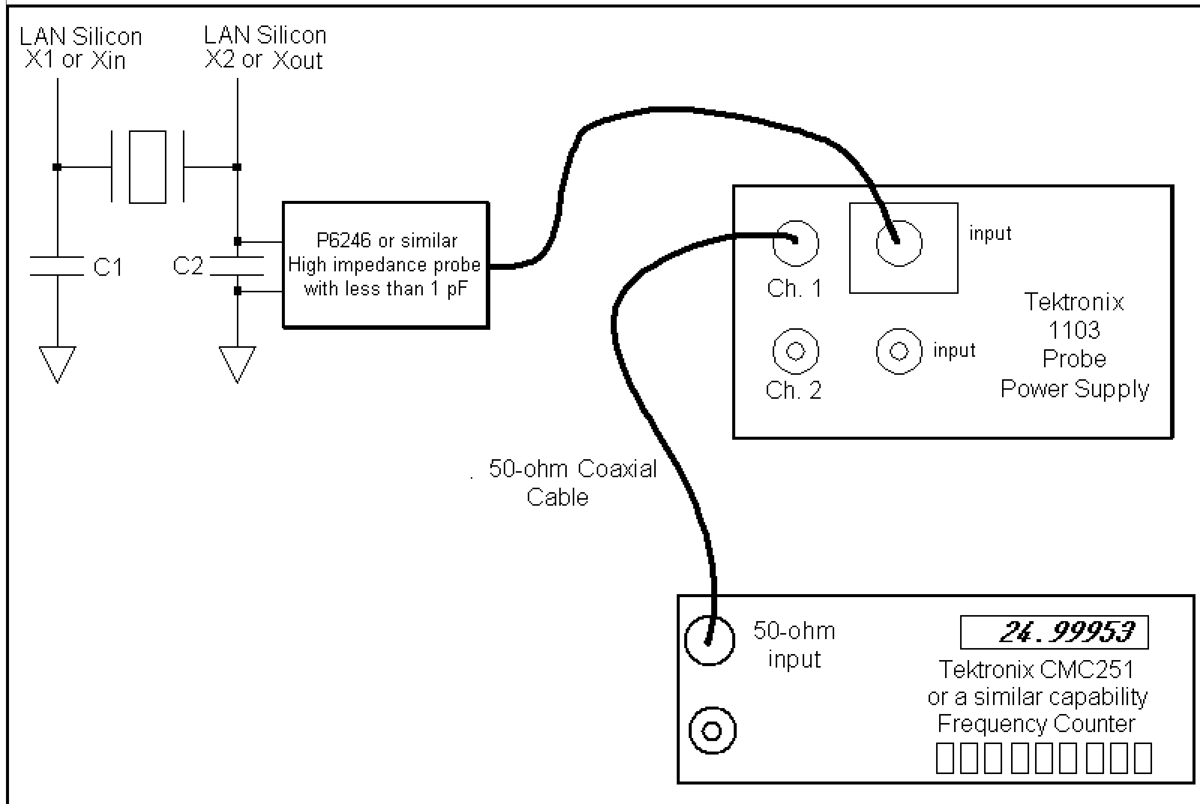
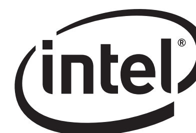


Figure 12. Direct Probing Method

A.6 Direct Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN controller enabled.
2. Connect the test equipment as shown in Figure 12.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~25.0000 MHz with at least four decimal places frequency resolution.
4. Ensure the LAN circuits are powered.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 25.0000 MHz reference frequency.



$$FrequencyAccuracy(ppm) = \frac{(x - y)}{(y / 1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 3.

Given: The measured averaged center frequency is 24.99963 MHz (or 24,999,630 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(24999630 - 25000000)}{(25000000 / 1000000)} = -14.8ppm$$

Example 4.

Given: The measured averaged center frequency is 25.00027 MHz (or 25,000,270 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(25000270 - 25000000)}{(25000000 / 1000000)} = 10.8ppm$$

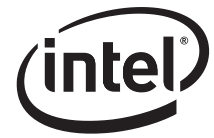
Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.

Appendix B GigConf.exe Register Settings for 82547GI(EI) Devices

The following steps describe the indirect probing test method using GigConf.exe for 82547GI(EI) devices.

1. Boot to DOS using a DOS Boot Diskette.
2. Launch Gigconf from the diskette (gigconf.exe).
3. Select the Intel network connection to be measured.
    a. If multiple adapters are installed, use the arrow keys to navigate to highlight the selected adapter and press Enter.
4. Select Registers by pressing “R”.
5. Select PHY Registers by pressing “P”.
6. Use the arrow keys to navigate to the value listed next to address 0000.
7. Press Enter when the value is highlighted and then use Backspace to clear out the current value.
8. Type “0100” for the value and then press Enter.
9. Navigate to the value listed next to address 0012.
10. Press Enter to select the highlighted value and use Backspace to clear the current value.
11. Type “8000” for the value and then press Enter.
12. Navigate to the Set Address field on the right side of the screen (use the right arrow key)
13. Press Enter to select the highlighted value and then use Backspace to clear out the current value.
14. Type “4011” for the value and then press Enter.
    This changes the PHY register screen and updates it with new addresses and values.
15. Use the arrow keys to navigate to the value for address 4011.
16. Press Enter when the value is highlighted and then use Backspace to clear the current value.
17. Type “8000” for the value and then press Enter.
18. Use the right arrow key to navigate to the Set Address field on the right side of the screen.
19. Press Enter when the value is highlighted and use Backspace to clear the current value.
20. Enter “2F5B” (capital letters are not required) for the address and then press Enter.
21. Use the arrow keys to navigate to the value for address “2F5B”.
22. Press Enter when the value is highlighted and then use Backspace to clear the current value.
23. Type “0003” for the value and then press Enter.
24. Use the right arrow key to navigate to the Set Address field on the right side of the screen.
25. Press Enter when the value is highlighted and then use Backspace to clear the current value.



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