Features

- 68 Pins
- 24 I/O Pins
- 29 Dedicated Inputs
- 52 Flip-Flops
- Foldback NAND Structure
- Full Connectivity
- Erasable Version and One Time Programmable Version Available
- Scan Test
- Power Down Mode
- Power on Reset
- 100% Testable
- Power Dissipation (TTL) = 630 mW
- Power Dissipation (CMOS) = 525 mW
- Power Dissipation (Power-Down Mode) = 52 mW
- Security Fuse for Copy Protection
- Reprogrammable
- Second Source to Signetic's PML2552

CMOS High Density Programmable Macro Logic

8

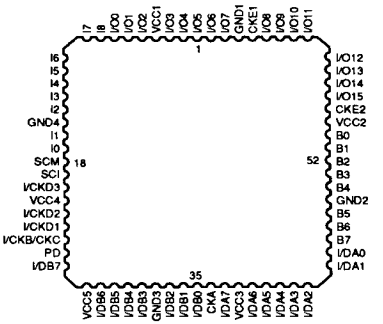
Description

The Atmel ATS2552 provides "instant gate array" capabilities for general purpose logic integration applications. Fabricated in Atmel's high-performance EPROM process, it is an ideal way to reduce NRE costs, inventory problems, and quality concerns. The ATS2552 incorporates a folded NAND array architecture which provides 100% connectivity to eliminate routing restrictions. What distinguishes the ATS2552 from the "classic" PLD architectures is its flexibility and the potent flip-flop building blocks. The device utilizes a folded NAND architecture, which enables the designer to implement multiple levels of logic on a single chip. The ATS2552 eliminates the NRE costs, risks, and hard to use design tools associated with semicustom and full custom approaches. It allows the system designer to manage reliable functionality, in less time and space plus a faster time to market. The ATS2552 is ideal in today's instrumentation, industrial control, EISA, bus interface and dense state machine applications in conjunction with the state-of-the-art CMOS processors. It is capable of replacing large amounts of TTL, SSI and MSI logic and literally allows the designer to build a system on the chip.

Development software gives easy access to the density and flexibility of the ATS2552 through a variety of design entry formats, including schematic, logic equations, and state equations in any combination. The ATS2552 is supported by Signetic's SNAP and SLICE development systems, as well as third-party tools such as ABEL™ and CUPL™.

Pin Configurations

Pin Name	Function
I#/CLK	Clock and Logic Input
I#	Logic Inputs
F#	Bidirectional Buffers
*	No Internal Connection
Vcc	+5V Supply



ABEL™ is a trademark of Data I/O Corporation.
CUPL™ is a trademark of Logical Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM

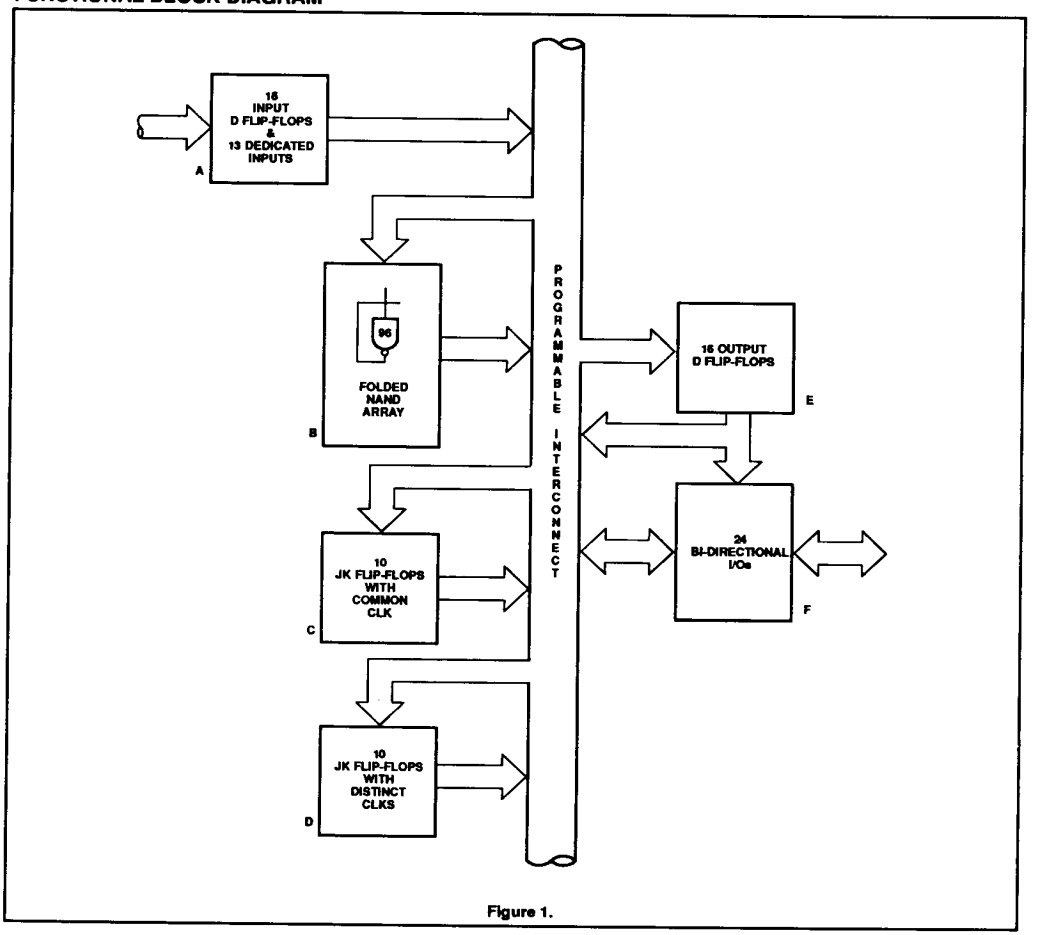
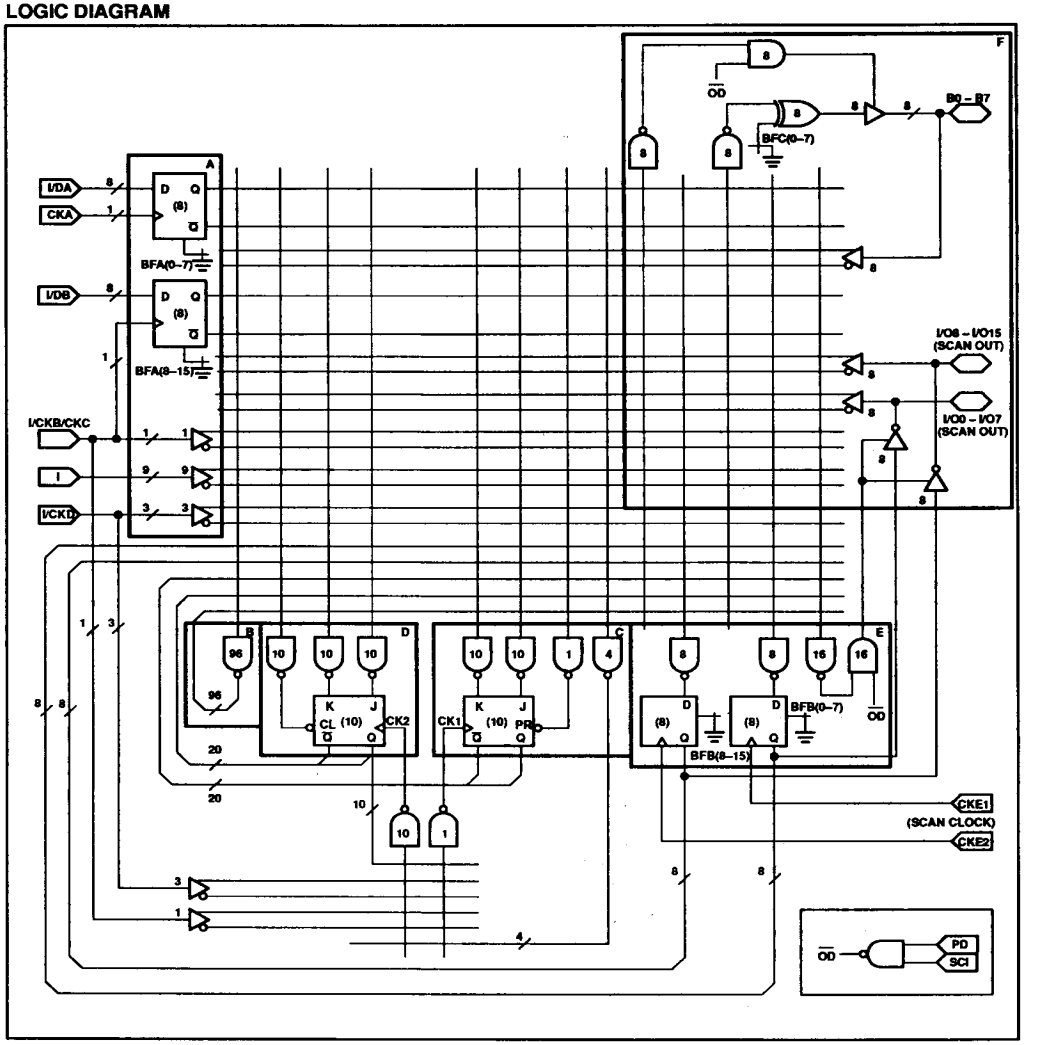


Figure 1.

LOGIC DIAGRAM



STRUCTURE

- 112 possible foldback NAND gates:
  - 96 internal NAND
  - 16 from the I/O macros
- 114 additional logic terms
- 53 possible inputs (with programmable polarity)
  - 29 dedicated inputs
  - 24 bidirectional I/Os
- 24 bidirectional pins
- 52 flip-flops
- 24 possible outputs with individual Output Enable control (8 with programmable polarity)
- Multiple independent clocks
- 20 Buried JK-type flip-flops with foldback (JKFFs):
  - 10 JKFFs with one shared preset signal and one shared clocked signal originating from the clock array.
  - 10 JKFFs with 10 independent clock signals originating from the clock array and 10 independent clear signals
- 258 inputs per NAND gate
- Bypassable Input D-type flip-flop (DFFs)/Combinatorial Inputs:
  - 16 DFFs/combinatorial inputs
  - DFFs clocked in two groups of eight
  - DFFs not bypassed in unprogrammed state
  - Independent bypass fuse on each DFF
- Inputs/bypassable D-type flip-flop outputs/foldback NAND gates:
  - 16 output DFFs/combinatorial inputs/outputs with individual Output Enable control
  - DFFs clocked in two groups of eight
  - DFFs not bypassed in unprogrammed state
  - Independent bypass fuse on each DFF
  - The DFF can be used as an internal DFF or an internal foldback NAND gate.
- Combinatorial inputs:
  - 9 dedicated inputs to the NAND array
  - 3 inputs optional to NAND array and/or clock array
  - 1 input optional to NAND array and/or clock array, and/or clock of Input D Flip-Flops (Group B)
- Separate clock array:
  - Separate clock array for JKFFs clock inputs
  - 4 inputs to clock array originated from NAND array
  - 4 inputs (with programmable polarity) directly from input pins
  - 10 inputs from Q outputs of JKFFs with clear
- Dedicated clocks:
  - One dedicated clock for input DFFs (Group A)
  - Two dedicated clocks for output DFFs
- Scan test feature:
  - Scan chain is implemented through the 20 buried JKFFs and 16 output DFFs
  - Pins SCI, SCM, and CKE1 are used to operate the scan test
- Power down mode
  - Dedicated pin (PD) freezes the circuit when brought to logic "1". The circuit remains in the same state prior to the logic "0" to logic "1" transition of the "PD" pin.
  - When in the power down mode, the SCI pin acts as the 3-State pin for the 24 outputs.
- Power on reset:
  - All flip-flops (16 input DFFs, 20 buried JKFFs, and 16 output DFFs) are reset to logic "0" after V_{CC} power on.

ARCHITECTURE

The core of the PML2552 is a programmable NAND array of 96 NAND gates and 20 buried JKFFs. The output of each NAND gate folds back upon itself and all other NAND gates and flip-flops. The 'Q' and '$\overline{Q}$' output of each flip-flop also folds back in the same manner. Thus, total connectivity of all logic functions is achieved in the PML2552. Any logic function can be created within the core without wasting valuable I/O pins. Furthermore, a speed advantage is acquired by implementing multi-level logic within a fast internal core without incurring any delays from the I/O buffers. Figure 1 shows the functional block diagram of the PML2552.

Macro Cells

There are 16 bypassable DFFs on the input to the NAND array. These flip-flops are split in two banks of 8 (Bank A and Bank B). Each bank of flip-flops has a common clock. In the unprogrammed state of the device the flip-flops are active. In order to bypass any DFF, its respective bypass fuse (BFA_X) must be programmed.

The 16 I/O pins (IO_0 - IO_{15}) and their respective D flip-flop macros can be used in any one of the following configurations:

1. As combinatorial input(s).
   Each of the 16 3-State outputs can be individually disabled by the associated NAND term and the pin is used as an inverting or non-inverting input.
2. As registered DFF outputs.
   These DFFs are split into two banks of 8, and each bank is clocked separately. The bypass fuse BFB_X (see PML2552 Logic Diagram) is used to bypass any one of these DFFs. The flip-flops are all active in an unprogrammed device.
3. As combinatorial outputs.
   By programming the bypass (BFB_X) fuse of any one of the DFFs, the flip-flop(s) is bypassed. The I/O pin can then be used as a combinatorial output.
4. As Internal foldback DFFs or foldback NAND gates.
   When the I/O pin is used as an input, the output macro can be used as an internal DFF or a foldback NAND term. If the bypass fuse is programmed, the macro will act as a foldback NAND term. Otherwise it will act as an internal DFF.

The 8 bidirectional pins (B0-B7) can be used as either combinatorial inputs or outputs with programmable polarity. The Exclusive-OR polarity gates are non-inverting in the unprogrammed state.

The NAND signal labeled '$\overline{OD}$' (Output Disable) shown on the PML2552 logic diagram is used for the Power Down mode operation. This signal disables the outputs when the device enters the Power Down mode and SCI is high.

Clock Array

The 20 buried JKFFs can be clocked through the 'Clock Array'. The Clock Array consists of 11 NAND terms. Ten of these terms are connected to the clock inputs of the Bank A flip-flops that can be clocked individually. One NAND gate is connected to Bank B flip-flops that have a common clock. There are 18 inputs to the clock array. Four come directly from the input pins (with programmable polarity), 4 inputs are from 4 NAND gates connected directly to the folded NAND array. 10 inputs are from the Q outputs of the JKFFs with clear.

SCAN TEST FEATURE

With the rise in the ratio of devices on a chip to the number of I/O pins, Design For Testability is becoming an essential factor in logic design methodology. The PML2552 incorporates a variable length scan test feature which permits access to the internal flip-flop nodes without requiring a separate external I/O pin for each node accessed. Figure 2 (Scan Mode Operation) shows how a scan chain is implemented through the 20 buried JKFFs and 16 output DFFs. Two dedicated pins, SCI (Scan In) and SCM (Scan Mode), are used to operate the scan test. The SCM pin is used to put the circuit in scan mode. When this pin is brought to a logic "1", the circuit enters the scan mode.

In this mode it is possible to shift an arbitrary test pattern into the flip-flops. The SCI pin is used to input the pattern. The inverted outputs of flip-flops D0 - D15 are observable on pins I/O0 - I/O15.

The following are features and characteristics of the device when in Scan Mode:

1. CKE1 is the common scan-clock for all the flip-flops when in scan mode. CKE1 overrides all clock resources of normal operational mode.
2. The Preset (PR) and Clear (CL) functions of the flip-flops are disabled.
3. Scan overrides the bypass fuse of the flip-flops. This means that all the bypassable DFFs remain intact during scan operation even though they may have been bypassed during normal operation.
4. To observe the SCAN data, the output buffers must be enabled by the Output Enable (tri-ctrl) terms.
5. The outputs of the flip-flops are complemented on pins I/O0 - I/O15.
6. All external inputs to flip-flops in the scan chain are disabled when the device enters the scan mode.
7. Blowing the security fuse does not disable the Scan Test feature.

SCAN MODE OPERATION

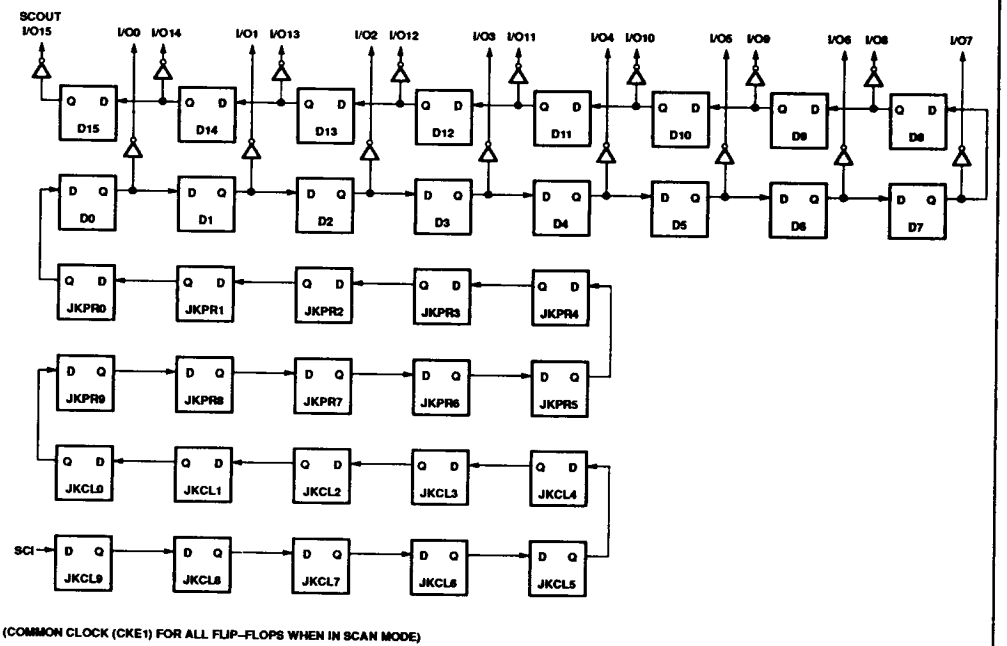


Figure 2.

SCAN TEST STRATEGY

The scan test pattern is design dependent and the user must make considerations for Design For Testability (DFT) during the initial stages of the design. A typical test sequence is to pre-load (i.e., enter a state); revert to normal operation (i.e., activate the next state transition); go back to scan mode to check the result. Note that the scan test feature available in the PML2552 is a variable length scan chain. The DATA entered at SCI (JKCL9) can be accessed anywhere between 21 clock cycles (at I/O0) to 36 clock cycles (at I/O15). For the strategy discussed here, DATA is read out after 36 clocks at I/O15 (i.e., D15). The following operation sequence suggests a possible scan test method.

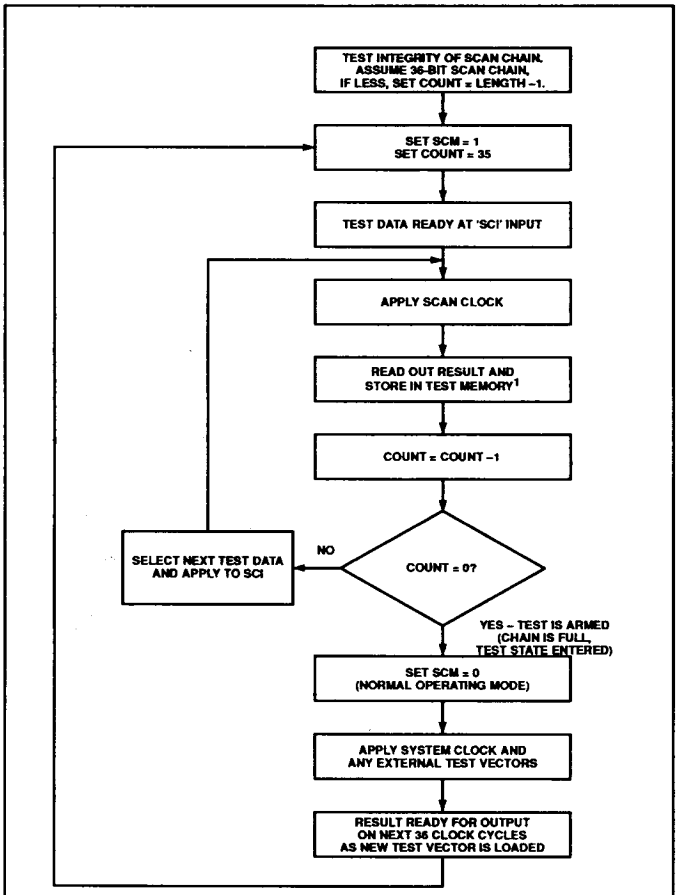
A conservative test policy demands proof that the test facility is working. Thus, to prove Scan Chain holds and maintains correct data:

a. Fill chain with several patterns (for example, all ones and all zeros).

b. Retrieve same patterns.

The user is responsible for managing an external test memory buffer for applied vectors and results, as part of the test equipment.

1. Parallel readout of I/O0 - I/O15 is possible, but assume only I/O15 is used for this strategy.
2. The first DATA entered at SCI (or JKCL9) will be the content of D15 after 36 clocks. This DATA will be inverted at the output pin I/O15 (i.e., SCOUT). The last DATA entering the scan chain will be the content of JKCL9. Thus, the scan chain resembles a first-in-first-out shift register with inverted outputs (I/O0 - I/O15).
3. 'Test Data' is read in at the SCI input and read out of the SCOUT output pin (I/O15). To enter 'Test Data':
   a. Put device in Scan Mode by applying the scan control signals (SCM=1).
   b. Clock device with scan clock (CKE1).
   c. Apply consecutive serial test vectors.
   d. Read back results as new 'Test Data' (States) are applied. The first 36 outputs read at SCOUT (I/O15) are random ('old') data (e.g., remnant of Step 1).
   e. Apply 36 'Test Data' until the chain is full.
4. To apply 'Test Data' (States), exit Scan Mode and apply on system clock together with any other possible test vectors.
5. To read result of the state transition, re-enter scan and apply the scan clock (CKE1). The result of the state transition in JKCL9 will be available at SCOUT (I/O15) after 36 clocks. The results can be stored in a user defined test memory buffer in inverted logic representation.
6. As the results are being read and stored, new 'Test Data' can be entered via SCI.
7. Repeat for all test patterns of interest.
8. Figure 3 (FLOW_CHART) depicts a flow chart version of the test sequence.



NOTE:
1. The first 36 outputs are random ('OLD') data.

Figure 3. FLOW_CHART

A Simple Example

Assume the last three cells of the scan chain (JKCL9, JKCL8, JKCL7 in Figure 4 contain a 3-bit up counter. Our test vector will be a single clock applied to the counter. Suppose we wish to first check the *State 5* (i.e., 101) to *State 6* (i.e., 110) transition, then the *State 3* (i.e., 011) to *State 4* (i.e., 100) transition. Assume the scan chain has been pre-verified and we may begin.

Enter scan mode (set SCM=1)I apply 36 bits in sequence so that the value *101* (i.e., State 5) resides in the last three cells. Exit scan mode (set SCM=0) and apply a single clock to the counter. Now the value *110* (i.e., State 6) resides in the last three cells. Re-enter scan mode (set SCM=1) and read back 36 bits from position I/O15. Note that the outputs are complemented and are also read back in the reverse order. Therefore the value for *STATE 6* read at I/O15 will be 100 which is the complement of *STATE 6* (110) read in the reverse order.

As this is being read back, apply a new state, serially equal to the value *011* (i.e., State 3). This state should be loaded on the last three clock cycles during which *STATE 6* is being read back at I/O15. After *STATE 3* has been loaded (and *STATE 6* read back), exit scan mode and apply a single clock which will invoke the *STATE 3* (i.e., 011) to *STATE 4* (i.e., 100) transition. Re-enter scan mode and read back 36 bits at I/O15. The last three bits should contain *110* which is the complement of *State 4* read in the reverse order. Figure 4 (SCAN_EXAMPLE) shows a flow diagram of this example. Note that the States will always be complemented and read back in the reverse at I/O15. Other sequences may be applied in the same manner.

A possible alternative to this example is to read back the output states at I/O0 (D0) instead of I/O15 (JKCL9). This will allow the outputs to be read back after 21 clock cycles rather than the 36 used in the above example.

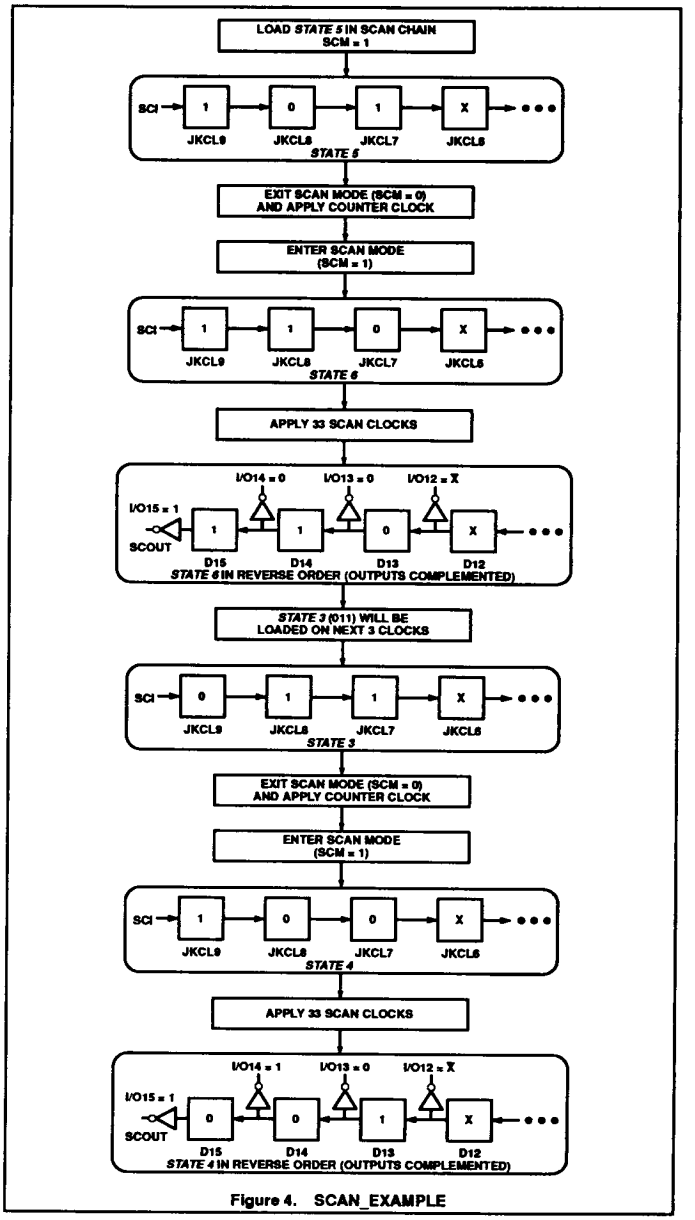


Figure 4. SCAN_EXAMPLE

8

POWER DOWN

The PML2552 offers the user controlled capability of putting the device to "sleep" where power dissipation is reduced to very low levels. When brought to a logic "1", the PD pin freezes the circuit while reducing the power. All data is retained. This not only includes that of the registers, but also the state of each foldback gate. For those cases where it is desirable to 3-State the outputs, that can be accomplished by raising the SCI pin to a logic "1".

There is one point that should be noted while the circuit is in its power-down mode. The switching of any external clock pin will cause a disruption of the data. All clocks must be frozen before the circuit goes into power-down and stay that way until it powered back up. Clocks that are internally generated and feed the clock array are automatically stopped by the power-down circuitry. Any other input can toggle without any loss of data.

NOTE:
1. During power down, external clocks (CKA, CKB/CKC, CKE1, CKE2) should not change.
2. SCM must be "0" as in normal operation mode.
3. External clock recovery time (low-to-high) is 60ns (high-speed) and 70ns (standard) after the device is powered up.
4. Power Down Timing Diagrams on pages 17 and 18 are for combinatorial operation only.

DEVELOPMENT TOOLS

The PM2552 is supported by the Signetics SNAP software development package and a multitude of hardware and software development tools. These include industry standard PLD programmers and CAD software.

SNAP

Features

- Schematic entry using DASH™ 4.0 or above or OrCAD™ SDT III
- State Equation Entry
- Boolean Equation Entry
- Allows design entry in any combination of above formats
- Simulator
  - Logic and fault simulation
  - Timing model generation for device timing simulation
  - Synthetic logic analyzer format
- Macro library for standard TTL and user defined functions
- Device independent netlist generation
- JEDEC fuse map generated from netlist

SNAP (Synthesis, Netlist, Analysis and Program) is a versatile development tool that speeds the design and testing of PML. SNAP combines a user-friendly environment and powerful modules that make designing with PML simple. The SNAP environment gives the user the freedom to design independent of the device architecture.

The flexibility in the variations of design entry methodologies allows design entry in the most appropriate terms. SNAP merges the inputs, regardless of the type, into a high-level netlist for simulation or compilation into a JEDEC fuse map. The JEDEC fuse map can then be transferred from the host computer to the device programer.

SNAP's simulator uses a synthetic logic analyzer format to display and set the nodes of the design. The SNAP simulator provides complete timing information, setup and hold-time checking, plus toggle and fault grading analysis.

SNAP operates on an IBM® PC/XT, PC/AT, PS/2, or any compatible system with DOS 2.1 or higher. A minimum of 640K bytes of RAM is required together with a hard disk.

SLICE

SLICE, which supports Atmel's PLD line, is easy to understand and simple to use. Select a PLD, assign input and output pins and enter the desired equations in either Boolean or state form. SLICE then checks the equations for errors. It automatically generates a JEDEC-format fuse map for downloading to a PLD programmer.

Fully menu driven, SLICE incorporates a fuse table editor for making quick modifications to the design and a test vector editor for input of test vectors.

A built-in Boolean equation extractor allows existing PLDs to be used as the basis for a new design. the extractor reads JEDEC information from a PLD and creates a file containing the corresponding Boolean equations. The result can then be used to consolidate several PLD designs into a single, denser part.

And SLICE is upward compatible with Signetics extensive design suite, SNAP.

DESIGN SECURITY

The PML2552 has a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary design implemented in the device cannot be copied or retrieved.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	–30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DASH is a trademark of Data I/O Corporation.
OrCAD is a trademark of OrCAD, Inc.
IBM is a registered trademark of International Business Machines Corporation.

DC ELECTRICAL CHARACTERISTICS

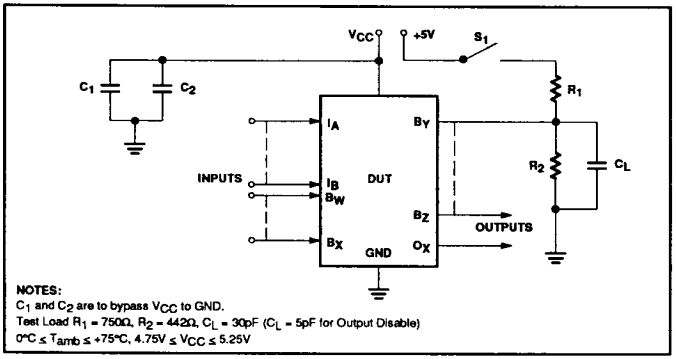
$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Input voltage							
V_{IL}	Low	V_{CC} = MIN		–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX		2.0		V_{CC} + 0.3	V
Output voltage							
V_{OL}	Low	V_{CC} = MIN, I_{OL} = 5mA				0.45	V
V_{OH}	High	V_{CC} = MIN, I_{OH} = –2mA		2.4			V
Input current							
I_{IL}	Low	V_{IN} = GND				–10	µA
I_{IH}	High	V_{IN} = V_{CC}				10	µA
Output current							
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC}				10	µA
		V_{OUT} = GND				–10	µA
I_{OH}	Output High	V_{CC} = MIN, V_{OUT} = 2.4V				–2	mA
I_{OL}	Output Low	V_{CC} = MIN, V_{OUT} = 0.45V				5	mA
I_{OS}	Short-circuit[5]	V_{OUT} = GND				–100	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX, No load	CMOS input[2]		60	100[6]	mA
		f = 1MHz	TTL input[3]		65	120[6]	mA
I_{SB}	Standby V_{CC} supply current	V_{CC} = MAX, No load	CMOS input		1.0	10	mA
		PD = V_{IH}	TTL input		1.5	10	mA
Capacitance							
C_{IN}	Input	V_{CC} = 5V, T_{amb} = +25°C, V_{IN} = 2.0V			8		pF
C_B	I/O	V_{CC} = 5V, T_{amb} = +25°C, V_{IO} = 2.0V			16		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. CMOS inputs: V_{IL} = GND, V_{IH} = V_{CC}.
3. TTL inputs: V_{IL} = 0.45V, V_{IH} = 2.4V.
4. All voltage values are with respect to network ground terminal.
5. Duration of short-circuit should not exceed one second. Test one at a time.
6. ΔI_{CC} vs. Frequency = 4mA/MHz max.

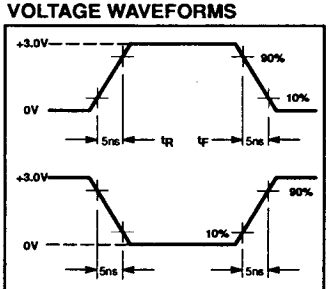
8

TEST LOAD CIRCUITS



NOTES:
C_1 and C_2 are to bypass V_{CC} to GND.
Test Load R_1 = 750Ω, R_2 = 442Ω, C_L = 30pF (C_L = 5pF for Output Disable)
$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

MACRO CELL AC SPECIFICATIONS

Min: 0°C, 5.25V; Typ: 25°C, 5.0V; Max: 75°C, 4.75V (SNAP Resource Summary Designations in Parentheses)

Input Buffer
(DIN552, NIN552, BDIN55, BNIN552 CDIN552, CNIN552, CKDIN552, CKNIN552)

SYMBOL	PARAMETER		LIMITS						UNIT
	To	From	PML2552-35			PML2552-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	X	I	5	7	10	7	10	15	ns
t_{PLH}	X	I	5	7	10	7	10	15	ns
t_{PHL}	Y	I	5	7	10	7	10	15	ns
t_{PLH}	Y	I	5	7	10	7	10	15	ns

Input Pins: 8–14, 16, 17, 20, 22–24.
Bidirectional Pins: 1–3, 5–7, 46–48, 50–54, 57–64, 67, 68.

Internal NAND of Main Array
(FBNAND, NAND)

SYMBOL	PARAMETER		LIMITS			LIMITS			UNIT
	To	From	PML2552-35			PML2552-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Y	X	10	15	20	12	18	25	ns
t_{PLH}	Y	X	10	15	20	12	18	25	ns

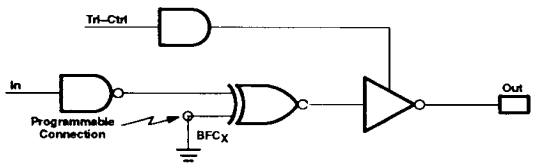
Internal NAND of Clock Array
(NAND)

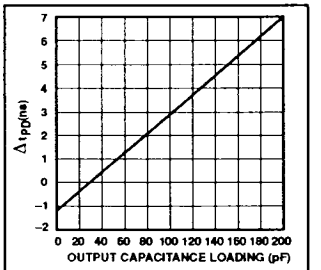
SYMBOL	PARAMETER		LIMITS			LIMITS			UNIT
	To	From	PML2552-35			PML2552-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Y	X	5	7	10	7	10	15	ns
t_{PLH}	Y	X	5	7	10	7	10	15	ns

MACRO CELL AC SPECIFICATIONS (Continued)

Min: 0°C, 5.25V; Typ: 25°C, 5.0V; Max: 75°C, 4.75V (SNAP Resource Summary Designations in Parentheses)

3-State Output with Programmable Polarity (TOUT552 + EXOR552)



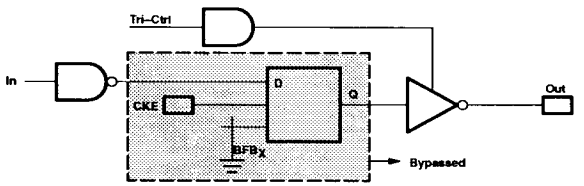


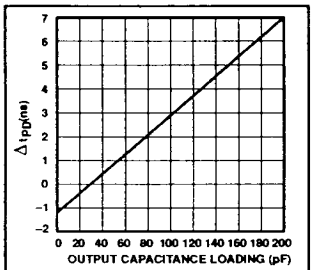
Δt_{PD} vs Output Capacitance Loading (Typical)

SYMBOL	PARAMETER		LIMITS						UNIT
	To	From	PML2552-35			PML2552-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Out	In	12	18	25	17	25	35	ns
t_{PLH}	Out	In	12	18	25	17	25	35	ns
t_{OE}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns
t_{OD}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns

Bidirectional Pins: 46–48, 50–54.

I/O Output Buffer with 3-State Control, DFF Bypassed (TOUT552 + NAND)





Δt_{PD} vs Output Capacitance Loading (Typical)

SYMBOL	PARAMETER		LIMITS						UNIT
	To	From	PML2552-35			PML2552-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Out	In	12	18	25	17	25	35	ns
t_{PLH}	Out	In	12	18	25	17	25	35	ns
t_{OE}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns
t_{OD}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns

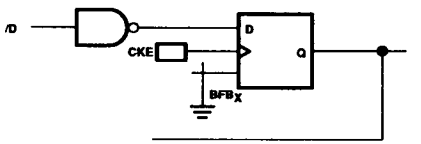
I/O Pins: 1–3, 5–7, 57–64, 67, 68.

Notes on page 8-157

8

MACRO CELL AC SPECIFICATIONS (Continued) (SNAP Resource Summary Designations in Parentheses)
D FLIP-FLOP

Output DFF Used Internally
(ODFF552)



SYMBOL	PARAMETER	LIMITS						UNIT
		PML2552-35			PML2552-50			
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{CKE}	Flip-flop toggle rate			50			35	MHz
$t_{W\,CKE}$ High	Clock HIGH	10			14			ns
$t_{W\,CKE}$ Low	Clock LOW	10			14			ns
t_{SETUP} /D	/D setup time to CKE	15			20			ns
t_{HOLD} /D	/D hold time to CKE	4			6			ns

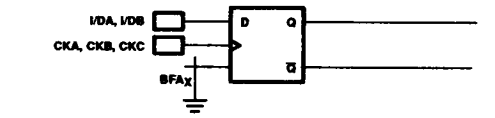
SYMBOL	PARAMETER		LIMITS						UNIT
	From	To	PML2552-35			PML2552-50			
	(Input)	(Output)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CKE ↑	Q	10	15	20	14	20	25	ns
t_{PHL}	CKE ↑	Q	10	15	20	14	20	25	ns

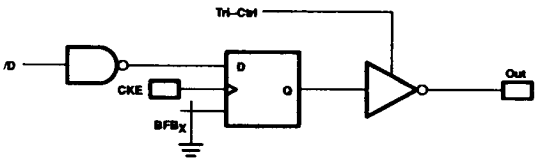
MACRO CELL AC SPECIFICATIONS (Continued) (SNAP Resource Summary Designations in Parentheses)
D FLIP-FLOP (Continued)

Input and Output
(IDFF552 & ODFF552)

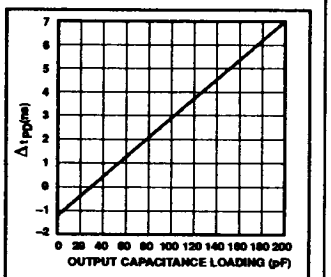
INPUTS		OUTPUTS	
CK	D	Q	$\overline{Q}$
L	X	Q_0	$\overline{Q}_0$
↑	H	H	L
↑	L	L	H

NOTE:
Q_0, $\overline{Q}_0$ represent previous stable condition of Q, $\overline{Q}$.





SYMBOL	LIMITS						UNIT
	PML2552-35			PML2552-50			
	MIN	TYP	MAX	MIN	TYP	MAX	
$f_{CKA, CKB, CKC}$			50			35	MHz
$t_{W\ CKA, CKB, CKC}$ High	10			14			ns
$t_{W\ CKA, CKB, CKC}$ Low	10			14			ns
t_{SETUP} I/DA, I/DB	5			7			ns
t_{HOLD} I/DA, I/DB	5			7			ns
f_{CKE}			50			35	MHz
$t_{W\ CKE}$ High	10			14			ns
$t_{W\ CKE}$ Low	10			14			ns
t_{SETUP} /D	15			20			ns
t_{HOLD} /D	4			6			ns



Δt_{PD} vs Output Capacitance Loading (Typical)

SYMBOL	PARAMETER		LIMITS						UNIT
	From (Input)	To (Output)	PML2552-35			PML2552-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CKA, CKB/CKC ↑	Q, $\overline{Q}$	5	7	10	7	10	15	ns
t_{PHL}	CKA, CKB/CKC ↑	Q, $\overline{Q}$	5	7	10	7	10	15	ns
t_{PLH}	CKE ↑	Out	12	18	25	17	25	35	ns
t_{PHL}	CKE ↑	Out	12	18	25	17	25	35	ns

8

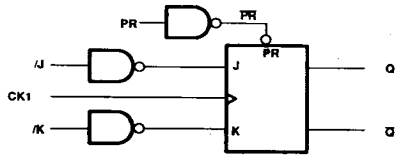
MACRO CELL AC SPECIFICATIONS (Continued) (SNAP Resource Summary Designations in Parentheses)
JK FLIP-FLOPS

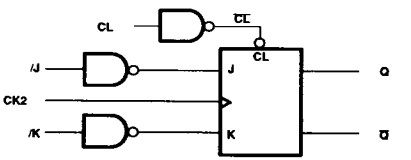
(JKPR552)

INPUTS				OUTPUTS	
$\overline{PR}$	CK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↑	L	L	Q_0	$\overline{Q}_0$
H	↑	H	L	H	L
H	↑	L	H	L	H
H	↑	H	H	TOGGLE	
H	L	X	X	Q_0	$\overline{Q}_0$

(JKCL552)

INPUTS				OUTPUTS	
$\overline{CL}$	CK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↑	L	L	Q_0	$\overline{Q}_0$
H	↑	H	L	H	L
H	↑	L	H	L	H
H	↑	H	H	TOGGLE	
H	L	X	X	Q_0	$\overline{Q}_0$





SYMBOL	PARAMETER	LIMITS						UNIT
		PML2552-35			PML2552-50			
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{CK1}	CK1 toggle frequency			50			35	MHz
f_{CK2}	CK2 toggle frequency			50			35	MHz
$t_{W\,CK1}$ High	CK1 clock HIGH	10			14			ns
$t_{W\,CK1}$ Low	CK1 clock LOW	10			14			ns
$t_{W\,CK2}$ High	CK2 clock HIGH	10			14			ns
$t_{W\,CK2}$ Low	CK2 clock LOW	10			14			ns
t_{SETUP} /J, /K	/J, /K setup time to CK1, CK2	27			35			ns
t_{HOLD} /J, /K	/J, /K hold time to CK1, CK2	0			0			ns
t_W PR Low	Preset Low period	10			14			ns
t_W CL Low	Clear Low period	10			14			ns

SYMBOL	PARAMETER		LIMITS						UNIT
	From (Input)	To (Output)	PML2552-35			PML2552-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CK1,2	Q, $\overline{Q}$	2	3.5	5	3	5	7	ns
t_{PHL}	CK1,2	Q, $\overline{Q}$	2	3.5	5	3	5	7	ns
t_{PLH}	PR	Q, $\overline{Q}$	12	18	25	17	24	30	ns
t_{PHL}	PR	Q, $\overline{Q}$	12	18	25	17	24	30	ns
t_{PLH}	CL	Q, $\overline{Q}$	12	18	25	17	24	30	ns
t_{PHL}	CL	Q, $\overline{Q}$	12	18	25	17	24	30	ns

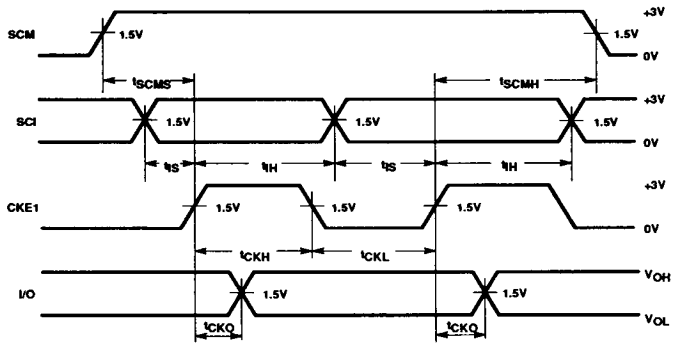
AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $V_{PP} = V_{CC}$,
$R_1 = 750\Omega$, $R_2 = 442\Omega$, $C_L = 5pF$ for Output Disable) (See Test Load Circuit Diagram)

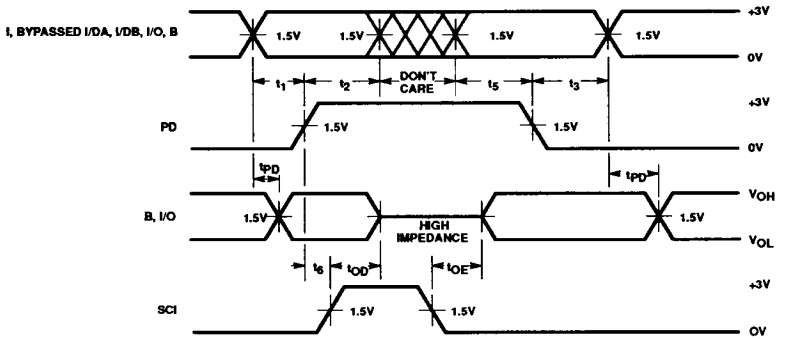
SYMBOL	PARAMETER	LIMITS				UNIT
		PML2552-35		PML2552-50		
		MIN	MAX	MIN	MAX	
Scan mode operation[1]						
t_{SCMS}	Scan Mode (SCM) Setup time	15		15		ns
t_{SCMH}	Scan Mode (SCM) Hold time	25		30		ns
t_{IS}	Data Input (SCI) Setup time	5		5		ns
t_{IH}	Data Input (SCI) Hold time	5		5		ns
t_{CKO}	Clock to Output (I/O) delay		30		40	ns
t_{CKH}	Clock High	10		15		ns
t_{CKL}	Clock Low	10		15		ns
Power down, power up[2]						
t_1	Input (I, bypassed I/DA, I/DB, I/O, B) setup time before power down	40		50		ns
t_2	Input hold time	30		35		ns
t_3	Power Up recovery time		60		70	ns
t_4	Output hold time	0		0		ns
t_5	Input setup time before Power Up	20		25		ns
t_{OE}	SCI to Output Enable time[3]		40		50	ns
t_{OD}	SCI to Output Disable time[3]		40		50	ns
t_6	Power Down setup time	10		15		ns
t_7	Power Up to Output valid		70		80	ns
Power-on reset						
t_{PPR1}	Power-on reset output register (Q = 0) to output (I/O) delay		10		15	ns
t_{PPR2}	Power-on reset input register (Q = 0), buried JK Flip-Flop (Q = 0) to output (B, bypassed I/O) delay		40		50	ns

NOTES:
1. SCM recovery time is 50ns after SCM operation. 50ns after SCM operation, normal operations can be resumed.
2. Timings are measured without foldbacks.
3. Transition is measured at steady state High level (–500mV) or steady state Low level (+500mV) on the output from 1.5V level on the input with specified test load ($R_1 = 750\Omega$, $R_2 = 442\Omega$, $C_L = 5pF$). This parameter is sampled and not 100% tested.
4. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

TIMING DIAGRAMS

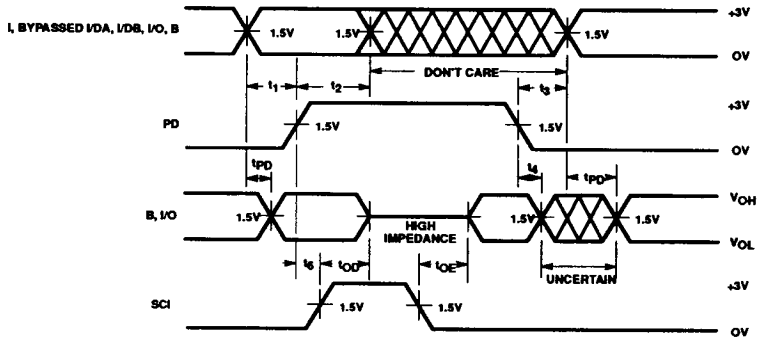


Scan Mode Operation

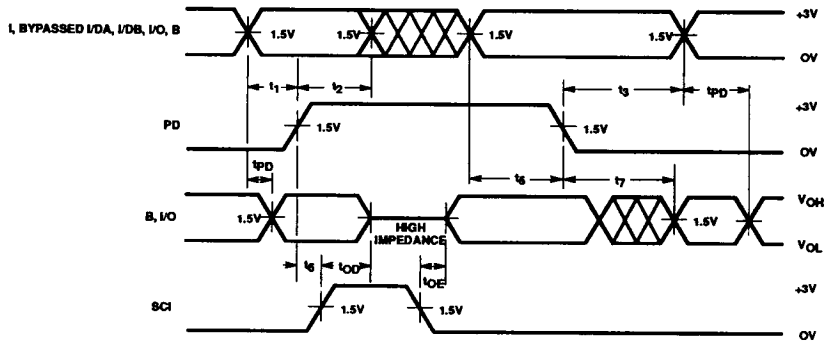


Power Down, Power Up
Input (old) Ready Before Power Up

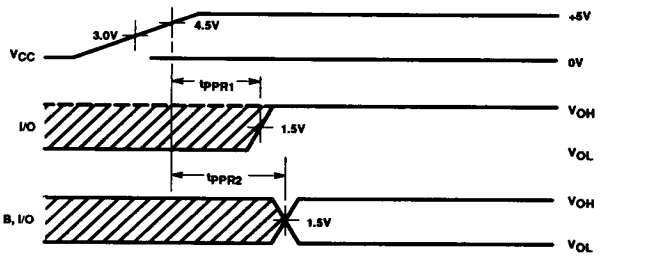
TIMING DIAGRAMS (Continued)



Power Down, Power Up
Input (new) Ready After Power Up



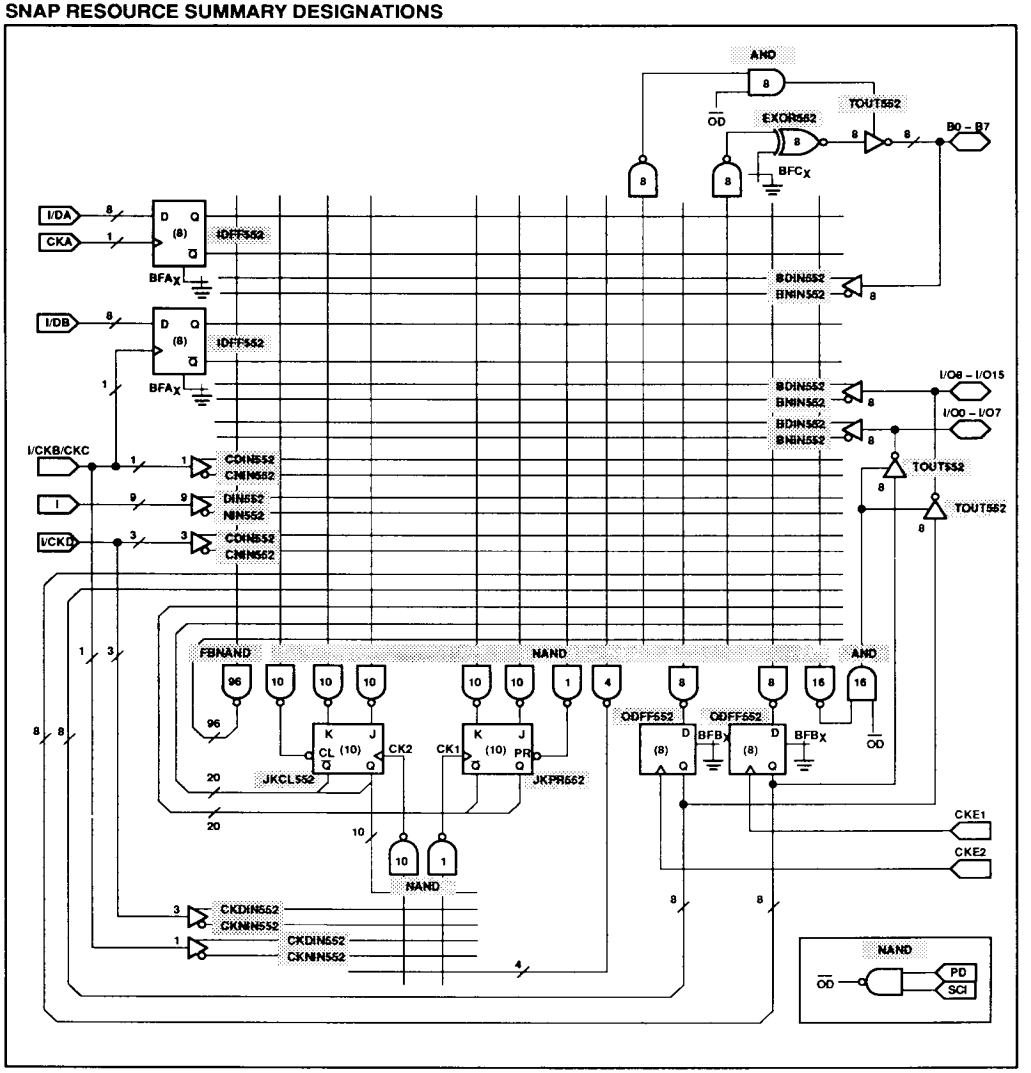
Power Down, Power Up
Input (new) Ready Before Power Up



Power-On Reset

8

SNAP RESOURCE SUMMARY DESIGNATIONS



ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PML2552 device is such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 – 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PML2552 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PML2552 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PML2552 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12,000µW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

PROGRAMMING

Refer to the following charts for qualified manufacturers of programmers and software tools:

PROGRAMMER MANUFACTURER	PROGRAMMER MODEL	FAMILY/PINOUT CODES
DATA I/O CORPORATION 10525 WILLOWS ROAD, N.E. P.O. BOX 97046 REDMOND, WASHINGTON 98073–9746 (800)247–5700	UNISITE 40/48 V2.8 Pinsite – V2.0	15908C* (with adaptor) 15908D (with pinsite)
STREBOR DATA COMMUNICATIONS 1008 N. NOB HILL AMERICAN FORK, UT 84003	PLP–S1A Programmer MP68CC Adaptor	

* Needs a 40-pin DIP to 68-pin PLCC adaptor that is available from Emulation Technology.
Part Number: AS–68–40–04P–6

EMULATION TECHNOLOGY, INC.
2368B Walsh Avenue, Blvd. D
Santa Clara, California 95051
Telephone No. (408) 982–0660
Fax. No. (408) 982–0664

SOFTWARE MANUFACTURER	DEVELOPMENT SYSTEM
SIGNETICS COMPANY 811 EAST ARQUES AVENUE P.O. BOX 3409 SUNNYVALE, CALIFORNIA 94088–3409 (408)991–2000	SNAP SOFTWARE REV. 1.4 AND LATER

8

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
35	15	25	ATS2552-35JC ATS2552-35KC	68J 68KW	Commercial (0°C to 70°C)
50	20	35	ATS2552-50JC ATS2552-50KC	68J 68KW	Commercial (0°C to 70°C)

Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)