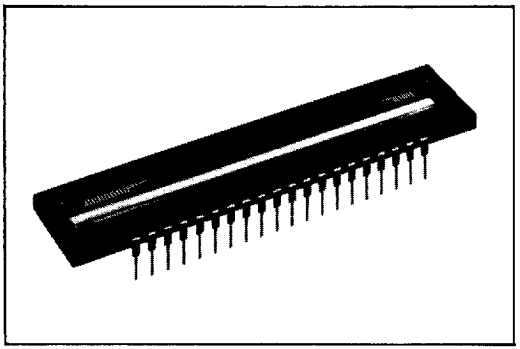
LORAL
Fairchild Imaging Sensors

**PRELIMINARY**

# CCD192
# 6000 Element
# Linear Image Sensor

## FEATURES

- **6000 × 1 photosite array**
- **10μm × 7μm photosites on 10μm pitch**
- **Anti-blooming and integration control**
- **Enhanced resolution in the red region**
- **Excellent low-light-level performance**
- **Low dark signal**
- **High-speed operation**
- **Dynamic range typical: 11000:1**
- **Over 2V peak-to-peak outputs**
- **Special selection available—consult factory**
- **AR coated window**



## GENERAL DESCRIPTION

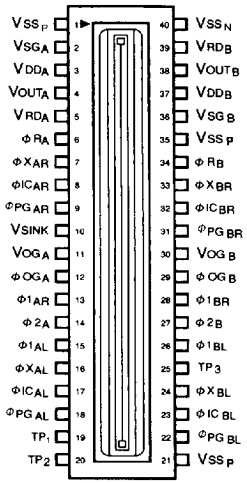
The CCD192 is a 6000 element line image sensor designed for scanning applications which require very high resolution, high sensitivity and wide dynamic range. Incorporation of on-chip anti-blooming and integration controls allow the CCD192 to be extremely useful in industrial measurement and control environments or environments where lighting conditions are difficult to control.

The CCD192 is a third generation device having an overall improved performance compared with first and second generation devices, including excellent low light level performance. The photoelement size is 10μm (0.39 mils) × 7μm (0.28 mils) on 10μm (0.39 mils) centers. The device is manufactured using Loral Fairchild's advanced charge-coupled device n-channel Isoplanar buried-channel technology.

| PIN NAME | DESCRIPTION |
|---|---|
| $V_{SG\ (A,B)}$ | Amp Signal Grounds |
| $V_{OUT_A}$ | Output Amp—A Source |
| $\Phi_{R_A}$ | Reset Gate—A |
| $V_{RD_A}$ | Reset Drain—A |
| $\Phi_{OG(A,B)}$ | Output Clock Gates |
| $V_{OG_A}$ | Output DC Gate—A |
| $\Phi_{X\ (AR,AL,BR,BL)}$ | Transfer Clocks (A & B sides, left & right)* |
| $\Phi_{2A}$, $\Phi_{2B}$ $\Phi_{1A}$,$\Phi_{1B}$ | Transport Clocks (A & B) |
| $\Phi_{IC\ (AR,AL,BR,BL)}$ | Integration Control (A & B sides, left & right)* |
| $\Phi_{PG\ (AR,AL,BR,BL)}$ | Photogates (A & B sides, left & right)* |
| TP1, TP2, TP3 | Test Points |
| $V_{SINK}$ | Anti Blooming Sink |
| $V_{OG_B}$ | Output DC Gate—B |
| $V_{RD_B}$ | Reset Drain—B |
| $\Phi_{R_B}$ | Reset Gate—B |
| $V_{OUT_B}$ | Output Amp—B Source |
| $V_{DD(A,B)}$ | Output Amp Drains |
| $V_{SS}$ | Substrate |

NOTE: Left & right pins must be connected together. Example: $\Phi PG_{AR}$ and $\Phi PG_{AL}$

**PIN DIAGRAM**

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## FUNCTIONAL DESCRIPTION

The CCD192 consists of the following functional elements illustrated in the block diagram and circuit diagram.

**Photosites** — A row of 6000 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon dioxide layer creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

**Two Transfer Gates** — Gate structures adjacent to the row of image sensor elements. The charge packets accumulated in the photosites are transferred in parallel via the transfer gates ($\phi$X) to the transport shift registers whenever the transfer gate voltages go high. Alternate charge packets are transferred to the A and B transport registers.

**Two Analog Transport Shift Registers** — The transport shift registers are used to move the light generated charge packets delivered by the transfer gates ($\phi_{1A}$, $\phi_{1B}$, $\phi_{2A}$, $\phi_{2B}$) serially to the charge detector/amplifier. The parallel layout of the last elements of the two transport registers provides for simultaneous delivery of charge packets at the output amplifiers.

**A Gated Charge Detector/Amplifier** — Charge packets are transported to a precharged capacitor whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the input gate of the two-stage NMOS amplifiers producing a signal at the output "$V_{OUT}$" pin. Before each charge packet is sensed, a reset clock ($\phi_{RA}$, $\phi_{RB}$) recharges the input node capacitor to a fixed voltage ($V_{RDA}$, $V_{RDB}$).

**Integration and Anti-Blooming Controls** — In many applications the dynamic range in parts of the image is larger than the dynamic range of the CCD, which may cause more electrons to be generated in the photosite area than can be stored in the CCD shift register. This is particularly common in industrial inspection and satellite applications. The excess electrons generated by bright illumination tend to "bloom" or "spill over" to neighboring pixels along the shift register, thus "smearing" the information. This smearing can be eliminated using two methods:

**Anti-Blooming Operation:**

A DC voltage applied to the integration control gate (approximately 1 to 3 volts) will cause excess charge generated in the photosites to be diverted to the anti-blooming sink ($V_{SINK}$) instead of to the shift registers. This acts as a "clipping circuit" for the CCD output.

**Integration Control Operation:**

Variable integration times which are less than the CCD exposure time may be attained by supplying a clock to the integration control gate. Clocking $\phi_{IC}$ reduces the integration time from $t_{EXPOSURE}$ to $t_{INT}$. Greater than 10:1 reduction in average photosite signal can be achieved with integration control.

The integration-control and anti-blooming features can be implemented simultaneously. This is done by setting the $\phi_{IC}$, clock-low level to approximately 1 to 3 volts.

## DEFINITION OF TERMS

**Charge-Coupled Device** — A charge-coupled device is a semiconductor device in which finite isolated charge packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge packets are minority carriers with respect to the semiconductor substrate.

**Prescan Reference** — Video output level generated from shift register cells which provides a reference voltage equivalent to device operation in the dark. This permits use of external DC restoration circuitry.

**Dynamic Range** — The saturation exposure divided by the RMS temporal noise equivalent exposure. Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times RMS noise.

**RMS Noise Equivalent Exposure** — The exposure level that gives an output signal equal to the RMS noise level at the output in the dark.

**Saturation Exposure** — The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosite integration time.

**Charge Transfer Efficiency** — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

**Responsivity** — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

**Total Photoresponse Non-Uniformity** — The difference of the response levels of the most and the least sensitive element undre uniform illumination. Measurements of PRNU excludes first and last elements.

**Dark Signal** — The output in the dark caused by thermally generated electrons that is a linear function of the integration time and is highly sensitive to temperature.

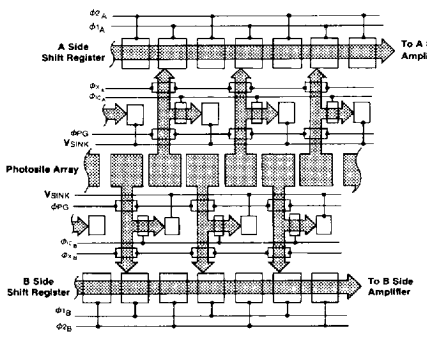
**Saturation Output Voltage** — The maximum useable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

**Integration Time** — The time interval between the falling edge of the integration clock and the falling edge of the transfer clock. The integration time in which charge is accumulated in the photosites.

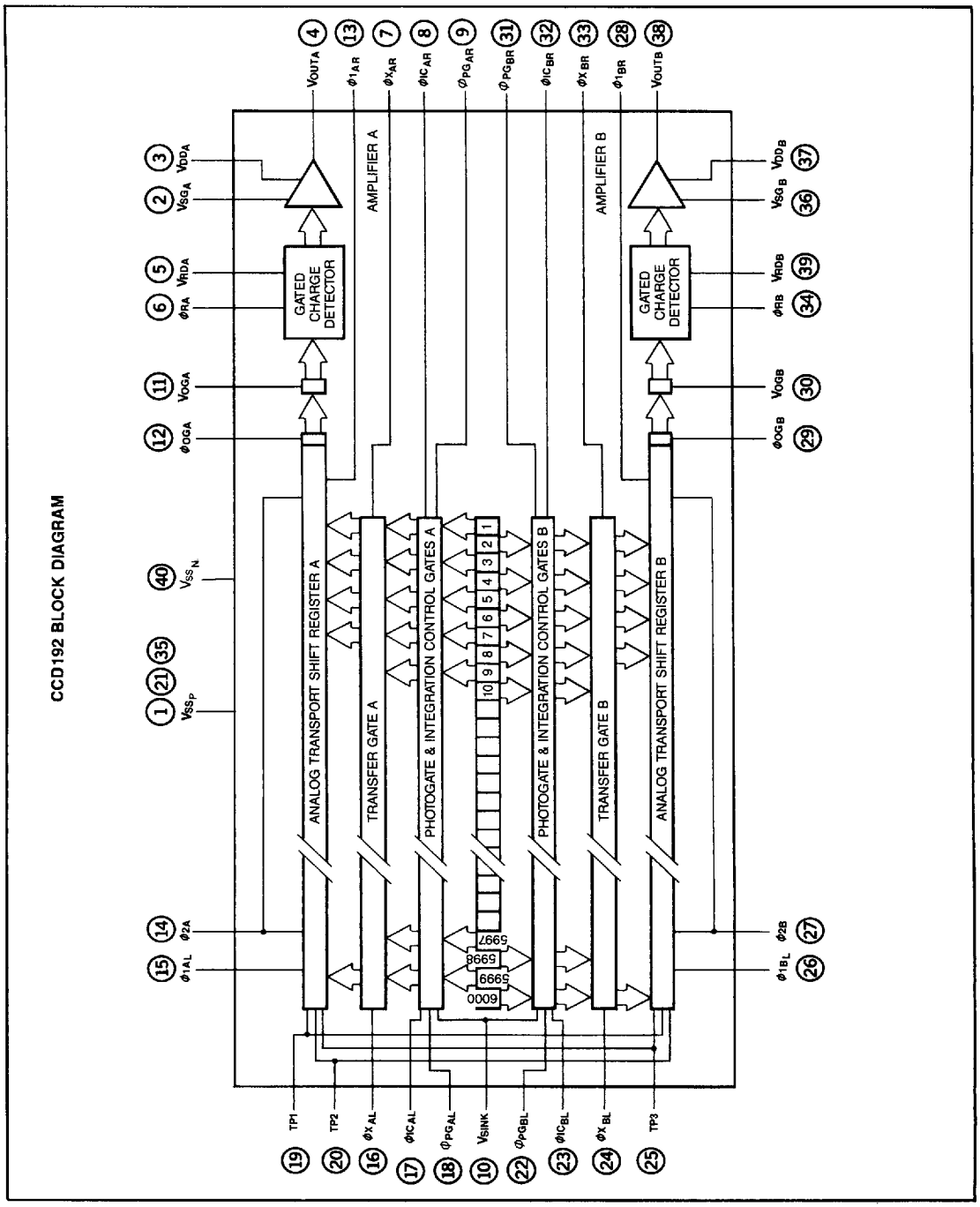
**Exposure Time** — The time interval between the falling edge of the two transfer pulses ($\phi$X) shown in the timing diagram. The exposure time is the time between transfers of signal charge from the photosites into the transport registers.

**Pixel** — A picture element (photosite).

**CCD192 CIRCUIT DIAGRAM**



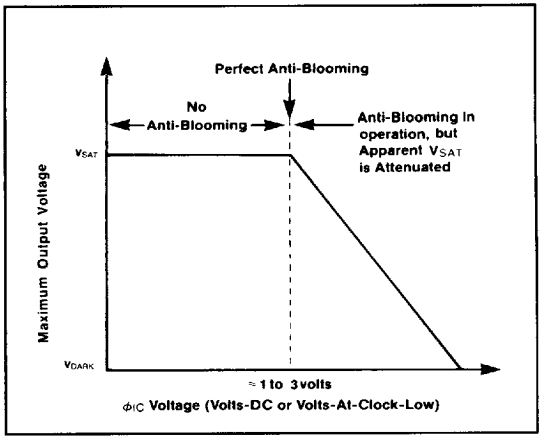
CCD192 BLOCK DIAGRAM



(above which useful life may be impaired)

| | |
|---|---|
| Storage Temperature | -25° C to +125° C |
| Operating Temperature | -25° C to +70° C |
| CCD 191: Pins 2, 36 ($V_{SG}$) | 0V |
| Pins 1, 21, 35 ($V_{SSP}$) | -3.0V to 0V |
| Pins 4, 38 ($V_{OUT}$) | See Caution Note |
| Pin 40 ($V_{SSN}$) | 0V to +5V |
| All other pins | -3.0V to +18V |

**CAUTION NOTE:**
These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $V_{OUTA+B}$ to $V_{SS}$ or $V_{DD}$ during operation of the devices. Shorting these pins temporarily to $V_{SS}$ or $V_{DD}$ may destroy the output amplifiers.




**DC CHARACTERISTICS:** Tp = 25° C (Note 1)

| SYMBOL | CHARACTERISTIC | RANGE | | | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| $V_{DD}$ | Output Amplifier Drain Supply Voltage | 16.0 | 17.0 | 18.0 | V | |
| $V_{RD\ (A+B)}$ | Output Reset Drain Supply Voltages | 16.5 | 17.0 | 17.5 | V | |
| $V_{SINK}$ | Anti-Blooming Sink Voltage | 16.0 | 17.0 | 18.0 | V | |
| $V_{OG\ (A+B)}$ | Output DC Gate Voltages | 5.5 | 6.0 | 6.5 | V | |
| $TP_1$, $TP_2$ | | 0.0 | 0.0 | 0.5 | V | |
| $TP_3$ | | 16.0 | 17.0 | 18.0 | V | |
| $V_{SG}$ | Amplifier Signal Ground | 0.0 | 0.0 | 0.5 | V | |
| $V_{SS}$ | Substrate Bias | -2.0 | -1.0 | -0.0 | V | Note 2 |
| $V_{SSN}$ | | 0.0 | $V_{SG}$ | 5.0 | V | Note 14 |
| $V_{SSP}$ | | -3.0 | -1.0 | 0.0 | V | |
| $I_{DD}$ | Output Amplifier Drain Supply Current | 6.0 | 10.0 | 15.0 | mA | |

**CLOCK CHARACTERISTICS:** Tp = 25° C

| SYMBOL | CHARACTERISTIC | RANGE | | | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| $V_{\phi X\ HIGH}$ | Transfer Clock HIGH | 14.5 | 15.0 | 15.5 | V | Note 3 |
| $V_{\phi 1\ HIGH\ (A+B)}$ $V_{\phi 2\ HIGH\ (A+B)}$ | Transport Clock HIGH | 7.5 | 8.0 | 8.5 | V | Note 3 |
| $V_{\phi PG\ HIGH\ (A+B)}$ | Photogate Clock HIGH | 8.0 | 10.0 | 12.0 | V | Note 3, 11 |
| $V_{\phi PG\ LOW\ (A+B)}$ | Photogate Clock LOW | 0.0 | 2.0 | 2.5 | V | Note 3 |
| $V_{\phi OG\ HIGH\ (A+B)}$ | Output Clock Gate HIGH | 7.5 | 8.0 | 8.5 | V | Note 3 |
| $V_{\phi R\ HIGH\ (A+B)}$ | Reset Clock HIGH | 14.5 | 15.0 | 15.5 | V | Note 3 |
| $V_{\phi IC\ HIGH}$ | Integration Control Clock HIGH | 14.5 | 15.0 | 15.5 | V | Note 3 |
| $V_{\phi IC\ LOW}$ | Integration Control Clock LOW | 0.0 | 0.3 | 0.7 | V | Notes 2, 3, 13 |
| $V_{\phi X\ LOW}$ | Transfer Clock LOW | 0.0 | 0.3 | 0.7 | V | Notes 2, 3 |
| $V_{\phi 1\ LOW\ (A+B)}$ | Transport Clock LOW | 0.0 | 0.3 | 0.7 | V | Notes 2, 3 |
| $V_{\phi 2\ LOW\ (A+B)}$ | Transport Clock LOW | 0.0 | 0.3 | 0.7 | V | Notes 2, 3 |
| $V_{\phi R\ LOW\ (A+B)}$ | Reset Clock LOW | 0.0 | 0.3 | 0.7 | V | Notes 2, 3 |
| $V_{\phi OG\ LOW\ (A+B)}$ | Output Clock Gate LOW | 0.0 | 0.3 | 0.7 | V | Notes 2, 3 |
| $f_{data}$ max | Maximum Output Data Rate | 2.0 | 5.0 | 10.0 | MHz | |

**AC CHARACTERISTICS:** Tp = 25° C (Note 1), $f_{data}$=2.0 MHz, $t_{int}$=1ms, Light Source = 2854° K + 2.0mm thick Schott BG-38 and OCLI WBHM Filters (Note 4).

| SYMBOL | CHARACTERISTIC | RANGE | | | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| DR | Dynamic Range<br>Relative to peak-to-peak noise<br>Relative to rms noise | | <br>2000:1<br>11000:1 | | | |
| NEE | RMS Noise<br>Equivalent exposure | | <br>$3.0 \times 10^{-6}$ | | <br>$\mu J/cm^2$ | |
| CTE | Charge Transfer Efficiency | .99999 | .99999 | | | Note 6 |
| $V_O$ | Output DC Level | 6.0 | 8.0 | 12.0 | V | |
| Z | Output Impedance | | 1 | | kΩ | |
| P<br>N | On-Chip Amplifier Power Dissipation<br>Peak-to-Peak Temporal Noise | | 150<br>1.0 | 300 | mW<br>mV | |

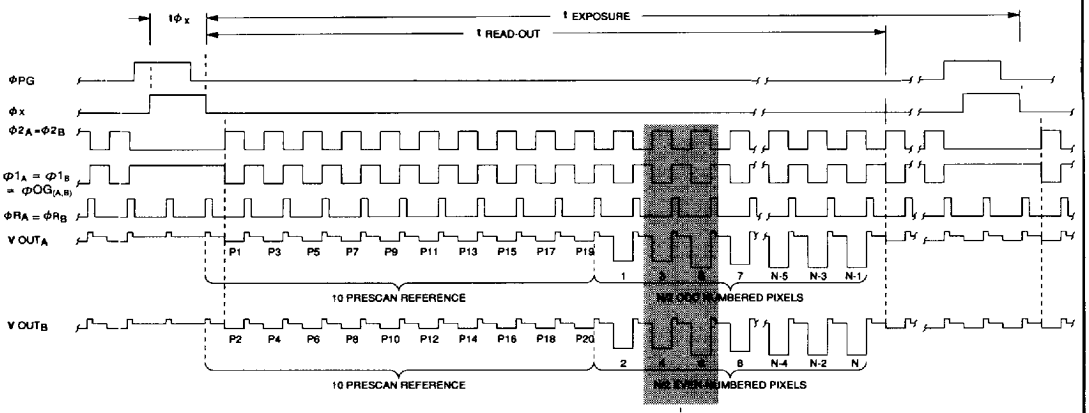
**PERFORMANCE CHARACTERISTICS:** Tp = 25° C (Note 1), $f_{data}$=2.0 MHz, $t_{int}$=1ms, Light Source = 2854° K + 2.0mm thick Schott BG-38 and OCLI WBHM Filters (Note 4).

| SYMBOL | CHARACTERISTIC | RANGE | | | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| PRNU* | Photoresponse Non-uniformity<br>Peak-to-peak<br>Peak-to-peak Positive or Impulses | | <br>90<br>55 | <br>240<br>110 | <br>mV<br>mV | |
| M Video | Video Mismatch | | 75 | 225 | mV | Note 7 |
| M DC | DC Mismatch | | 0.5 | 2.0 | V | Note 8 |
| DS | Dark Signal<br>DC Component<br>Low Frequency Component | | <br>5<br>5 | <br>15<br>15 | <br>mV<br>mV | Notes 9, 10 |
| SPDSNU | Single Pixel DS Non-Uniformity | | 5 | 15 | mV | Note 10 |
| R | Responsivity | 2.5 | 5.0 | 9.0 | $V/\mu Jcm^2$ | |
| $V_{SAT}$ | Saturation Output Voltage | 1.5 | 2.5 | 4.5 | V | |

* All PRNU measurements are taken at approximately 80% of $V_{SAT}$ using an f/5.0 lens and exclude the outputs from the first and last elements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU. The above characteristics are based on a 1200mV output (approximately 80% of the minimum $V_{SAT}$).

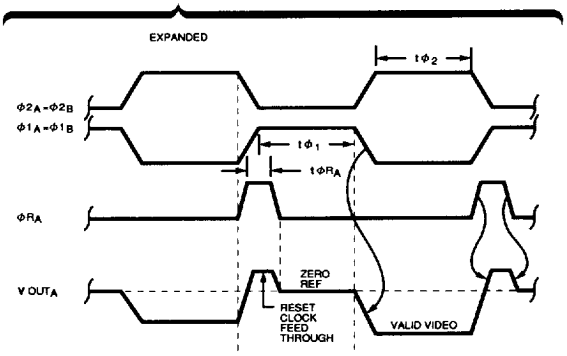
NOTES:
1. $T_P$ is defined as the package temperature measured on a copper block in good thermal contact with the entire backside of the device.
2. Negative transients on any clock pin going below 0.0 volts may cause charge injection, which results in an increase in apparent DS. Adjusting $V_{SSN}$ to a more negative voltage than the clock low voltages will reduce charge injection, if present.
3. $C_{\phi XA} = C_{\phi XB} = C_{\phi ICA} = C_{\phi ICB} = 450pF$; $C_{\phi 1A} = C_{\phi 1B} = C_{\phi 2A} = C_{\phi 2B} = 800pF$; $C_{\phi RA} = C_{\phi RB} = C_{\phi OGA} = C_{\phi OGB} = 5pF$.
4. OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror.
5. The minimum clock frequency is limited by increases in dark signal.
6. CTE is the measurement for a one-stage transfer.
7. Video mismatch is the difference in AC amplitudes between $V_{OUT}$ A and $V_{OUT}$ B under uniform illumination. It can be eliminated by attenuation/amplification of one of the video inputs.
8. DC mismatch is the difference in DC output level $V_O$) between $V_{OUT}$ A and $V_{OUT}$ B.
9. Dark signal component approximately doubles for every 5° to 15° increase in $T_P$.
10. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 5° to 15° increase in $T_P$.
11. The HIGH level of the Photogate Clock can actually be as high as 18V. However, increasing the high level of this clock may also increase the photosite dark signal.
12. Metal back plate electrically tied to $V_{SSN}$.
13. See "Anti-Blooming" and "Integration Control" under "Functional Description" for additional information; also see Application Note.
14. $V_{SSN}$ is normally tied to $V_{SG}$.

## TIMING DIAGRAM

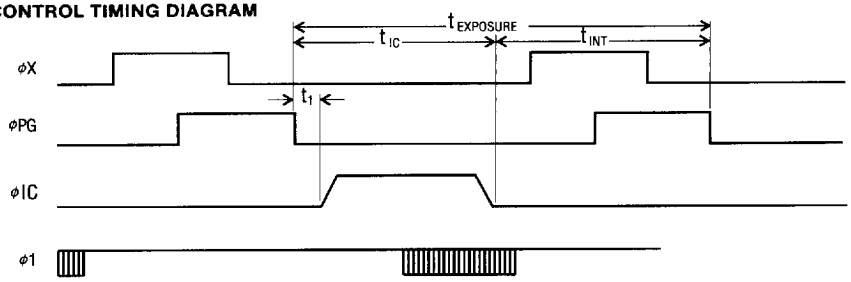



NOTES:

1. Timing requirements for $\phi_1$ and $\phi_2$:
   a. 50 ± 10% duty cycle, ~180° out of phase (See 1b).
   b. $\phi_{OG}$ and $\phi_2$ clocks must cross at ≥4V on the falling edge of $\phi_2$. (Both $\phi_{OG}$ and $\phi_2$ must not be <4V simultaneously.)
   c. 20ns ≤ ($t_{rise}$ = $t_{fall}$) ≤ 100ns
2. Timing requirements for $\phi R_A$ and $\phi R_{2B}$:
   a. 20ns ≤ ($t_{rise}$ = $t_{fall}$) < (0.3·$t\phi_R$)
   b. 30ns < ($t\phi R_A$ = $t\phi R_B$) < $t\phi_2$
   c. $t_{fall}$ time of $\phi R_A$ must not overlap $t_{fall}$ of $\phi OG_A$
   d. $t_{fall}$ time of $\phi R_B$ must not overlap $t_{fall}$ of $\phi OG_B$
3. Integration Control Clock ($\phi IC$) has been omitted from these timing diagrams for clarity. See "Integration Control Timing" diagram
4. Timing requirements for $\phi_X$:
   a. $t\phi_X$ ≥10μs
   b. $t_{rise}$ and $t_{fall}$ times of $\phi_X$ must not overlap $t_{rise}$ or $t_{fall}$ times of $\phi_1$ or $\phi_2$.




## INTEGRATION CONTROL TIMING DIAGRAM

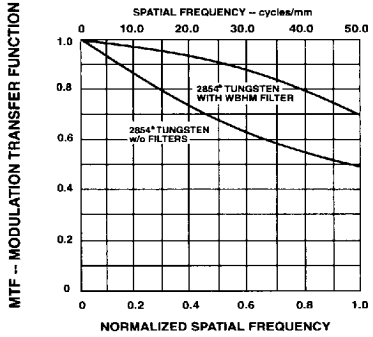



NOTES:

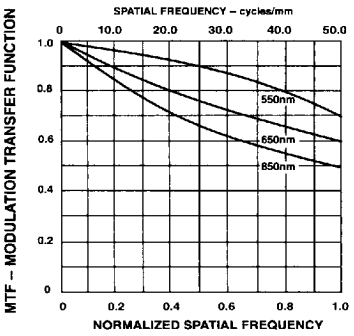
1. $t_1$ > ($t_{fall}$ of $\phi X$).
2. All charge generated in photosites during $t_{IC}$ is dumped in $V_{SINK}$.
3. All charge generated in photosites < $Q_{SAT}$ during $t_{INT}$ is transferred into the shift registers during $\phi x$ clock-high period. Photosite charge > $Q_{SAT}$ (shift reg.) generated during $t_{INT}$ goes into $V_{SINK}$ if anti-blooming voltage is optimized.
4. $\phi IC$ clock-low = 1 to 3 volts will give best anti-blooming operation.
5. $\phi IC$ $t_{rise}$ & $t_{fall}$ > 4μs to minimize clock coupling of $\phi IC$, into $V_{OUT}$.
6. To eliminate integration control, but retain anti-blooming $\phi IC$ = +2VDC.
7. To eliminate both integration control and anti-blooming, $\phi IC$ = 0VDC or $V_{SS}$(-1V).
8. To use integration control without anti-blooming, use $\phi IC$ clock-low = 0.0 to 0.7 volts and $\phi IC$ clock-high = same range as $\phi X$ clock-high voltage.
9. See Application Note "Inverted Photogate" for best low-light charge transfer

## TYPICAL PERFORMANCE CURVES

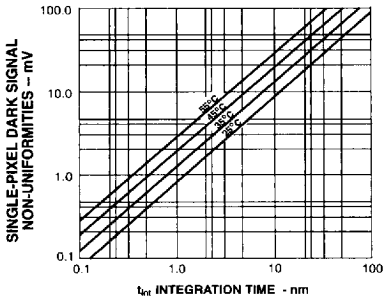
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



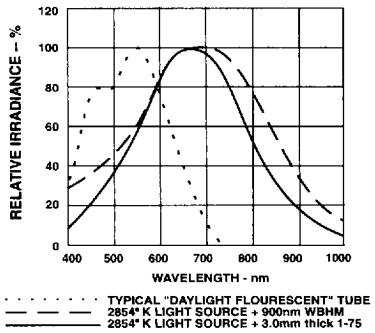

MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



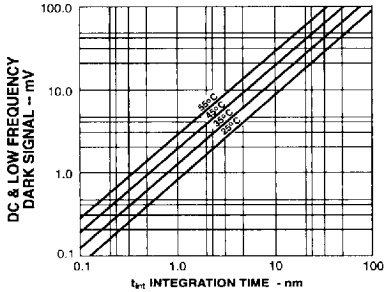

SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VS INTEGRATION TIME



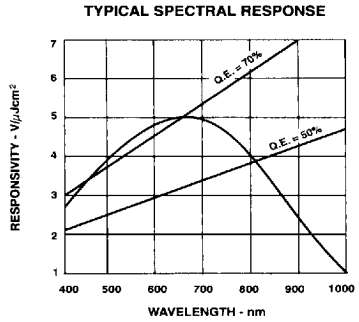

RELATIVE RADIANT FLUX VS WAVELENGTH



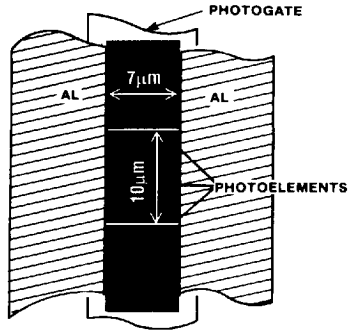

DC AND LOW-FREQUENCY DARK SIGNAL VS INTEGRATION TIME



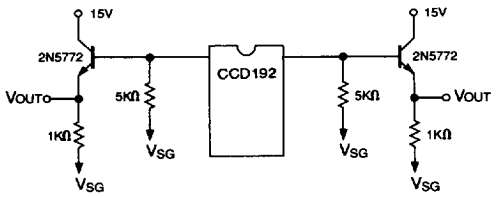

TYPICAL SPECTRAL RESPONSE



PHOTOELEMENT DIMENSIONS

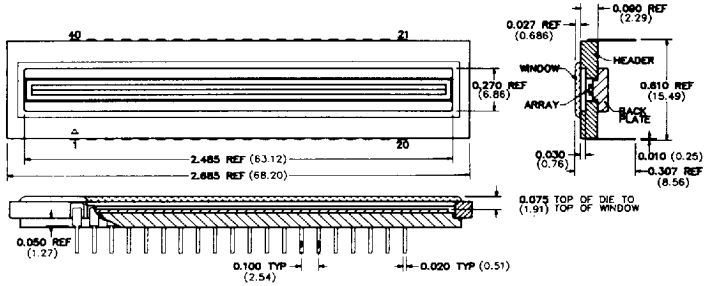



TEST LOAD CONFIGURATION

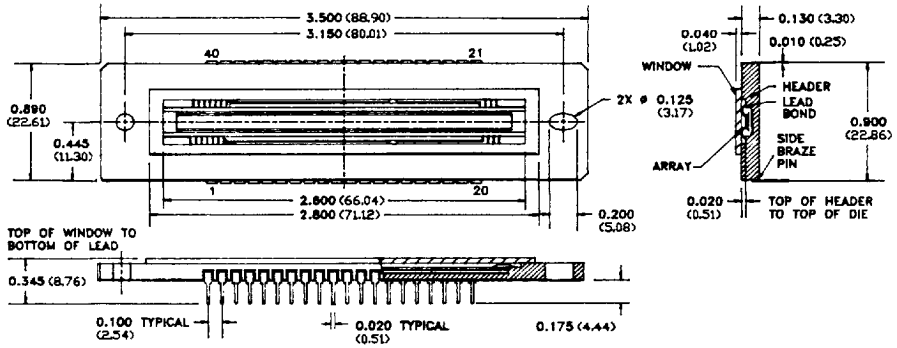



PACKAGE OUTLINE

CCD192DC




CCD192FDC




## DEVICE CARE AND OPERATION

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with de-ionized water. Allow the glass to dry preferably by blowing with filtered dry $N_2$ or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal DC and low frequency components approximately double for every 5° C temperature increase and single-pixel dark signal non-uniformities approximately double for every 12° C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

## ORDER INFORMATION

Order CCD192FDC where "F" stands for special flatness, "D" stands for ceramic package and "C" stands for commercial temperature range. Order CCD192DC for the standard package.

LORAL
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