Preliminary Data Sheet
July 1995

AT&T Microelectronics

DSP1605
Digital Signal Processor

1 Features

- For 5 V operation:
  - — 25 ns instruction cycle time (40 MIPS)
  - — 30 ns instruction cycle time (33 MIPS)
- For 3.3 V operation:
  - — 31.25 ns instruction cycle time (32 MIPS)
- Power-savings features:
  - — Low-power 0.6 µm CMOS technology; fully static design
  - — Active power: 9.5 mW/MIPS at 5.0 V
    3.8 mW/MIPS at 3.3 V
  - — Low-power standby: 3.0 mW at 5.0 V
    0.4 mW at 3.3 V
- 16 Kwords internal ROM
- 1 Kword internal RAM
- 16 x 16-bit multiplication and 36-bit accumulation in one instruction cycle
- Two 36-bit accumulators
- Instruction cache for high-speed, program-efficient, zero-overhead looping
- One external vectored interrupt
- Two 64 Kword address spaces with software wait-states for external accesses
- Single- or dual-channel 20 Mbits/s serial I/O port; 8-bit, 16-bit, 32-bit, and 48-bit data channel
- One 8-bit I/O port for flexible status or control pins
- External DRAM interface
- Two interrupt timers
- 68-pin PLCC or 80-pin MQFP package
- High- and low-frequency clock inputs
- Parallel host interface for rapid transfer of data with external devices
- Internal power-loss detection unit
- Object code upward compatible with DSP1600 Digital Signal Processor family
- Supported by DSP160X-ST Support Tools
- Full-speed in-circuit emulation HDS (HD-supported) Flash ROM device

2 Description

The DSP1605 is a 16-bit fixed-point digital signal processor (DSP) based on the DSP1600 core. It is programmable to perform a wide variety of fixed-point signal processing functions. A member of the DSP160X family, the DSP1605 includes a mix of peripherals specifically intended to support processing-intensive but cost-sensitive applications. In addition to the core, the DSP1605 consists of the following peripheral blocks: external memory interface unit (EMI), serial I/O unit (SIO), an 8-bit I/O port (IOP), two timer units, a parallel host interface (PHIF), and a JTAG interface; as well as one Kword of RAM and 16 Kwords of ROM. The DSP1605 is part of a low-cost, high-performance solution for consumer product applications.

The DSP1605 is available in the following packages:

- 68-pin PLCC (See Figure 1 on page 9.)
- 80-pin MQFP (See Figure 2 on page 10.)

The DSP achieves high throughput without programming restrictions or latencies due to its parallel pipelined architecture. The processor has an arithmetic unit capable of a 16 x 16 multiplication and 36-bit accumulation, or a 32-bit ALU operation in one instruction cycle. Data is accessed from memory via two independent addressing units.

A fully static, low-power, 0.6 µm CMOS design and a low-power standby mode support power-sensitive equipment applications. Two sets of pins allow the use of high-frequency and low-frequency clocks. Under program control, the DSP1605 can be switched between the high-frequency and low-frequency clock inputs. When switched to the low-frequency clock, the power is reduced.

The *FlashDSP*™ device is the development platform for the DSP1605. To support full-speed in-circuit emulation, the *FlashDSP* device includes an internal HDS module.

Table of Contents

Contents

Page

Table of Contents (continued)

Contents

Page

Table of Contents (continued)

Contents **Page**

List of Figures

Page

List of Tables

Page

List of Tables (continued)

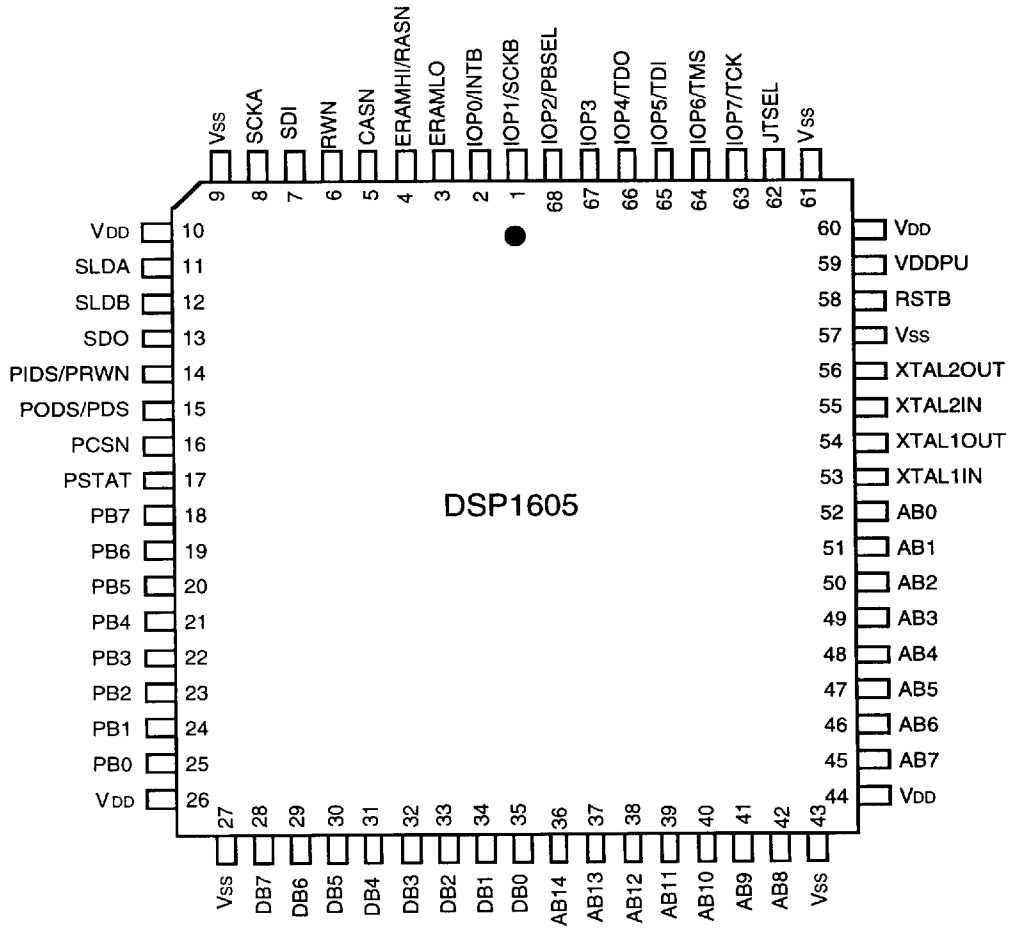
Page

List of Tables (continued)

Page

3 Pin Information

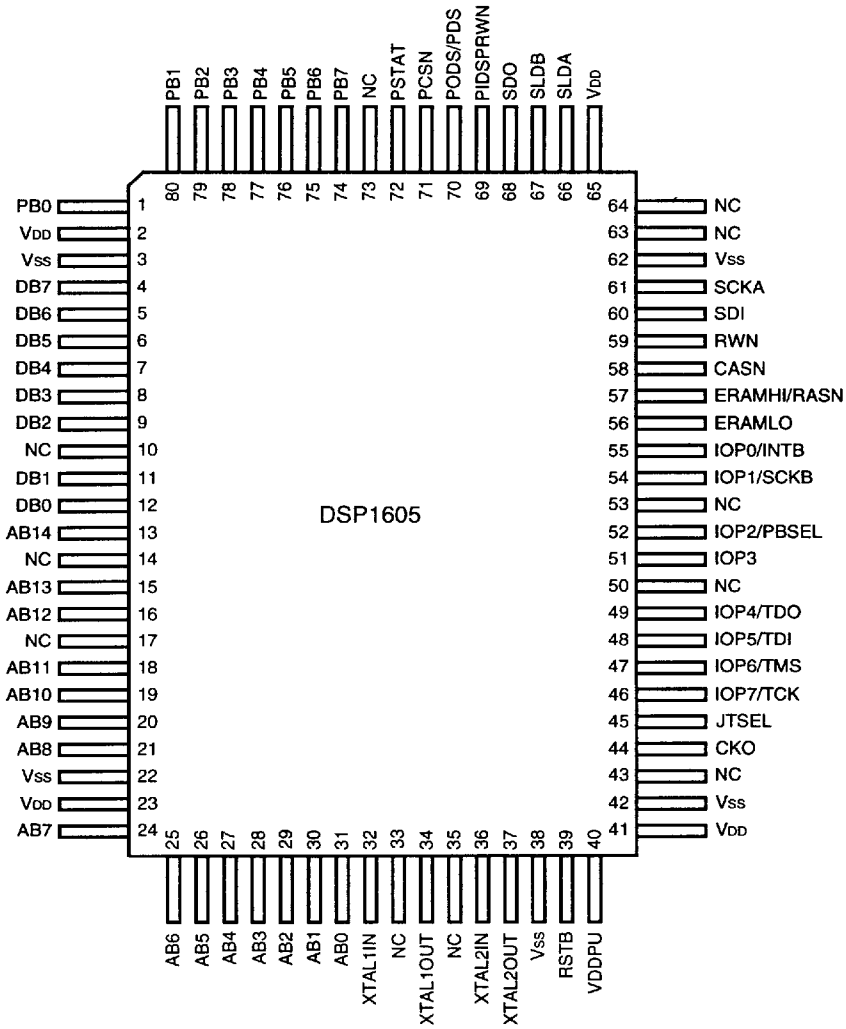
The device is packaged in either a 68-pin PLCC (see Figure 1) or an 80-pin MQFP (see Figure 2).



5-3980(C)

Figure 1. DSP1605 68-Pin PLCC Pin Diagram

3 Pin Information (continued)



5-3995(C)

Figure 2. DSP1605 80-Pin MQFP Diagram

3 Pin Information (continued)

Figure 3 shows DSP1605 pins organized into their seven functional groups. Tables 1 and 2 and Sections 3.1 through 3.7 describe these pins.

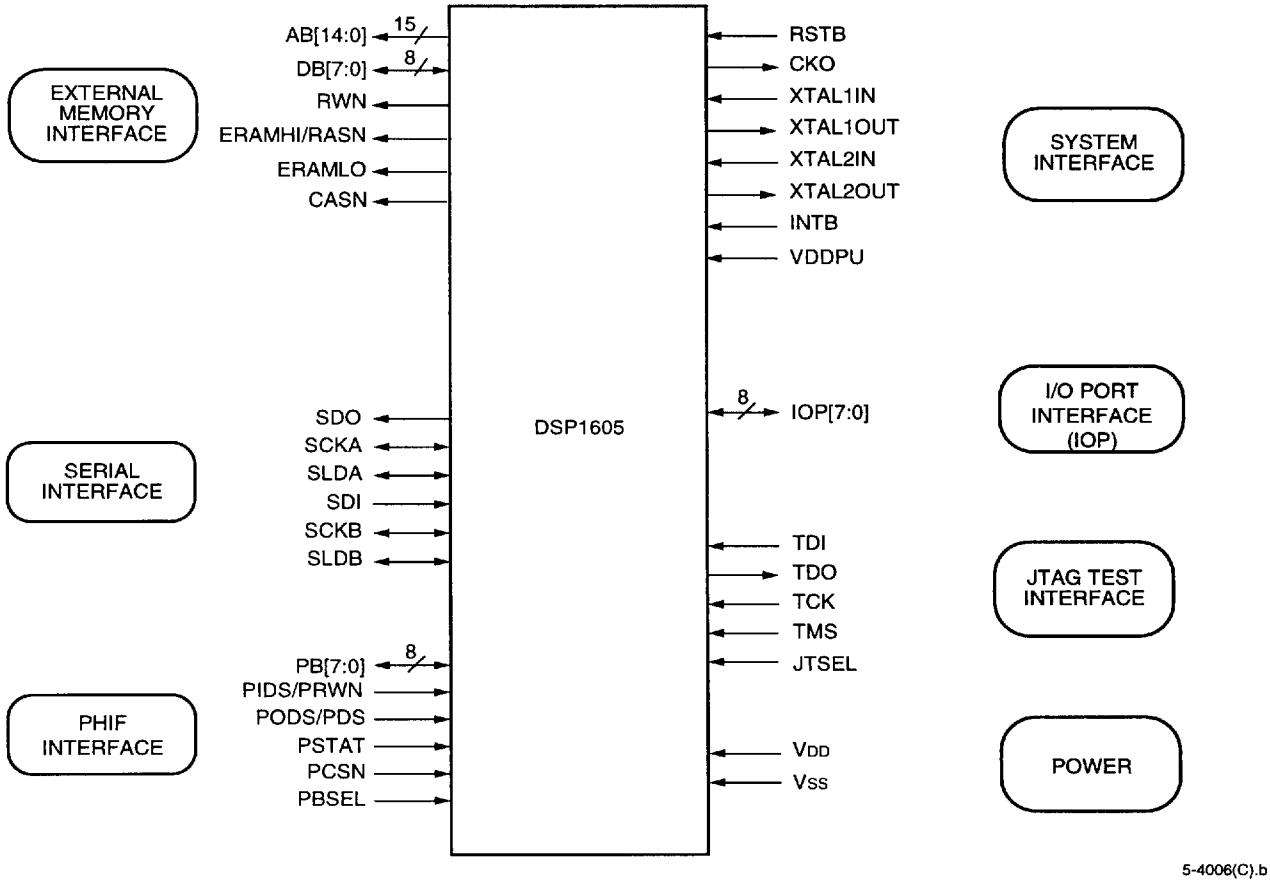


Figure 3. DSP1605 Pinout by Group

Note: The CKO pin is available only on the 68-pin PLCC.

3 Pin Information (continued)

For each DSP1605 pin listed in Table 1:

- Each entry in the Type column is one of the following:
  - —I (input)
  - —I/O (input/output)
  - —O (output)
  - —TO (tristate output)
- Each entry in the Active column is one of the following:
  - —High
  - —Low
  - —Pgm (programmable polarity)
  - —Neg (negative edge triggered)

Table 1. DSP1605 Pinout

Symbol	Pin Number		Type	Active	Pin Description
	68-Pin PLCC	80-Pin MQFP			
AB14	36	13	O	High	15-bit external memory address bus, bits 14—0.
AB[13:12]	37—38	15—16			
AB[11:8]	39—42	18—21			
AB[7:0]	45—52	24—31			
CASN	5	58	O	Low	Column address select.
CKO	—	44	O	High	Processor clock. (The 68-pin PLCC has no CKO pin.)
DB[7:2]	28—33	4—9	I/O	High	8-bit external memory data bus. Each of these pins has an internal pull-down resistor that is typically 68 kΩ.
DB[1:0]	34—35	11—12			
ERAMHI/ RASN	4	57	O	Low	External RAM, high select, or row address select.
ERAMLO	3	56	O	Low	External RAM, low select.
IOP7/TCK	63	46	I/O	Pgm/ —	I/O port bit 7, multiplexed with TCK (JTAG test clock).
IOP6/TMS	64	47	I/O	Pgm/ High	I/O port bit 6, multiplexed with TMS (JTAG test mode select).
IOP5/TDI	65	48	I/O	Pgm/ High	I/O port bit 5, multiplexed with TDI (JTAG test data in).
IOP4/TDO	66	49	I/O	Pgm/ High	I/O port bit 4, multiplexed with TDO (JTAG test data out).
IOP3	67	51	I/O	Pgm	I/O port bit 3.
IOP2/PBSEL	68	52	I/O	Pgm/ High	I/O port bit 2, multiplexed with PBSEL (PHIF byte select).
IOP1/SCKB	1	54	I/O	Pgm	I/O port bit 1, multiplexed with SCKB [serial clock channel B (dual-channel mode), or serial input clock (single-channel mode)].
IOP0/INTB	2	55	I/O	Pgm/ Neg	I/O port bit 0, multiplexed with INTB (external interrupt, negative edge triggered).
JTSEL	62	45	I	High	JTAG select input.
PB[7:0]	18—25	74—80	I/O	High	8-bit parallel data bus.

3 Pin Information (continued)

Table 1. DSP1605 Pinout (continued)

Symbol	Pin Number		Type	Active	Pin Description
	68-Pin PLCC	80-Pin MQFP			
PCSN	16	71	I	Low	Parallel device enable strobe.
PIDS/PWRN	14	69	I	Low	Parallel input data strobe, or parallel read/write.
PODS/PDS	15	70	I	Low	Parallel output data strobe, or parallel data strobe.
PSTAT	17	72	I	High	PHIF status.
RSTB	58	39	I/O	Low	Reset.
RWN	6	59	O	—	Read/write not.
SCKA	8	61	I/O	—	Serial clock channel A (dual-channel mode), or serial output clock (single-channel mode).
SDI	7	60	I	High	Serial data in.
SDO	13	68	TO	High	Serial data out.
SLDA	11	66	I/O	Pgm	Serial load channel A (dual-channel mode), or serial output load (single-channel mode).
SLDB	12	67	I/O	Pgm	Serial load channel B (dual-channel mode), or serial input load (single-channel mode).
VDDPU	59	40	I	High	V_{DD} powerup.
XTAL1IN	53	32	I	—	High-frequency crystal in.
XTAL1OUT	54	34	O	—	High-frequency crystal out.
XTAL2IN	55	36	I	—	Low-frequency crystal in.
XTAL2OUT	56	37	O	—	Low-frequency crystal out.

Table 2. DSP1605 Power Supply, Ground, and Unconnected Pins

Symbol	Pin Number		Pin Description
	68-Pin PLCC	80-Pin MQFP	
V_{DD}	10, 26, 44, and 60	2, 23, 41, and 65	5 V or 3.3 V power supply.
V_{SS}	9, 27, 43, 57, and 61	3, 22, 38, 42, and 62	Ground.
NC	—	10, 14, 17, 33, 35, and 43	No connection.

3 Pin Information (continued)

3.1 System Interface

This section describes the system interface pins on the DSP1605.

3.1.1 XTAL1IN, XTAL1OUT

High-Frequency Crystal Oscillator. Input/Output. The 1x crystal oscillator for high-frequency clocks. XTAL1IN is the input node for the oscillator amplifier. XTAL1OUT is the output node for the oscillator amplifier. If the high-frequency clock is selected (see the **ioc** register, Table 33, on page 54), this clock determines the DSP1605 instruction cycle time. For more information, see Section 9.1, High-Frequency Crystal Oscillator, on page 108.

3.1.2 XTAL2IN, XTAL2OUT

Low-Frequency Crystal Oscillator. Input/Output. The 1x crystal oscillator generates the low-frequency clock, which typically generates the internal clock when the DSP is in low-power standby mode. XTAL2IN is the input node for the oscillator amplifier. XTAL2OUT is the output node for the oscillator amplifier. If the low-frequency clock is selected (see the **ioc** register, Table 33, on page 54), this clock provides DRAM refresh, determines the DSP1605 instruction cycle time, and drives TIMER1. For more information, see Section 9.2, Low-Frequency Crystal Oscillator or Resonator, on page 112.

3.1.3 CKO

Clock Out. (Only on 80-pin MQFP package.) Output clock or single-bit data output. CKO is selectable through programming the **ioc** register (see Table 33 on page 54). The following options are selectable: a free-running clock, a wait-stated clock, a logic 0, or a logic 1. If used as a single-bit output, this pin initializes to a free-running clock after reset.

3.1.4 RSTB

Reset. Bidirectional (Schmitt trigger). Negative Assertion. A high-to-low transition on RSTB causes the DSP1605 to enter the reset state. Upon deassertion, the DSP begins execution from location 0x0000. This input contains a Schmitt trigger providing a hysteresis between positive- and negative-going transitions.

Note: This pin is internally tied to the open-drain output of the power-loss detect circuit. To indicate a reset, a power-loss detect condition forces this pin low.

3.1.5 INTB

Interrupt. Input (Schmitt trigger). Negative Edge-Triggered. External interrupt to the DSP1605. This input contains a Schmitt trigger providing a hysteresis between positive- and negative-going transitions. An interrupt is posted when a negative-going transition is detected. Note that there is no interrupt acknowledge pin. External hardware must guarantee that the interrupt service routine has completed before issuing another interrupt on INTB. Any activity on INTB is not recognized during the interrupt service routine.

Note: This pin is multiplexed with IOP0 (see Section 3.4, I/O Port (IOP[7:0])).

3.1.6 VDDPU

V_{DD} Powerup. Input. This pin should be connected to V_{DD} to enable the internal power-loss detect circuit. To disable, this pin should be pulled low.

3 Pin Information (continued)

3.2 External Memory Interface

3.2.1 AB[14:0]

Address Bus. Output. Address bus for read or write transactions to external memory.

3.2.2 DB[7:0]

Data Bus. Bidirectional. Data bus for read or write transactions to external memory or I/O. Each pin has an internal pull-down resistor that is typically 68 kΩ.

3.2.3 ERAMLO

External RAM Lo Select. Output. Negative assertion. Asserted when the ERAMLO segment in the Y memory space is accessed. The leading edge of ERAMLO may be programmed to be delayed by one half of an instruction cycle.

3.2.4 ERAMHI/RASN

External RAM Hi Select/Row Address Select. Output. Negative assertion. The function of this pin depends on whether the DRAM controller is enabled in the **ioc** register. If the DRAM controller is enabled, this pin functions as RASN. Along with its assertion, the row address is driven on the AB pins. If the DRAM controller is not enabled, this pin functions as ERAMHI and is asserted when the ERAMHI segment in the Y memory (data) space is accessed. The leading edge of ERAMHI may be programmed to be delayed by one half of an instruction cycle.

3.2.5 CASN

Column Address Select. Output. Negative assertion. Asserted when the ERAMHI segment in the Y address space is accessed. Along with its assertion, the column address is driven on the AB pins.

3.2.6 RWN

Read/Write Not. Output. When a logic 1, a read access is in progress; when a logic 0, a write access is in progress.

3.3 Serial Interface (SIO)

The SIO is configurable for either single-channel or dual-channel mode, selectable by the **sioc** register. The SIO pins perform different functions depending on whether the single-channel or dual-channel mode is selected. In the descriptions below, both functions are described for each pin. For more information about the **sioc** register, see Table 43 on page 59. For the **sioce** register, see Table 44 on page 60.

3.3.1 SDI in Single-Channel Mode

Serial Data Input. Input. Serial input data latched on the falling edge of SCKB, either LSB or MSB first, according to the **sioc** register MSB field.

3.3.2 SDI in Dual-Channel Mode

Serial Data Input. Input. Channel A serial input data is latched on the falling edge of SCKA, and channel B serial input data is latched on the falling edge of SCKB. The data is either LSB or MSB first, according to the **sioc** register MSB field.

3.3.3 SCKB Multiplexed

This pin is multiplexed with IOP1 (see Section 3.4, I/O Port (IOP[7:0])). This multiplexed signal is selected by the UENHSIO bit of the **ioc** register (see Table 33 on page 54). If the UENHSIO bit is cleared to zero, SCKB is internally tied to SCKA.

3.3.4 SCKB in Single-Channel Mode

Input Clock (ICK). Bidirectional. Clock for serial input data. In active mode, SCKB is an output; in passive mode, SCKB is an input, according to the **sioc** register ICK field.

3.3.5 SCKB in Dual-Channel Mode

Serial Clock B. Bidirectional. Channel B clock for serial input data and for serial output data. In active mode, SCKB is an output; in passive mode, SCKB is an input, according to the **sioc** register ICK field.

3 Pin Information (continued)

3.3 Serial Interface (SIO) (continued)

3.3.6 SLDB in Single-Channel Mode

Input Load (ILD). Bidirectional. The strobe for loading the input buffer **sdx<0—1>**_i from the input shift register. The assertion of SLDB indicates the beginning of a serial input word. In active mode, SLDB is an output. In passive mode, SLDB is an input and should only be asserted once per serial input word. Passive or active mode is set through the **sioc** register ILD field. The assertion level of SLDB is selectable through the **sioce** register ILDH field, and the duty cycle for the active SLDB is selectable through the **sioce** register ILDP field.

3.3.7 SLDB in Dual-Channel Mode

Serial Load B. Bidirectional. The strobe for channel B for loading the input buffer **sdx<0—1>**_i from the input shift register and for loading the output shift register from the output buffer **sdx<0—2>**_o. The assertion of SLDB indicates the beginning of a channel B serial input word and the beginning of a channel B serial output word. In active mode, SLDB is an output. In passive mode, SLDB is an input and should only be asserted once per serial input word. Passive or active mode is set through the **sioc** register ILD field. The assertion level of SLDB is selectable through the **sioce** register ILDH field, and the duty cycle for the active SLDB is selectable through the **sioce** register ILDP field.

3.3.8 SDO in Single-Channel Mode

Serial Data Output. Output. Serial output data is clocked out on the rising edge of SCKA and may be configured to be least significant bit (LSB) first or most significant bit (MSB) first through the MSB bit of the **sioc** register.

3.3.9 SDO in Dual-Channel Mode

Serial Data Output. Output. Serial output data for channel A is clocked out on the rising edge of SCKA, and serial output data for channel B is clocked out on the rising edge of SCKB. Data may be configured to be least significant bit (LSB) first or most significant bit (MSB) first through the MSB bit of the **sioc** register.

3.3.10 SCKA in Single-Channel Mode

Output Clock (OCK). Bidirectional. Clock for serial output data. In active mode, SCKA is an output; in passive mode, SCKA is an input, according to the **sioc** register OCK field.

3.3.11 SCKA in Dual-Channel Mode

Serial Clock A. Bidirectional. Channel A clock for serial input data and serial output data. In active mode, SCKA is an output; in passive mode, SCKA is an input, according to the **sioc** register OCK field.

3.3.12 SLDA in Single-Channel Mode

Output Load (OLD). Bidirectional. The strobe for loading the output shift register from the output buffer **sdx<0—2>**_o. The assertion of SLDA indicates the beginning of a serial output word. In active mode, SLDA is an output. In passive mode, SLDA is an input and should only be asserted once per serial output word. Passive or active mode is set through the **sioc** register OLD field. The assertion level of SLDA is selectable through the **sioce** register OLDH field, and the duty cycle for the active SLDA is selectable through the **sioce** register OLDP field.

3.3.13 SLDA in Dual-Channel Mode

Serial Load A. Bidirectional. The strobe for channel A for loading the input buffer **sdx<0—1>**_i from the input shift register and for loading the output shift register from the output buffer **sdx<0—2>**_o. The assertion of SLDA indicates the beginning of a channel A serial input word and the beginning of a channel A serial output word. In active mode, SLDA is an output. In passive mode, SLDA is an input and should only be asserted once per serial input word. Passive or active mode is set through the **sioc** register OLD field. The assertion level of SLDA is selectable through the **sioce** register OLDH field, and the duty cycle for the active SLDA is selectable through the **sioce** register OLDP field.

3.4 I/O Port (IOP[7:0])

I/O Port. Bidirectional. These pins can be individually configured to be inputs or outputs. As outputs, each bit may be set, cleared, or toggled under program control. As inputs, they may be read.

Note: As shown in Figure 1 on page 9, Figure 2 on page 10, and Table 1 on page 12, IOP[7:4] and IOP[2:0] are multiplexed with other functions.

3 Pin Information (continued)

3.5 PHIF

This section describes the PHIF pins on the DSP1605.

3.5.1 PCSN

Parallel Device Enable Strobe. Input. Negative assertion. When asserted, the PHIF registers may be read or written by the host processor.

3.5.2 PODS/PDS

Parallel Output Data Strobe/Parallel Data Strobe. Input. This pin is configurable by the DSP in software. When configured as PODS, it has a negative assertion level. When PODS is asserted along with PCSN, the PHIF output data register or the PHIF status register is read by the host processor. When configured as PDS, the assertion level of the pin (active-high or active-low) is also configurable by the DSP in software. When PDS is asserted along with PCSN, the level of the PRWN signal determines whether a read or a write transaction is performed by the host processor.

3.5.3 PIDS/PRWN

Parallel Input Data Strobe/Parallel Read/Write. Input. This pin is configurable by the DSP in software. When configured as PIDS, it has a negative assertion level. When PIDS is asserted along with PCSN, the PHIF input data register is written by the host processor. When configured as PRWN, the state of PRWN when PCSN and PDS are asserted determines whether the host processor performs a read (PRWN = 1) or a write (PRWN = 0).

3.5.4 PSTAT

PHIF Status. Input. A logic 0 on PSTAT during a write transaction selects the parallel input data register to be written; on a read transaction, the parallel output data register is read. A logic 1 on PSTAT during a read transaction selects the PHIF status register to be read.

3.5.5 PBSEL

PHIF Byte Select. Input. When the PHIF is configured for 16-bit transfers through the **phifc** register, PBSEL selects the byte available for access by the host. For more information, see Table 38, phifc Register PHIF Function (8-Bit and 16-Bit Modes), on page 56.

This pin is multiplexed with IOP2 (see Section 3.4, I/O Port (IOP[7:0])). This multiplexed signal is selected by bit 7 of the **phifc** register (see Table 37 on page 56). If bit 7 is cleared to 0, this pin functions as IOP2 and the internal PBSEL signal is tied to logic 0.

3.5.6 PB[7:0]

Parallel Data Bus. Bidirectional. On the host processor write transaction to the PHIF, the data written is placed on PB[7:0] by the host. On a host processor read transaction from the PHIF, the data being read is placed on PB[7:0] by the DSP1605.

3 Pin Information (continued)

3.6 JTAG Test Mode Interface

This section describes the JTAG pins on the DSP1605.

3.6.1 JTSEL

JTAG Select. Input. This pin controls the multiplexing of the four JTAG pins (TCK, TMS, TDI, and TDO) with pins IOP[7:4]. Set JTSEL high to select the JTAG pins. Set JTSEL low to select IOP[7:4]. (See Section 3.4, I/O Port (IOP[7:0]).

3.6.2 TCK

This pin is multiplexed with IOP7.

Test Clock. Input. JTAG serial shift clock that clocks data into TDI and out of TDO and controls the JTAG port by latching TMS into the state machine controller.

3.6.3 TMS

This pin is multiplexed with IOP6.

Test Mode Select. Input. JTAG mode control signal that controls the state of the JTAG controller. TMS is sampled on the rising edge of TCK.

3.6.4 TDI

This pin is multiplexed with IOP5.

Test Data Input. Input. JTAG serial input of all serial-scanned data and instructions that is sampled on the rising edge of TCK.

3.6.5 TDO

This pin is multiplexed with IOP4.

Test Data Output. Tristate Output. JTAG serial output of all serial-scanned data and status bits. TDO changes on the falling edge of TCK.

3.7 PWR/GND

This section describes the power and ground pins on the DSP1605.

3.7.1 V_{SS}

Ground. There are five ground pins.

3.7.2 V_{DD}

5.0 V or 3.3 V Supply. There are four power pins.

4 Hardware Architecture

The DSP1605 is a 16-bit fixed-point digital signal processor (DSP) that is generally upward object code compatible with the DSP1610, except for specific I/O configurations and peripherals. The DSP1605 consists of a DSP1600 core together with internal memory and peripherals.

To minimize pin count, the DSP1605 multiplexes the following package pins:

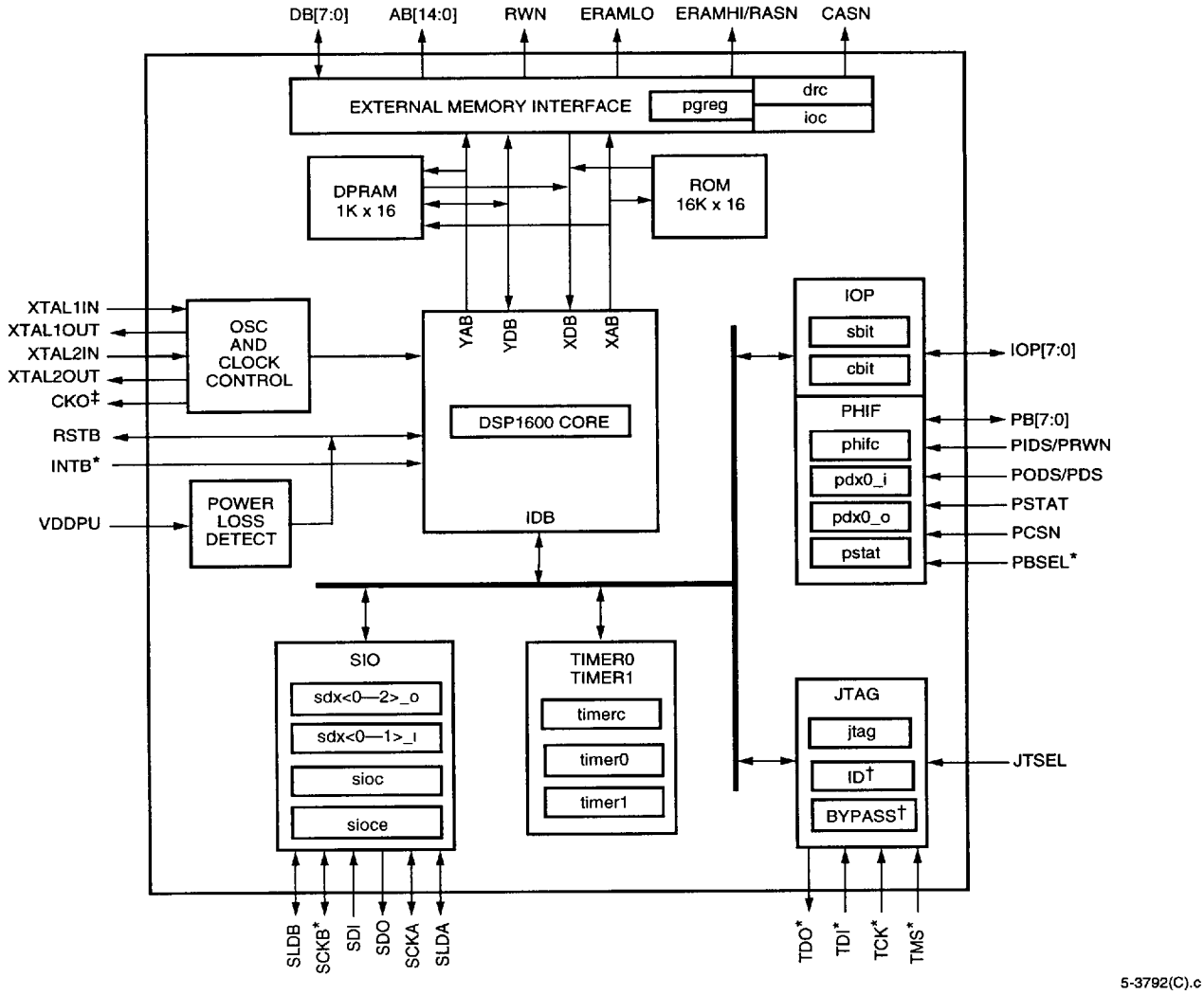
- IOP0 is multiplexed with INTB
- IOP1 is multiplexed with SCKB
- IOP2 is multiplexed with PBSEL
- IOP4 is multiplexed with TDO
- IOP5 is multiplexed with TDI
- IOP6 is multiplexed with TMS
- IOP7 is multiplexed with TCK

4.1 DSP1605 Architectural Overview

Figure 4 on page 20 shows a block diagram of the DSP1605, which consists of the modules described in Sections 4.1.1 through 4.1.9. Table 3 on page 21 shows a legend for the DSP1605 block diagram. Certain modules contain internal registers that are illustrated (not to scale) in Figure 4. The DSP has a pair of internal buses (address bus and data bus) for program/coefficient memory (X memory space) and a second independent pair of internal buses for data memory (Y memory space).

4 Hardware Architecture (continued)

4.1 DSP1605 Architectural Overview (continued)



* These pins are multiplexed with other pins.
† These registers are accessible through pins only.
‡ The CKO pin is available only on the 80-pin MQFP package.

Note: The registers whose names are shown in lower-case letters are accessible by the DSP software (some are also accessible externally through the pins). The registers whose names are shown in upper-case letters are accessible only through the DSP pins.

Figure 4. DSP1605 Block Diagram

4 Hardware Architecture (continued)

4.1 DSP1605 Architectural Overview (continued)

Table 3. DSP1605 Block Diagram Legend

Symbol	Name
BYPASS	JTAG bypass register
cbit	Control registers for IOP
drc	DRAM control register
ID	JTAG device identification register
IDB	Internal data bus
ioc	I/O configuration register
IOP	I/O port
jtag	16-bit serial/parallel register
OSC	Internal high- and low-frequency clock oscillators
pdx0_i	PHIF data register input buffer
pdx0_o	PHIF data register output buffer
pgreg	Page register for row address select
PHIF	Processor host interface
PSTAT	PHIF status register
phifc	PHIF control register
DPRAM	Internal RAM (1K x 16)
ROM	Internal ROM (16K x 16)
sbit	Status register for IOP
sdx<0—1>_i	Serial data transmit input registers
sdx<0—2>_o	Serial data transmit output registers
SIO	Serial I/O unit
sioc	Serial I/O control register
sioce	Serial I/O extended control register
TIMER<0,1>	Programmable timer units
timer<0,1>	Timer running count registers
timerc	Timer control register
XAB	X space (program space) address bus
XDB	X space data bus
YAB	Y space (data space) address bus
YDB	Y space data bus

4.1.1 DSP1600 Core

The DSP1600 core is the heart of the DSP1605. The core consists of a data arithmetic unit (DAU), two address arithmetic units (XAAU and YAAU), an instruction cache, and a control section. The core provides support for external memory wait-states and internal dual-port RAM, and features vectored interrupts and a trap mechanism. (For more information, see Section 4.2, DSP1600 Core Architectural Overview, on page 24.)

4 Hardware Architecture (continued)

4.1 DSP1605 Architectural Overview (continued)

4.1.2 Dual-Port RAM (DPRAM)

This module contains one bank of zero wait-state memory. It consists of 1K of 16-bit words and has separate address and data ports to the instruction/coefficient and data memory spaces. A program can reference memory from either space at any time, transparently and without restriction. The DSP1600 core automatically performs the required multiplexing. In the event that references to both ports of DPRAM are made simultaneously, the DSP1600 core automatically inserts a wait-state and performs the data port access first, followed by the instruction/coefficient port access. Because the DSP has only one 1-Kword bank, all simultaneous accesses from X and Y space result in an added wait-state. See also Section 4.4, Memory Maps and Wait-States.

A program can be downloaded from slow off-device memory into DPRAM and then be executed without wait-states. DPRAM is also useful for improving convolution performance in cases where the coefficients are adaptive. Because DPRAM can be downloaded through the JTAG port, full-speed remote in-circuit emulation is possible. DPRAM can also be used for downloading self-test code through the JTAG port.

4.1.3 Read-Only Memory (ROM)

The DSP1605 contains 16K of 16-bit words of zero wait-stated mask-programmable ROM for program and fixed coefficients. A mask-programmable secure option is available, which prohibits reading out the ROM contents externally. This is accomplished by prohibiting the selection of memory map 3.

4.1.4 External Memory Interface (EMI)

By connecting the DSP1605 to external memory and I/O devices, the EMI supports read and write operations from and to data memory (Y memory space). The DSP1600 core automatically controls the EMI. Instructions can transparently reference external memory from the internal data bus. Through the EMI, both SRAMs and DRAMs can be interfaced to the DSP. For more information, see Section 4.5, External Memory Interface (EMI) and Section 4.4, Memory Maps and Wait-States.

4.1.5 Timers

Two timers are provided in the DSP1605. They are used to provide an interrupt at the expiration of a programmed interval. The interrupt may be a single interrupt or a repetitive interrupt. TIMER0 has a clock prescaler and supports over nine orders of magnitude of interval selection. TIMER1 counts at the frequency of the low-frequency crystal, XTAL2, divided by four, and does not have a prescaler. The timers may be stopped and restarted at any time. For more information, see Section 4.8.

4.1.6 Input/Output Port (IOP)

One 8-bit IOP unit provides convenient and efficient monitoring and control of eight individually configurable pins. When configured as outputs, the pins can be individually set, cleared, toggled or left unchanged. When configured as inputs, the entire port can be read (those configured as inputs as well as those configured as outputs). Note that most of the pins are multiplexed with other functions. For detailed information about IOP operation, see Section 4.7, I/O Port (IOP).

4.1.7 JTAG

The JTAG section contains logic that implements the JTAG/*IEEE* * P1149.1 standard four-signal test port. No boundary-scan register is included. The JTAG port provides a mechanism for the DSP1600 core to communicate with remote test equipment or a remote hardware development system (DSP1600-HDS or *FlashDSP*1600-HDS). The JTAG port also supports program, memory, and register upload/download, and execution start/stop.

A 4-bit instruction register, a bypass register, and a device identification register have been implemented (see Table 34 on page 55). The JTAG instruction for accessing the ID register is 0xE (1110). The JTAG instruction for accessing the BYPASS register is 0xF (1111). Figure 4 on page 20 shows the ID and BYPASS registers. There is no separate TRST input pin.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

4 Hardware Architecture (continued)

4.1 DSP1605 Architectural Overview (continued)

4.1.8 Serial Input/Output Unit (SIO)

The SIO provides a serial interface to codecs and signal processors with few, if any, external devices. For example, the SIO port interfaces gluelessly to many industry-standard codecs, such as the AT&T T7513B and T7503. The high-speed, double-buffered port supports back-to-back transmissions.

Both passive mode, i.e., clock and load signals driven from an external source, and active mode, i.e., clock and load signals driven by the DSP, are supported. Output data transfers of 8, 16, 32, or 48 bits, and input data transfers of 8, 16, or 32 bits may be defined.

The SIO can be configured to operate in a dual-channel mode, in which data from two external serial devices are time-division multiplexed by sharing data in (SDI) and data out (SDO) pins. For more detail on the SIO, see Section 4.6, Serial I/O Unit (SIO).

4.1.9 Power-Loss Detect Circuit

The power-loss detect circuit is enabled by connecting the VDDPU pin to the power supply, V_{DD}. The output of the power-loss detect circuit is internally connected to the RSTB pin. If the supply voltage falls below the minimum required value, the bidirectional RSTB pin has an open-drain output that is pulled low. This causes an automatic device reset. The power-loss detect circuit is disabled by connecting the VDDPU pin to ground.

4.1.10 Oscillator and Clock Control

The DSP includes two internal oscillators that provide a high-frequency clock (XTAL1) and a low-frequency clock (XTAL2). The **ioc** register bit 12 (see Table 33 on page 54) determines which clock is selected to run the core and peripherals. The DSP instruction cycle time is determined by the period of the selected clock.

The power dissipation is reduced when XTAL2 is selected, and is further reduced if the XTAL1 oscillator is then disabled by setting bit 13 of the **ioc** register.

The DSP1605 80-pin MQFP package provides an output clock pin, CKO. As shown in Table 4, **ioc** register bits 10 and 11 select one of four CKO pin output functions.

Table 4. CKO Pin Output Functions

ioc Register		CKO Pin Output Function
Bit 11	Bit 10	
0	0	Free-running unstretched cycle clock.
0	1	Wait-stated clock. The high-to-low transition of the wait-stated clock is synchronized with the high-to-low transition of the free-running unstretched cycle clock.
1	0	Single-bit output held high.
1	1	Single-bit output held low. For maximum power savings, set bits 10 and 11 to 1 (by the setting the **ioc** register to 0x3C00) before setting the low-power standby mode. (For more information, see Section 4.3.5, Low-Power Standby Mode (AWAIT), on page 28.)

Note: Although the DSP1605 68-pin PLCC package does not provide a CKO pin, **ioc** register bits 10 and 11 must both still be set to 1 for minimum power consumption.

4.1.11 Parallel Host Interface (PHIF)

The PHIF is a passive, 8-bit parallel port that can interface to an 8-bit bus containing other AT&T DSPs, microprocessors, or peripheral I/O devices. The PHIF port supports either *Motorola** or *Intel*† protocols, as well as 8-bit or 16-bit transfers, configured in software. The port data rate depends upon the instruction cycle rate.

The PHIF is accessed in two basic modes: 8-bit or 16-bit mode. In 16-bit mode, the host determines an access of the high or low byte. In 8-bit mode, only the low byte is accessed. Software-programmable features allow for a glueless host interface to microprocessors. For more detail, see Section 4.9, Parallel Host Interface (PHIF).

* *Motorola* is a registered trademark of Motorola, Inc.
† *Intel* is a registered trademark of Intel Corporation.

4 Hardware Architecture (continued)

4.2 DSP1600 Core Architectural Overview

Figure 5 shows a block diagram of the DSP1600 core, which consists of the modules described in Sections 4.2.1 through 4.2.4. Table 5 on page 25 contains a legend for the DSP1600 core block diagram.

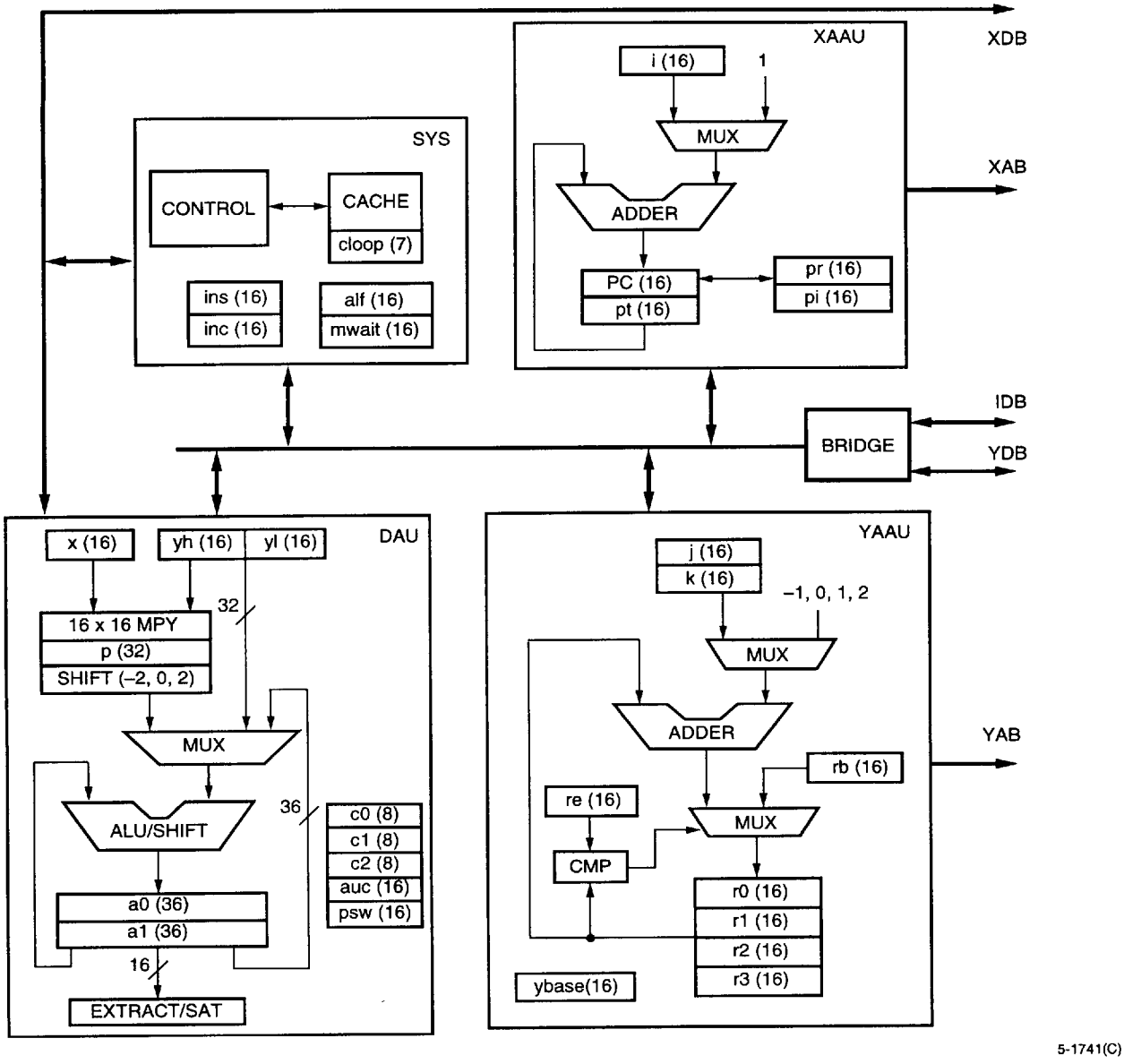


Figure 5. DSP1600 Core Block Diagram

4 Hardware Architecture (continued)

4.2 DSP1600 Core Architectural Overview (continued)

Table 5. DSP1600 Core Block Diagram Legend

Symbol	Name
16 x 16 MPY	16-bit by 16-bit multiplier
a0—a1	Accumulators 0 and 1 (16-bit halves specified as **a0**, **a0l**, **a1**, and **a1l**)*
alf	Low-power standby mode and memory map control
ALU/SHIFT	Arithmetic logic unit/shifter
auc	Arithmetic unit control
c0—c2	Counters 0—2
cloop	Cache loop count
CMP	Comparator
DAU	Digital arithmetic unit
i	Increment register
IDB	Internal data bus
inc	Interrupt control
ins	Interrupt status
j	Increment register
k	Increment register
MUX	Multiplexer
mwait	External memory wait-states control
p	Product register (16-bit halves specified as **p**, **pl**)
PC	Program counter
pi	Program interrupt return register
pr	Program return register
psw	Processor status word
pt	X address space pointer
r0—r3	Y address space pointers
rb	Modulo addressing register (begin address)
re	Modulo addressing register (end address)
SYS	System cache and control section
x	Multiplier input register
XAAU	X space address arithmetic unit
XAB	X space address bus
XDB	X space data bus
YAAU	Y space address arithmetic unit
YAB	Y space address bus
YDB	Y space data bus
ybase	Direct addressing base register
y	DAU register (16-bit halves specified as **y**, **yl**)

* F3 ALU instructions with immediates require specifying the high half of the accumulators as **a0h** and **a1h**.

4 Hardware Architecture (continued)

4.2 DSP1600 Core Architectural Overview (continued)

4.2.1 System Cache and Control Section (SYS)

This section of the core contains a 15-word cache memory and controls the instruction sequencing. It handles vectored interrupts and traps and also provides decoding for registers outside of the DSP1600 core. SYS stretches the processor cycle if wait-states are required (wait-states are programmable for external memory accesses). SYS sequences downloading through JTAG of self-test programs to internal DPRAM.

The cache loop iteration count can be specified at run time under program control as well as at assembly time.

4.2.2 Data Arithmetic Unit (DAU)

The data arithmetic unit (DAU) contains a 16 x 16 parallel multiplier that generates a full 32-bit product in one instruction cycle. The product can be accumulated with one of two 36-bit accumulators. The accumulator data can be directly loaded from, or stored to, memory in two 16-bit words with optional saturation on overflow. The arithmetic logic unit (ALU) supports a full set of arithmetic and logical operations on either 16-bit or 32-bit data. A standard set of flags can be tested for conditional ALU operations, branches, and subroutine calls. This procedure allows the processor to perform as a powerful 16-bit or 32-bit microprocessor for logical and control operations.

The user also has access to two additional DAU registers. The **psw** register contains status information from the DAU. The arithmetic control register, **auc**, is used to configure some of the features of the DAU.

4.2.3 Y Space Address Arithmetic Unit (YAAU)

The YAAU supports high-speed, register-indirect, compound, and direct addressing of data (Y) memory. Four general-purpose 16-bit pointer registers, **r0** to **r3**, are available in the YAAU. These registers can be used to supply the read or write addresses for Y space data.

The YAAU also decodes the 16-bit data memory address and outputs individual memory enables for the data access. The YAAU can address the 1 Kword DPRAM or three external memory segments. Up to 48 Kwords of off-device RAM are addressable.

Two 16-bit registers, **rb** and **re**, allow zero-overhead modulo addressing of data for efficient filter implementations. Two 16-bit signed registers, **j** and **k**, are used to hold user-defined postmodification increments. Fixed increments of +1, –1, and +2 are also available. Four compound addressing modes are provided to make read/write operations more efficient.

The YAAU allows direct (or indexed) addressing of data memory. In direct addressing, the 16-bit base register (**ybase**) supplies the 11 most significant bits of the address. The direct data instruction supplies the remaining 5 bits to form a Y space memory address and also specifies one of 16 registers for source or destination.

4.2.4 X Space Address Arithmetic Unit (XAAU)

The XAAU supports high-speed, register-indirect instruction/coefficient memory addressing with postmodification of the register. The **pt** register is used for addressing coefficients. The signed register **I** holds a user-defined postincrement. A fixed postincrement of +1 is also available. Register PC is the program counter. Registers **pr** and **pi** hold the return address for subroutine calls and interrupts, respectively.

All of the XAAU registers and the adder for increments are 16 bits wide. The XAAU decodes the 16-bit instruction/coefficient address and produces signals for the appropriate X memory segment. The addressable X segments are internal ROM, internal DPRAM, external ROM.

The locations of these memory segments depend upon the memory map selected. A security mode can be selected by mask option. This prevents unauthorized access to the contents of internal ROM.

4 Hardware Architecture (continued)

4.3 Interrupts, Trap, and Low-Power Standby Mode

The DSP1605 supports vectored interrupts and a trap. The device has nine internal hardware sources of program interrupt and one external interrupt pin. As shown in Table 6, each interrupt source has a unique vector address. The TRAP from JTAG also has a unique vector address.

Vectored interrupts are enabled in the **inc** register (see Table 31 on page 53) and monitored in the **ins** register (see Table 32 on page 53).

Table 6. Interrupt Vectors

Source	Vector	Priority	Issued By
No interrupt	0x0	—	—
Reserved	0x2	1 (lowest)	—
Reserved	0x1	2	—
JINT	0x42	3	JTAG interrupt
TIME0	0x4	4	TIMER0 expired
Reserved	0x8	5	—
INTB	0xc	6	INTB pin
Reserved	0x10	7	—
IBFB	0x14	8	SIO channel B input buffer full
OBEB	0x18	9	SIO channel B output buffer empty
Reserved	0x1c	10	—
Reserved	0x20	11	—
POBE	0x24	12	PHIF read
PIBF	0x28	13	PHIF write
IBF	0x2c	14	SIO (channel A) input buffer full
OBE	0x30	15	SIO (channel A) output buffer empty
TIME1	0x34	16	TIMER1 expired
Reserved	0x38	17	—
TRAP from JTAG	0x3	18	JTAG
Reserved	0x46	19 (highest)	—

4.3.1 Interruptibility

Vectored interrupts are serviced only after an interruptible instruction or the completion of a prior interrupt service routine. If more than one vectored interrupt is asserted at the same time, the interrupts are serviced sequentially according to their assigned priorities. Interrupt service routines, branch and conditional branch instructions, cache loops, and instructions which only decrement one of the RAM pointers, **r0** to **r3**, (e.g., ***r3– –**) are not interruptible.

A trap is similar to an interrupt, but it gains control of the processor by branching to the trap service routine even when the current instruction is noninterruptible. It may not be possible to return to normal instruction execution from the trap service routine because the machine state cannot always be saved. In particular, program execution cannot be continued from a trapped cache loop or interrupt service routine. While in a trap service routine, another trap is ignored.

4 Hardware Architecture (continued)

4.3 Interrupts, Trap, and Low-Power Standby Mode (continued)

4.3.1 Interruptibility (continued)

When set to 1, the status bits in the **ins** register indicate that an interrupt has occurred. Before an enabled vectored interrupt can be acted on, the processor must reach an interruptible state (completion on an interruptible instruction or a prior interrupt service routine). An interrupt is not serviced if it is not enabled. Polled interrupt service can be implemented by disabling the interrupt in the **inc** register and polling the **ins** register for the expected event.

4.3.2 Vectored Interrupts

A logic 1 written to any bit of the **inc** enables (or unmasks) the associated interrupt. If the bit is cleared to a logic 0, the interrupt is disabled (or masked).

The occurrence of an interrupt that is not masked causes the program execution to transfer to the memory location pointed to by that interrupt's vector address, assuming no other interrupt is being serviced.

The occurrence on an interrupt that is masked causes no automatic processor action, but it does set the corresponding status bit in the **ins** register. If an interrupt occurs while it is masked, it is latched. Subsequently, unmasking the interrupt causes it to be serviced as soon as the processor reaches an interruptible state. The status of the interrupt sources is readable in the **ins** register even if the interrupt is masked in the **inc** register.

4.3.3 External Interrupt Pin (INTB)

INTB is a negative edge triggered interrupt pin. External hardware must guarantee that the interrupt service routine has completed before issuing another interrupt on INTB. Any activity on INTB is **not** recognized during the interrupt service routine and must be reissued after the completion of the interrupt service routine. Because there is no interrupt acknowledge pin on the DSP1605, the interrupt service routine must communicate with the external hardware through other means. One possible way of performing this task would be through the use of IOP pins.

4.3.4 Clearing Interrupts

The SIO interrupts (IBF, IBFB, OBE, and OBEB) are cleared by reading or writing, as appropriate, the **sdx0** register. The JTAG interrupt (JINT) is cleared by reading the **jtag** register.

Other interrupts are cleared by either of the following methods:

- After a vectored interrupt has been serviced, it is cleared when the **ireturn** instruction is issued, leaving set any other vectored interrupts that are pending.
- In the **ins** register, writing a 1 to the bit that is associated with the interrupt.

If interrupts occur concurrently, all interrupts are serviced according to their priority.

4.3.5 Low-Power Standby Mode (AWAIT)

Setting the AWAIT bit (bit 15) of the **alf** register causes the processor to go into a low-power standby mode. Only the minimum circuitry on the device required to process an incoming interrupt remains active, which includes the SIO registers. If enabled, the timers, TIMER0 and TIMER1, also remain functional. After the AWAIT bit is set, one additional instruction is executed before the low-power standby mode is entered. An SIO word transfer completes if already in progress. The AWAIT bit is reset when the first interrupt occurs. The device then wakes up and continues executing.

Two **nop** instructions should be programmed after the AWAIT bit is set. The first **nop** (one cycle) is executed before sleeping. The second one is executed after the interrupt signal awakens the DSP, and before the interrupt service routine is executed.

For maximum power savings, do the following:

1. Set **ioc** to 0x3C00. This selects the low-frequency clock and holds the CKO pin low. (Although the DSP1605 68-pin PLCC package does not provide a CKO pin, the **ioc** register must still be set to 0x3C00 for minimum power consumption in low-power standby mode.)
2. Set **timerc** to 0x4040. This shuts down the timer and prescaler.
3. Make sure that no IOP port pins are floating.
4. Drive pins DB[7:0] to logic low.
5. Drive pins TDI and TMS to logic high.
6. Set **alf** to 0x8000. This sets the low-power standby mode.

4 Hardware Architecture (continued)

4.4 Memory Maps and Wait-States

The DSP1605 implements a modified Harvard architecture that has separate internal 16-bit address and data buses for the instruction/coefficient (X) and data (Y) memory spaces. The DSP1605 contains 16 Kwords of ROM (IROM) and 1 Kword of dual-port RAM (RAM1). The DSP1605 has a multiplexed external bus that accesses external RAM (ERAMHI and ERAMLO). Programmable wait-states are provided for external memory accesses to ERAMHI and ERAMLO. The instruction/coefficient memory map is configurable to provide application flexibility. Table 7 shows the two instruction/coefficient memory maps available for the DSP1605. Table 8 shows the data memory map, which is fixed.

Table 7. DSP1605 Instruction/Coefficient Memory Map

Decimal Address	Address in PC, pt, pi, pr	MAP1 LOWPR* = 0	MAP3† LOWPR = 1
0 — 1023	0x0000 — 0x03FF	IROM	RAM1
1024 — 16,383	0x0400 — 0x3FFF		Reserved
16,384 — 32,767	0x4000 — 0x7FFF	Reserved	IROM
32,768 — 49,151	0x8000 — 0xBFFF		Reserved
49,152 — 50,175	0xC000 — 0xC3FF	RAM1	
50,176 — 65,535	0xC400 — 0xFFFF	Reserved	

* LOWPR is an **alf** register bit. The AT&T development system tools can independently set the memory map.

† MAP3 is not available if the mask-programmable secure option is selected.

The internal RAM can be accessed by both the Y space and the X space. If the same bank of internal RAM is accessed from both memory spaces simultaneously, one wait-state is added, and the Y space is accessed first.

Table 8. DSP1605 Data Memory Map

Decimal Address	Address in r0, r1, r2, r3	Segment
0 — 1023	0x0000 — 0x03FF	RAM1
1024 — 16,383	0x0400 — 0x3FFF	Reserved
16,384 — 32,767	0x4000 — 0x7FFF	ERAMLO
32,768 — 65,535	0x8000 — 0xFFFF	ERAMHI

4.4.1 Instruction/Coefficient Memory Map Selection

In determining which memory map (MAP1 or MAP3) to use, the processor evaluates the state of the LOWPR bit (bit 14) of the **alf** register. The LOWPR bit of the **alf** register is initialized to 0 automatically at reset. LOWPR controls the address in memory assigned to the dual-port RAM. If LOWPR is low, internal dual-port RAM begins at address 0xC000. If LOWPR is high, internal dual-port RAM begins at address 0x0. LOWPR also moves IROM from 0x0 in MAP1 to 0x4000 in MAP3.

The AT&T development system tools using the JTAG port can independently set the memory map. Specifically, during a JTAG trap, the memory map is forced to MAP1. The user's map selection is restored when the trap service routine has completed execution.

Whenever the device is reset using the RSTB pin, the default memory map is MAP1. A reset through JTAG does not reinitialize the **alf** register, so the previous memory map is retained.

4 Hardware Architecture (continued)

4.4 Memory Maps and Wait-States (continued)

4.4.2 Data Memory Map Selection

Table 8 on page 29 shows the DSP1605 data memory map. RAM1 is a 1 Kword bank of internal dual-port RAM. ERAMLO and ERAMHI are external memory segments for external data RAMs. The ERAMHI segment may contain DRAM, for which the DRAM controller is enabled by setting bit 8 of the **ioc** register (see Table 33 on page 54).

Because both external memory segments reside in the upper half of the data memory space, the most significant address bit for each segment is always 1. Therefore, because there is no need to connect the most significant bit of the internal data address bus to external address bus, the external memory address bus, AB[14:0], has only 15 bits.

4.5 External Memory Interface (EMI)

The external memory interface supports read/write operations from data memory. The DSP1605 provides a 15-bit external address bus, AB[14:0], and an 8-bit external data bus, DB[7:0]. These buses are multiplexed between the internal buses for the data memory.

4.5.1 Memory Segment Enables

Two external memory enables, ERAMLO and ERAMHI, select the external memory segment to be addressed. The flexibility provided by the programmable options of the external memory interface allows the DSP1605 to interface gluelessly with a variety of commercial memory devices. See the **mwait** register, Table 36 on page 55, and the **ioc** register, Table 33 on page 54. Each of the two external memory segments, ERAMLO and ERAMHI, has a number of wait-states that is programmable (from 0 to 15) by writing to the **mwait** register. When the program references memory in one of the two external segments, the internal multiplexer is automatically switched to the appropriate set of internal buses, and the associated external enable of ERAMLO and ERAMHI is issued. The external memory cycle is automatically stretched by the number of wait-states in the appropriate field of the **mwait** register.

When writing to external memory, the RWN pin goes low for the external cycle. The external data bus, DB[7:0], is driven by the DSP starting halfway through the cycle. The data driven on the external data bus is automatically held after the cycle unless an external read cycle immediately follows. When an access to internal memory is made, the AB[14:0] bus holds the last valid external memory address. After reset, the AB[14:0] value is undefined.

The leading edge of the memory segment enables can be delayed approximately one-half an instruction cycle by programming bits 0 and 2 of the **ioc** register (see Table 33). This capability prevents a situation in which two devices might drive the data bus simultaneously.

4.5.2 DRAM Support

The DSP interfaces directly to dynamic RAMs. The ERAMHI segment may contain DRAM, for which the DRAM controller is enabled by setting bit 8 of the **ioc** register (see Table 33 on page 54). The timing of the row address select (RASN) and column address select (CASN) strobes are programmable for support of slow as well as fast DRAMs. The dynamic RAM control register (**drc**, see Table 30 on page 52) contains fields for programming the CASN delay, the access time, and the precharge time. The DRAM controller also automatically refreshes DRAMs, with a variable refresh interval programmed in the **drc** register. Also supported are CASN before RASN refreshing and the early write cycle on write transactions to DRAM. When the DSP is operating from the low-frequency clock (XTAL2), the DRAM controller prevents corruption of the DRAM contents by continuously refreshing using the low-frequency clock. During this time, the program must not access external memory. The DRAM controller also continues to refresh the DRAM during a reset, when the RSTB pin is asserted low.

On a DRAM access, the contents of the page register (**pgreg**, see Table 39 on page 57) are first driven onto the address bus as the row address for the DRAM devices. Next, the RASN strobe is asserted. The column address, which comes from the contents of the Y address space register pointer specified in the instruction, is then driven onto the address bus. This is followed by the assertion of the CASN strobe. The RWN signal indicates whether a read or write transaction is to occur. At the end of the programmed access time, both RASN and CASN are deasserted (returned high).

4 Hardware Architecture (continued)

4.6 Serial I/O Unit (SIO)

The serial I/O port on the DSP provides a serial interface to many codecs and signal processors with little, if any, external hardware required. Both a single-channel mode and a dual-channel mode are supported, selectable by bit 15 of the **sioc** register in conjunction with a mask option (see Table 43 on page 59). The high-speed, double-buffered port supports back-to-back transmissions of data. Output data transfers of 8, 16, 32, or 48 bits, and input data transfers of 8, 16, or 32 bits may be defined. Serial data is read through the **sdx<0—1>**_i registers, and written through the **sdx<0—2>**_o registers (**sdx2**_o is used only for 48-bit output). (Note that in the DSP instructions, the _i and _o suffixes are not used because they are implied by the instruction context.) The output buffer empty (OBE and OBEB) and input buffer full (IBF and IBFB) flags facilitate the reading and/or writing of the serial I/O port by program- or interrupt-driven I/O (see Table 31 and Table 32 on page 53).

4.6.1 Single-Channel SIO

For communication with a single external serial device, the SIO can be configured for single-channel mode. In this mode, the SIO pins take on the functions shown in Table 9.

Table 9. Pin Functions in Single-Channel Mode

Pin	Single-Channel Function
SCKA	Serial output clock (OCK)
SCKB	Serial input clock (ICK)
SLDA	Serial output load (OLD)
SLDB	Serial input load (ILD)
SDO	Serial data out
SDI	Serial data in

The UENHSIO bit of the **ioc** register (see Table 33 on page 54) must be set in order to enable the SCKB signal onto the corresponding device pin. If the UENHSIO bit is cleared, the SCKB signal is internally tied to the SCKA signal, and the input and output sections share the same clock.

Programmable modes of operation for the SIO are controlled by the serial I/O control registers: **sioc** and **sioce** (see Table 43 on page 59 and Table 44 on page 60). These registers are used to set the ports into various configurations. The following options are available to configure both the input and output sections together:

- MSB or LSB first for data
- Delayed load

In addition, the following options are available to configure the input and output sections independently:

- Passive or active load clocks
- Passive or active data clocks
- Selectable duty cycle of load clocks
- High or low assertion level for load clocks
- Frequency of active load clocks
- Frequency of data clocks
- Output data: 8, 16, 32, or 48 bits
- Input data: 8, 16, or 32 bits

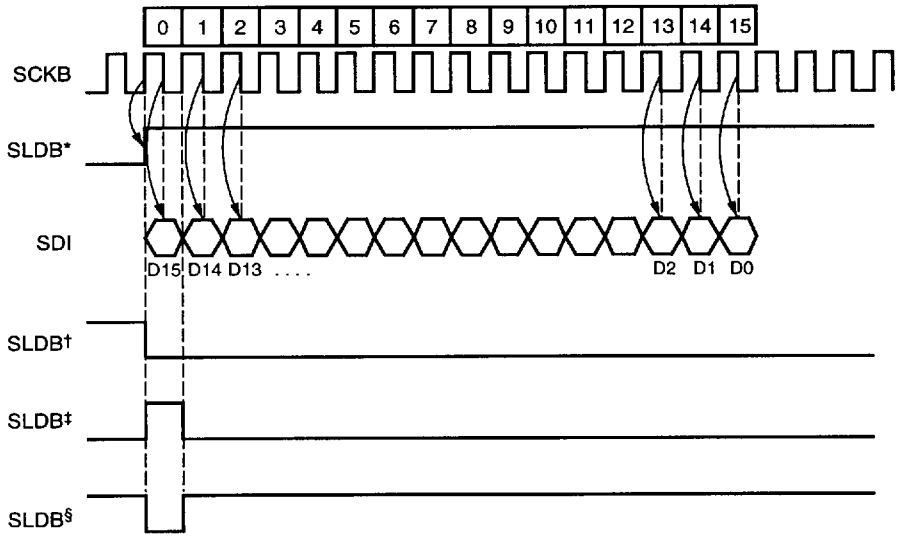
In the active mode, the DSP generates the signal. In the passive mode, the signal is an input, driven from an external source. Selectable active clock frequencies support 2.048 MHz, 4.096 MHz, and 8.192 MHz clock rates with a XTAL1 frequency of 32.768 MHz. Active data load rates of 8 kHz and 16 kHz (with a 32.768 MHz crystal connected to XTAL1) are among several selectable options.

4 Hardware Architecture (continued)

4.6 Serial I/O Unit (SIO) (continued)

4.6.1 Single-Channel SIO (continued)

The functional timing for the delayed load mode (controlled by the LDD bit in the **sioce** register) is illustrated in Figures 6 and 7. For each figure, four configurations of the load clock (SLDA and SLDB) are shown, corresponding to the four combinations of two selectable duty cycles and two selectable assertion levels for the load clocks. If the delayed load mode is not selected, the load signal appears one serial clock cycle earlier.



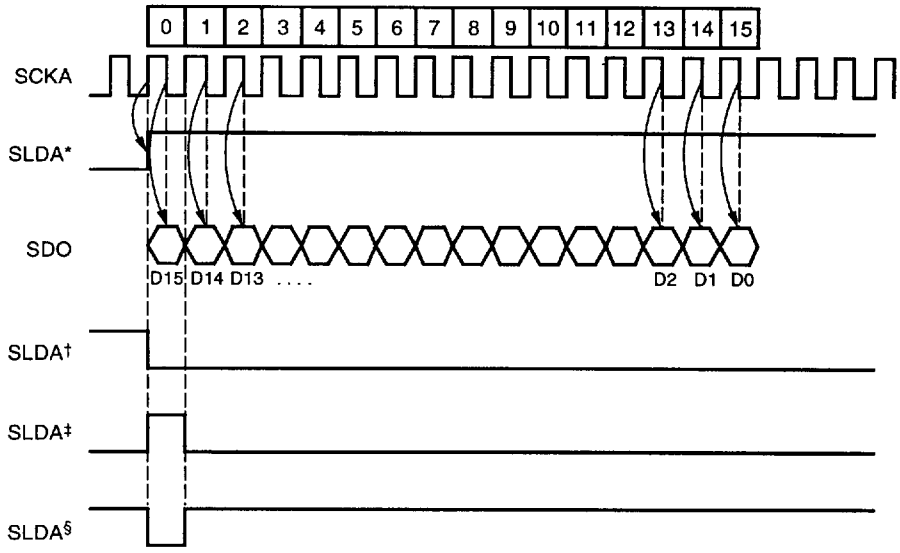
* ILDP = 0, ILDH = 1.
† ILDP = 0, ILDH = 0.
‡ ILDP = 1, ILDH = 1.
§ ILDP = 1, ILDH = 0.

Figure 6. Serial Input with Delayed Active Load (LDD = 1)

4 Hardware Architecture (continued)

4.6 Serial I/O Unit (SIO) (continued)

4.6.1 Single-Channel SIO (continued)



5-3997(C)

* OLDP = 0, OLDH = 1.
† OLDP = 0, OLDH = 0.
‡ OLDP = 1, OLDH = 1.
§ OLDP = 1, OLDH = 0.

Figure 7. Serial Output with Delayed Active Load (LDD = 1)

4 Hardware Architecture (continued)

4.6 Serial I/O Unit (SIO) (continued)

4.6.2 Dual-Channel SIO

For communication with two external serial devices, the SIO can be configured for dual-channel mode (see Table 43 on page 59). In this mode, the SIO pins take on the functions shown in Table 10.

Table 10. Pin Functions in Dual-Channel Mode

Pin	Dual-Channel Function
SCKA	Serial clock for channel A (input and output)
SCKB	Serial clock for channel B (input and output)
SLDA	Serial load for channel A (input and output)
SLDB	Serial load for channel B (input and output)
SDO	Serial data out (channels A and B)
SDI	Serial data in (channels A and B)

The UENHSIO bit of the **ioc** register (see Table 33 on page 54) must be set in order to enable the SCKB signal onto the corresponding device pin. If the UENHSIO bit is cleared, the SCKB signal is internally tied to the SCKA signal, and both channel A and channel B share the same clock.

Programmable modes of operation for the SIO are controlled by the serial I/O control registers: **sioc** and **sioce** (see Table 43 on page 59 and Table 44 on page 60). These registers are used to set the ports into various configurations. The following options are available to configure both channel A and channel B sections together:

- MSB or LSB first for data
- Delayed load
- Back-to-back transfers as opposed to offset

In addition, the following options are available to configure channel A and channel B independently:

- Passive or active load clocks
- Passive or active data clocks
- Selectable duty cycle of load clocks
- High or low assertion level for load clocks
- Frequency of active load clocks
- Frequency of data clocks
- Output data: 8, 16, 32, or 48 bits
- Input data: 8, 16, or 32 bits

In the active mode, the DSP generates the signal. In the passive mode, the signal is an input, driven from an external source.

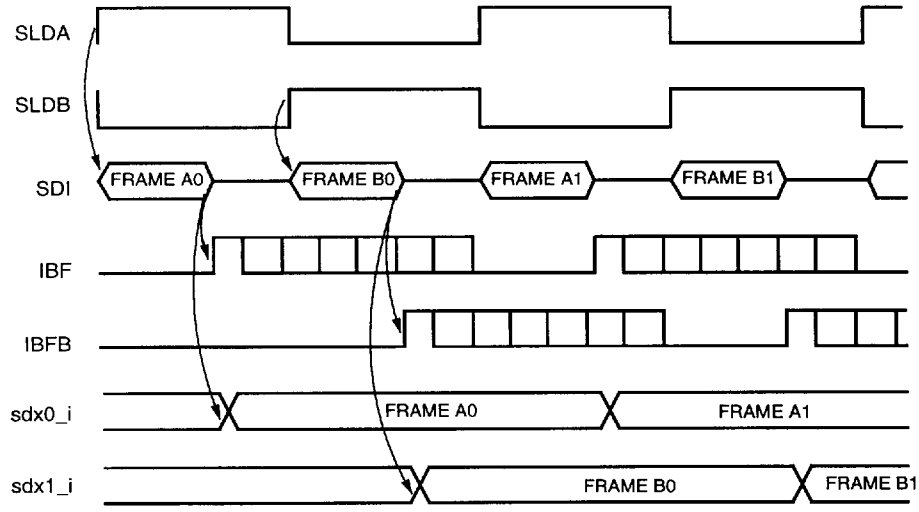
Selectable active clock frequencies support 2.048 MHz, 4.096 MHz, and 8.192 MHz clock rates with an XTAL1 frequency of 32.768 MHz. Active data load rates of 8 kHz and 16 kHz (with a 32.768 MHz crystal connected to XTAL1) are among several selectable options.

If both channels are configured for 8- or 16-bit transactions, the SIO unit is fully double-buffered. On the input port, channel A data is loaded in **sdx0**_i and channel B data is loaded into **sdx1**_i (see Figure 8 on page 35). Two interrupt flags are available: IBF for channel A and IBFB for channel B. The IBF flag is cleared when **sdx0**_i is read by the DSP; the IBFB flag is cleared when **sdx1**_i is read. The flag IBF is set when channel A data is received and loaded into **sdx0**_i. Likewise, IBFB is set when channel B data is received and loaded into **sdx1**_i. Eight-bit transaction lengths are sign-extended.

4 Hardware Architecture (continued)

4.6 Serial I/O Unit (SIO) (continued)

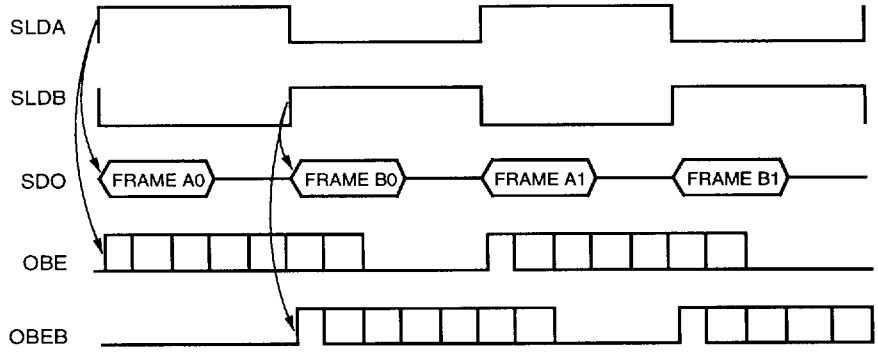
4.6.2 Dual-Channel SIO (continued)



53998(C)

Figure 8. Dual-Channel SIO 8-Bit or 16-Bit Data Input

On the output port, when the load signal is detected for channel A, data is transferred from **sdx0**_o to the output shift register and the OBE flag is set (see Figure 9). The OBE flag is cleared when data is written to **sdx0**_o by the DSP. For channel B, when the load signal for channel B is detected, data is transferred from **sdx1**_o to the output shift register and the OBEB flag is set. The OBEB flag is cleared when **sdx1**_o is written by the DSP.



5-3999(C)

Figure 9. Dual-Channel SIO 8-Bit or 16-Bit Data Output

4 Hardware Architecture (continued)

4.6 Serial I/O Unit (SIO) (continued)

4.6.2 Dual-Channel SIO (continued)

If either channel is configured for 32- or 48-bit transfers, the SIO unit is not fully buffered. Therefore, the **sdx<0—1>**_i registers and the input shift register are used to potentially hold data at the same time for each channel. Similarly, the **sdx<0—2>**_o registers and the output shift register are used to potentially hold data at the same time for each channel. Typically, interrupts for one channel must be serviced before the load for the next channel occurs; otherwise, data is lost.

If channel A and B transactions are spread out in time by setting the D50 configuration bit to 1 (see Table 44 on page 60), the following sequences occur:

- For 32-bit input transfers with the D50 bit set (see Figure 10), when channel A data is received, it is transferred from the input shift register to **sdx0**_i and to **sdx1**_i. The IBF flag is set. Next, when channel B data is received, it is transferred to **sdx0**_i and to **sdx1**_i. Channel A must be serviced before all of the channel B data bits have been received and vice versa; otherwise, data may be lost.

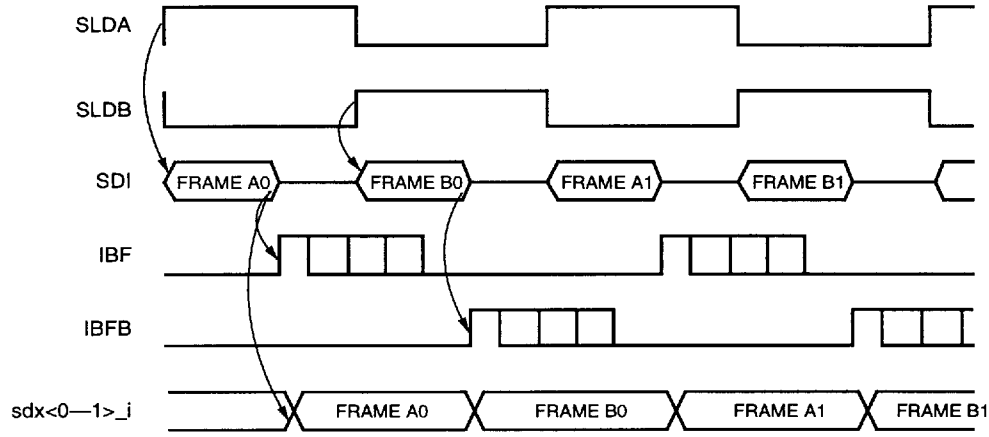


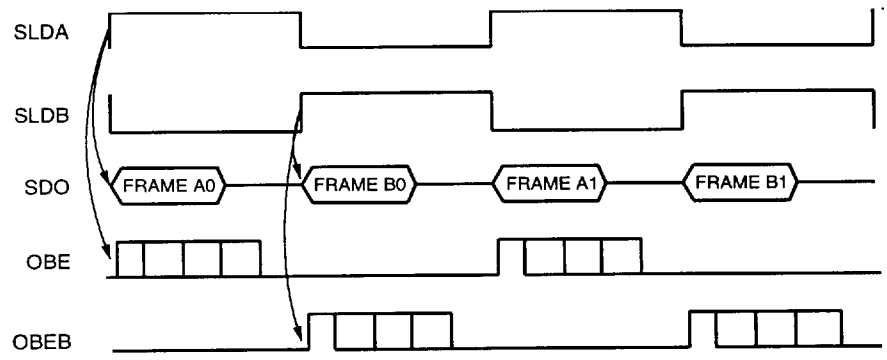
Figure 10. Dual-Channel SIO 32-Bit Data Input (Load Offset Selected (D50 = 1))

- For 32-bit output transfers with the D50 bit set (see Figure 11 on page 37), on a load for channel A, data is transferred from the **sdx<0—2>**_o registers to the output shift register. The OBE flag is set and the data is shifted out from the SDO pin. Similarly, when the channel B load occurs, the data is loaded from the **sdx<0—2>**_o registers into the output shift register and the data is shifted out from SDO. Again, the OBEB flag is cleared when the output shift register is loaded. When the **sdx0** register is written, an internal SIO unit status bit keeps track of whether channel A or channel B data is expected, and the appropriate flag is cleared. This status bit is toggled on every write to the **sdx0** register. When the SIO unit is initially configured for dual-channel mode by changing the DUAL bit in the **sioc** register from a zero to a one, the SIO unit resets the status bit and expects data for channel A to be written into the **sdx<0—2>** registers.

4 Hardware Architecture (continued)

4.6 Serial I/O Unit (SIO) (continued)

4.6.2 Dual-Channel SIO (continued)



5-4001(C)

Figure 11. Dual-Channel SIO 32-Bit or 48-Bit Data Output (Load Offset Selected (D50 = 1))

If channel A and B transactions are set back-to-back by clearing the D50 configuration bit to 0 and one channel is configured for 32-bit or 48-bit transactions, the following sequences occur:

- On the input port, first channel A data is received and transferred to the **sdx<0—1>**_i registers. The IBF flag is set. Next, channel B data is received and the IBFB flag is set. This data from channel B is not transferred to the **sdx<0—1>**_i registers until the channel A data is read as indicated by the IBF flag being cleared.
- On the output port, data for channel A should first be loaded, followed by channel B data. The channel A data is immediately transferred from the **sdx<0—2>**_o registers to the output shift register to make room for the channel B data. When the load for channel A occurs, the data is shifted out of the output shift register and onto the SDO pin. The OBE flag is set when the last bit has been shifted onto SDO. Next, the channel B data is transferred from the **sdx<0—2>**_o registers to the output shift register when the channel B load occurs. This data is then shifted out. After the last data bit has been shifted out, the OBEB flag is set.

4.7 I/O Port (IOP)

The DSP1605 contains one 8-bit IOP unit that controls the directions of eight bidirectional control I/O pins, IOP[7:0]. If a pin is configured as an output, it can be individually set, cleared, or toggled. If a pin is configured as an input, it can be read. See Table 11 for IOP operations.

The lower half of the **sbit** register (see Table 42 on page 58) contains the current values (VALUE[7:0]) of the eight bidirectional pins. The upper half of the **sbit** register (DIR[7:0]) controls the direction of the pins independently. A logic 1 configures the corresponding pin as an output; a logic 0 configures it as an input. The upper half of the **sbit** register is cleared upon reset, configuring all IOP pins as inputs.

4 Hardware Architecture (continued)

4.7 I/O Port (IOP) (continued)

The **cbit** register (see Table 42 on page 58) contains two 8-bit fields, MODE[7:0] and DATA[7:0]. The values of DATA[7:0] are cleared upon reset. The meaning of a bit in either field depends on whether it has been configured as an input or an output in the **sbit** register. If a pin has been configured to be an output, the meanings are MODE and DATA. For an input, MODE and DATA are ignored. Table 11 shows the functionality of the MODE and DATA bits based on the direction selected for the associated IOP pin.

Table 11. IOP Operations

DIR[n*]	MODE[n*]	DATA[n*]	Action on IOP[n*]
1 (Output)	0	0	Clear
1 (Output)	0	1	Set
1 (Output)	1	0	No Change
1 (Output)	1	1	Toggle
0 (input)	Don't Care	Don't Care	Input

* $0 \le n \le 7$.

If an IOP pin is switched from being configured as an output to being configured as an input and then back to being configured as an output, the pin retains the previous output value.

4.8 Timers

The DSP1605 contains two timers, TIMER0 and TIMER1. TIMER0 is composed of three main blocks: the timer control register, the prescaler, and the timer itself. The timer control register, **timerc**, (see Table 45 on page 61) sets up the operational state of the timer and prescaler. The prescaler is a programmable divider that can be set to a count of 2 to 65,536. It provides a wide range of time delay. The timer itself is a 16-bit binary counter that can be preloaded with any 16-bit number. If enabled, the timer counts down at the programmed rate and generates an interrupt upon reaching zero.

If the TIME0 interrupt is enabled (see Table 31 on page 53), program control jumps to location 0x0004 where typically a branch to an interrupt service routine should be placed. Writing the **timer0** register sets the initial count into the timer and loads the period register with the same value for repeated count cycles.

The following functions are programmable in the **timerc** register.

- T*n*EN starts TIMER*n* counting when set.
- RELOAD*n* enables repeated counts of TIMER*n* when set. If zero, TIMER*n* counts down once and stops. If one, TIMER*n* automatically reloads the previous starting value from the period register into the **timer*n*** register, and recommences counting down.
- DISABLE*n* turns off the TIMER*n* clock when set. This is a power-saving feature.
- PRESCALE encodes the value of the divider of the clock going to the counter. It ranges from XTALIN/2 to XTALIN/65,536 (where XTALIN is the free-running clock).

The timer interrupt can be individually enabled or disabled through the **inc** register. The timer can be stopped and started by software and can be reloaded with a new delay at any time. Its current value can also be read by software. When the DSP is reset, the timer is guaranteed to be in an inactive state.

The timer is normally run with two data move instructions, one to write the **timer0** register with the initial count, and the second to write the **timerc** register with initial values. Setting T*n*EN starts the counting.

When the DSP is reset, the control bits of the **timerc** register and the timer itself are initialized to 0. This sets the prescaler to XTALIN/2, turns off the reload feature, disables timer counting, and initializes the timer value to its inactive state. The act of resetting the device does not cause a timer interrupt. Note that the period register is not initialized on reset. Also, if the timer clocks are turned off by DISABLE*n*, the period register cannot be written.

TIMER1 is the same as TIMER0, except that it has no prescaler and its clock is XTAL2 ÷ 4.

4 Hardware Architecture (continued)

4.9 Parallel Host Interface (PHIF)

The DSP1605 has an 8-bit parallel host interface for rapid transfer of data with external devices. This parallel port is passive (data strobes provided by an external device) and supports either *Motorola* or *Intel* microcontroller protocols. The PHIF also provides for 8-bit or 16-bit data transfers. As a flexible host interface, it requires little or no glue logic to interface to other devices (e.g., microcontrollers, microprocessors, or another DSP).

The data path of the PHIF consists of a 16-bit input buffer, **pdx0**_i, and a 16-bit output buffer, **pdx0**_o. In addition, there are two registers used to control and monitor the PHIF's operation: the parallel host interface control register (**phifc**, see Table 37), and the PHIF status register (PSTAT, see Table 40). The PSTAT register, which reflects the state of the PIBF (parallel input buffer full) and POBE (parallel output buffer empty) flags, can only be read by an external device when the PSTAT input pin is asserted. The **phifc** register defines the programmable options for this port.

The function of the pins PIDS/PRWN and PODS/PDS is programmable to support both the *Intel* and *Motorola* protocols. The pin PCSN is an input that, when low, enables PIDS and PODS (or PRWN and PDS, depending on the protocol used). While PCSN is high, the DSP1605 ignores any activity on PIDS/PRWN and/or PODS/PDS. If a DSP1605 is intended to be continuously accessed through the PHIF port, PCSN should be grounded. If PCSN is low and their respective bits in the **inc** register (See Table 31 on page 53) are set, the assertion of PIDS (or PODS) by an external device sets the PIBF (or POBE) flag, and causes the DSP1605 to recognize an interrupt.

The parallel host interface can be programmed for 8-bit or 16-bit data transfers using bit 0, PMODE, of the **phifc** register. Setting PMODE selects 16-bit transfer mode. An input pin controlled by the host, PBSEL, determines an access of either the high or low bytes. The assertion level of the PBSEL input pin is configurable in software using bit 3 of the **phifc** register, PBSELF. Table 12 summarizes the port's functionality as controlled by the PSTAT and PBSEL pins and the PBSELF and PMODE fields.

Table 12. PHIF Function (8-Bit and 16-Bit Modes)

PMODE Field	PSTAT Pin	PBSEL Pin*	PBSELF Field = 0	PBSELF Field = 1	Flag†
0 (8-bit)	0	0	pdx0 low byte	reserved	set
		1	reserved	pdx0 low byte	set
	1	0	PSTAT register	reserved	
		1	reserved	PSTAT register	
1 (16-bit)	0	0	pdx0 low byte	pdx0 high byte	
		1	pdx0 high byte	pdx0 low byte	set
	1	0	PSTAT register	reserved	
		1	reserved	PSTAT register	

* If bit 7 of the **phifc** register, PMUX, is cleared to zero, the PBSEL input pin is ignored and the PBSEL input to the PHIF section is internally tied to logic zero.

† This column indicates the conditions under which the POBE or PIBF flag is set following a read or write of the **pdx0** register. Note that if a reserved condition exists (e.g., PSTAT = PBSEL = 0 and PBSELF = 1) and a read or write operation occurs, no flag is set.

For 16-bit transfers, if PBSELF is zero, the PIBF and POBE flags are set after the high byte is transferred. If PBSELF is one, the flags are set after the low byte is transferred. In 8-bit mode, only the low byte is accessed, and every completion of an input or output access sets PIBF or POBE.

4 Hardware Architecture (continued)

4.9 Parallel Host Interface (PHIF) (continued)

Bit 1 of the **phifc** register, PSTROBE, configures the port to operate either with an *Intel* protocol where only the device select (PCSN) and either of the data strobes (PIDS or PODS) are needed to make an access, or with a *Motorola* protocol where the device select (PCSN), a data strobe (PDS), and a read/write strobe (PRWN) are needed. PIDS and PODS are negative assertion data strobes, while the assertion level of PDS is programmable through bit 2, PSTRB, of the **phifc** register.

Bit 7 of the **phifc** register, PMUX, controls whether the PBSEL input pin is used. If PMUX is cleared to zero, the PBSEL input pin is ignored and the PBSEL input to the PHIF section is internally tied to logic 0. If the PMUX bit is cleared to zero, the combined IOP2/PBSEL pin is freed for the IOP2 function. The IOP2 and PBSEL pins are tied together internally.

5 Software Architecture

5.1 Instruction Set

The DSP1605 processor has six types of instructions: multiply/ALU, special function, control, F3 ALU, cache, and data move. The multiply/ALU instructions are the primary instructions used to implement signal processing algorithms. Statements from this group can be combined to generate multiply/accumulate, logical, and other ALU functions, and to transfer data between memory and registers in the data arithmetic unit. The special function instructions can be conditionally executed based on flags from the previous ALU operation, the condition of one of the counters, or the value of a pseudorandom bit in the DSP1605 device. Special function instructions perform shift, round, and complement functions.

The F3 ALU instructions enrich the operations available on accumulators. The control instructions implement the **goto** and **call** commands. Control instructions can also be executed conditionally. Cache instructions are used to implement low overhead loops, conserve program memory, and decrease the execution time of certain multiply/ALU instructions. Data move instructions are used to transfer data between memory and registers or between accumulators and registers. (For a detailed description of this instruction set, see the *DSP160X Digital Signal Processor Information Manual.*)

The operators in Table 13 are used to describe the instructions in Sections 5.1.1 through 5.1.7.

Table 13. Instruction Set Operators

Symbol	Meaning
*	Denotes any of the following: 16-by-16 multiplication for a 32-bit product Register-indirect addressing when used as a prefix to an address register Direct addressing when used as a prefix to an immediate
+	36-bit addition†
–	36-bit subtraction†
>>	Arithmetic right shift
>>>	Logical right shift
<<	Arithmetic left shift
<<<	Logical left shift
|	36-bit bitwise OR†
&	36-bit bitwise AND†
^	36-bit bitwise EXCLUSIVE OR†
:	Compound address swapping, accumulator shuffling
~	One's complement

† These are 36-bit operations. One operand is 36-bit data in an accumulator; the other operand may be 16, 32, or, 36 bits.

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.1 F1 Multiply/ALU Instructions

Note that the function statements and transfer statements in Table 14 are chosen independently. Any function statement (F1) can be combined with any transfer statement to form a valid multiply/ALU instruction. If either statement is not required, a single statement from either column constitutes a valid instruction. The number of cycles to execute the instruction is a function of the transfer column. (An instruction with no transfer statement executes in one instruction cycle.)

Whenever PC, **pt**, or rM is used in the instruction and points to external memory, the programmed number of wait-states must be added to the instruction cycle count. All multiply/ALU instructions require one word of program memory. The no-operation (**nop**) instruction is a special case encoding of a multiply/ALU instruction and executes in one cycle. The assembly-language representation of a **nop** is either **nop** or a single semicolon.

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.1 F1 Multiply/ALU Instructions (continued)

Table 14. F1 Multiply/ALU Instructions

F1 Function Statement	Transfer Statement†	Transfer Statement Cycles‡	
		Not Using Cache	Using Cache
p = x * y§	y = Y, x = X	2	1
aD = p, p = x * y§	y = aT, x = X	2	1
aD = aS + p, p = x * y§	y[I] = Y	1	1
aD = aS − p, p = x * y§	aT[I] = Y	1	1
aD = p	x = Y	1	1
aD = aS + p	Y	1	1
aD = aS − p	Y = y[I]	2	2
aD = y	Y = aT[I]	2	2
aD = aS + y	Z:y, x = X	2	2
aD = aS − y	Z:y[I]	2	2
aD = aS & y	Z:aT[I]	2	2
aD = aS | y	—	1	1
aD = aS ^ y	—	1	1
aS − y	—	1	1
aS & y	—	1	1

† The [I] is an optional argument that specifies the low 16 bits of aT or **y**.
‡ Add cycles for either of the following:
- When an external memory access is made in X or Y space and wait-states are programmed, add the number of wait-states.
- If an X space access and a Y space access are made to the same bank of DPRAM in one instruction, add one cycle.

§ **p = x * y** becomes a single-cycle squaring operation if the **auc** bit 7 is set. With bit 7 set, a transfer statement of the form **y = Y** loads the **x** register and the **y** register with the same number, so **p = x * y** results in the square.

Note: For transfer statements when loading the upper half of an accumulator, the lower half is cleared if the corresponding CLR bit in the **auc** register is zero. **auc** is cleared by reset.

Table 15. Replacement Table for F1 Multiply/ALU Instructions

Replace	Value	Meaning
aD, aS, aT	a0, a1	One of the DAU accumulators.
X	*pt++, *pt++i	X space memory location pointed to by **pt**. **pt** is postmodified by +1 and **i**, respectively.
Y	*rM, *rM++, *rM− −, *rM++j	RAM location pointed to by rM (M = 0, 1, 2, 3). rM is postmodified by 0, +1, −1, or **j**, respectively.
Z	*rMzp, *rMpz, *rMm2, *rMjk	Read/write compound addressing. rM (M = 0, 1, 2, 3) is used twice. First, postmodified by 0, +1, −1, or **j**, respectively; and, second, postmodified by +1, 0, +2, or **k**, respectively.

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.2 F2 Special Function Instructions

All forms of the special function instructions require one word of program memory and execute in one instruction cycle. (If PC points to external memory, add programmed wait-states.)

The special functions in Table 16 can be executed conditionally, as in:

```
if CON instruction
```

and with an event counter

```
ifc CON instruction
```

which means:

```
if CON is true then
    c1 = c1 + 1
    instruction
    c2 = c1
else
    c1 = c1 + 1
```

The preceding special function instructions can be executed unconditionally by writing them directly. For example, **a0 = a1**.

Table 16. F2 Special Function Instructions

Statement	Meaning
aD = aS >> 1	Arithmetic right shift (sign preserved) of the 36-bit accumulators.
aD = aS >> 4	
aD = aS >> 8	
aD = aS >> 16	
aD = aS	Load destination accumulator from source accumulator.
aD = –aS	2's complement.
aD = ~aS	1's complement.
aD = rnd(aS)	Round upper 20 bits of accumulator.
aDh = aSh + 1	Increment upper half of accumulator (lower half cleared).
aD = aS + 1	Increment accumulator.
aD = y	Load accumulator with 32-bit **y** register value with sign extend.
aD = p	Load accumulator with 32-bit **p** register value with sign extend.
aD = aS << 1	Arithmetic left shift (sign not preserved) of the lower 32 bits of accumulators (upper 4 bits are sign-extended from bit 31 at the completion of the shift).
aD = aS << 4	
aD = aS << 8	
aD = aS << 16	

Table 17. Replacement Table for F2 Special Function Instructions

Replace	Value	Meaning
aD, aS	a0, a1	One of the two DAU accumulators.
CON	mi, pl, eq, ne, gt, le, lvs, lvc, mvs, mvc, c0ge, c0lt, c1ge, c1lt, heads, tails, true, false, npint, njint	See Table 20 for definitions.

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.3 Control Instructions

Table 18 shows control instructions and their required numbers of instruction cycles and program-memory words. Required instruction cycles and program-memory words vary according to whether each instruction is executed unconditionally or conditionally. Control instructions cannot be executed from the cache.

Table 18. Control Instructions

Control Instructions	Executed Unconditionally		Executed Conditionally	
	Number of Cycles	Number of Words	Number of Cycles	Number of Words
goto JA† goto pt‡ call JA† call pt‡ return (goto pr)‡	2	1	3	2
ireturn (goto pi)§	2	1	—	—

† The **goto JA** and **call JA** instructions should not be placed in the last or next-to-last instruction before the boundary of a 4 Kword page. If the **goto** or **call** is placed there, the program counter increments to the next page and the jump is to the next page rather than the desired current page.
‡ If PC, **pt**, or **pr** point to external memory, add programmed wait-states.
§ The **ireturn** instruction can only be executed unconditionally.

With the exception of **ireturn**, the control instructions in Table 18 can be executed conditionally. For example:

```
if le goto 0x0345
```

Table 19. Replacement Table for Control Instructions

Replace	Value	Meaning
CON	mi, pl, eq, ne, gt, le, lvs, lvc, mvs, mvc, c0ge, c0lt, c1ge, c1lt, heads, tails, true, false, npint, njint	See Table 20 for definitions of mnemonics.
JA	12-bit value	Least significant 12 bits of absolute address within the same 4 Kword memory section.

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.4 Conditional Mnemonics (Flags)

Please note the following:

- Testing the state of the counter (**c0** or **c1**) automatically increments the counter by one.
- The pseudorandom sequence generator (PSG) may be reset by writing any value to the **pi** register, except during an interrupt service routine. While in an interrupt service routine, writing to the **pi** register updates the register and does not reset the PSG. If not in an interrupt service routine, writing to the **pi** register resets the PSG. (The **pi** register is updated, but written with the contents of the PC on the next instruction.) Interrupts must be disabled when writing to the **pi** register. If an interrupt is taken after the **pi** write, but before **pi** is updated with the PC value, the **ireturn** instruction does not return to the correct location. However, if the RAND bit in the **auc** register is set, writing the **pi** register never resets the PSG. A random rounding function can be implemented with either heads or tails.

Table 20. DSP1605 Conditional Mnemonics

Test	Meaning	Test	Meaning
pl	Result is nonnegative (sign bit is bit 35).	mi	Result is negative.
eq	Result is equal to 0.	ne	Result is not equal to 0.
gt	Result is greater than 0.	le	Result is less than or equal to 0.
lvs	Logical overflow set.†	lvc	Logical overflow clear.
mvs	Mathematical overflow set.‡	mvc	Mathematical overflow clear.
c0ge	Counter 0 greater than or equal to 0.	c0lt	Counter 0 less than 0.
c1ge	Counter 1 greater than or equal to 0.	c1lt	Counter 1 less than 0.
heads	Pseudorandom sequence bit set.	tails	Pseudorandom sequence bit clear.
true	The condition is always satisfied in an if instruction.	false	The condition is never satisfied in an if instruction.
npint	Not PINT (used by JTAG).	njint	Not JINT (used by JTAG).

† Result is not representable in the 36-bit accumulators (36-bit overflow).
‡ Bits 35:31 are not the same (32-bit overflow).

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.5 F3 ALU Instructions

These instructions, shown in Table 21, are implemented in the DSP1600 core. F3 ALU instructions allow accumulator two-operand operations with either another accumulator, the **p** register, or a 16-bit immediate operand. The result is placed in a destination accumulator that can be independently specified. All operations are done with the full 36 bits. For the accumulator with accumulator operations, both inputs are 36 bits. For the accumulator high with immediate operations, the immediate is sign-extended into bits 35:32 and the lower bits 15:0 are filled with zeros, except for the AND operation, for which they are filled with ones. These conventions allow the user to do operations with 32-bit immediates by programming two consecutive 16-bit immediate operations.

Table 21. F3 ALU Instructions

Cacheable† (1 cycle)	Not Cacheable† (2 cycle)
aD = aS + aT	aD = aSh + IM16
aD = aS − aT	aD = aSh − IM16
aD = aS & aT	aD = aSh & IM16
aD = aS | aT	aD = aSh | IM16
aD = aS ^ aT	aD = aSh ^ IM16
aS − aT	aSh − IM16
aS & aT	aSh & IM16
aD = aS + p	aD = aSl + IM16
aD = aS − p	aD = aSl − IM16
aD = aS & p	aD = aSl & IM16
aD = aS | p	aD = aSl | IM16
aD = aS ^ p	aD = aSl ^ IM16
aS − p	aSl − IM16
aS & p	aSl & IM16

† If PC points to external memory, add programmed wait-states.

Table 22. Replacement Table for F3 ALU Instructions

Replace	Value	Meaning
aD, aT, aS	a0 or a1	One of the two accumulators.
IM16	16-bit value	Long immediate data: sign-, zero-, or one-extended as appropriate.
aSh	a0h or a1h	Upper half of the accumulator.
aSl	a0l or a1l	Lower half of the accumulator.

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.6 Cache Instructions

Each cache instruction requires one program-memory word. Table 23 shows cache instructions and their required numbers of instruction cycles. Control instructions and long immediate values cannot be stored inside the cache.

Table 23. Cache Instructions

Cache Instructions	Number of Cycles†
do	1
redo	2

† If PC points to external memory, add programmed wait-states.

Cache instruction formats are as follows:

```
do K {
INSTR_1
INSTR_2
.
.
.
INSTR_NI
}
redo K
```

Table 24. Replacement Table for Cache Instructions

Replace	Instruction Encoding	Meaning
K	cloop†	Number of times the instructions are to be executed taken from bits 6:0 of the **cloop** register.
	1 to 127	Number of times the instructions are to be executed are encoded in the instruction.
NI	1 to 15	1 to 15 instructions can be included.

† The assembly-language statement, **do cloop** (or **redo cloop**) is used to specify that the number of iterations is to be taken from the **cloop** register. K is encoded as 0 in the instruction encoding to select **cloop**.

When the cache is used to execute a block of instructions, the cycle timings of the instructions are as follows:

- In the first pass, the instructions are fetched from program memory and the cycle times are the normal out-of-cache values, except for the last instruction in the block of NI instructions. This instruction executes in two cycles.
- During pass two through pass K – 1, each instruction is fetched from cache and the in-cache timings apply.
- During the last (Kth) pass, the block of instructions is fetched from cache and the in-cache timings apply, except that the timing of the last instruction is the same as if it were out-of-cache.
- If any of the instructions access external memory, programmed wait-states must be added to the cycle.

The **redo** instruction treats the instructions currently in the cache memory as another loop to be executed K times. Using the **redo** instruction, instructions are re-executed from the cache without reloading the cache.

The number of iterations, K, for a **do** or **redo** can be set at run time by first moving the number of iterations into the **cloop** register (7 bits unsigned), then issuing the **do cloop** or **redo cloop**. At the completion of the loop, the value of **cloop** is decremented to 0; hence, **cloop** needs to be written before each **do cloop** or **redo cloop**.

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.7 Data Move Instructions

Table 25 shows data move instructions and their required numbers of program-memory words and instruction cycles. Required instruction cycles vary according to whether either PC or rM points to external memory. All data move instructions, except those doing long immediate loads, can be executed from within the cache. A direct data addressing mode has been added to the DSP1600 core.

Table 25. Data Move Instructions

Data Move Instructions	Number of Words	Number of Cycles†
R = IM16	2	2
SR = IM9	1	1
aT[I] = R R = aS[I] Y = R R = Y Z:R DR = *(OFFSET) *(OFFSET) = DR	1	2

† If either **PC** or rM point to external memory, add any programmed wait-state. If both **PC** and rM point to same bank of DPRAM, add one cycle.

When signed registers less than 16 bits wide (**c0**, **c1**, **c2**) are read, their contents are sign-extended to 16 bits. When unsigned registers less than 16 bits wide are read, their contents are zero-extended to 16 bits.

Loading an accumulator with a data move instruction does not affect the flags.

Table 26. Replacement Table for Data Move Instructions

Replace	Value	Meaning
R	Any of the registers in Table 72 on page 67†	—
DR	**r<0—3>**, **a0[I]**, **a1[I]**, **y[I]**, **p[I]**, **x**, **pt**, **pr**, **psw**	Subset of registers accessible with direct addressing.
aS, aT	**a0**, **a1**	High half of accumulator.
Y	*rM, *rM++, *rM– –, *rM++j	Same as in multiply/ALU instructions.
Z	*rMzp, *rMpz, *rMm2, *rMjk	Same as in multiply/ALU instructions.
IM16	16-bit value	Long immediate data.
IM9	9-bit value	Short immediate data for YAAU registers.
OFFSET	5-bit value from instruction 11-bit value from base register	Value in bits 15:5 of **ybase** register form the 11 most significant bits of the base address. The 5-bit offset is concatenated to this to form a 16-bit address.
SR	**r<0—3>**, **rb**, **re**, **j**, **k**	Subset of registers for short immediate.

† The **sioc** register is not readable.

5 Software Architecture (continued)

5.2 Register Settings

The following tables, listed alphabetically, describe the programmable registers of the DSP1605.

Note: Some tables in this section use the following abbreviations:

X = don't care
W = write only

Table 27. alf (Standby and Memory Map) Register

Bit	15	14	13—0
Field	AWAIT	LOWPR	Res

Bit	Field	Description
15	AWAIT	Set to 1 to enter low-power standby mode.
14	LOWPR	Memory map selection: 0 = select memory MAP1. 1 = select memory MAP3.
13—0	Res	Reserved—read as zero, write as zero.

Table 28. auc (Arithmetic Unit Control) Register

Bit	15—9	8	7	6—4	3—2	1—0
Field	Res	RAND	X = Y =	CLR	SAT	ALIGN

Bit	Field	Value	Description
15—9	Res	—	Reserved—read as zero, write as zero.
8	RAND	0	Pseudorandom number generator (PNG) reset by writing the **pi** register only outside an interrupt service routine.
		1	PNG never reset by writing the **pi** register.
7	X = Y =	0	Normal operation.
		1	Transfer statements **y = Y** load both the **x** and the **y** registers. All instructions that load the high half of the **y** register also load the **x** register. This allows single-cycle squaring (**p = x * y**).
6—4	CLR	1XX	Clearing **yl** is disabled (enabled when 0).
		X1X	Clearing **a1l** is disabled (enabled when 0).
		XX1	Clearing **a0l** is disabled (enabled when 0).
3—2	SAT	1X	**a1** saturation on overflow is disabled (enabled when 0).
		X1	**a0** saturation on overflow is disabled (enabled when 0).
1—0	ALIGN	00	**a0, a1** ← **p**.
		01	**a0, a1** ← **p**/4.
		10	**a0, a1** ← **p** x 4 (and zeros written to the two LSBs).
		11	Reserved.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 29. cbit (IOP Control Bit) and sbit (IOP Status Bit) Registers

cbit Registers

Bit	15—8	7—0
Field	MODE[7:0]	DATA[7:0]

sbit Registers

Bit	15—8	7—0
Field	DIR[7:0]	VALUE[7:0]†

cbit and sbit Register Fields

DIR[n]‡	MODE[n]‡	DATA[n]‡	Action on IOP[n]‡
1 (Output)	0	0	Clear
1 (Output)	0	1	Set
1 (Output)	1	0	No change
1 (Output)	1	1	Toggle
0 (Input)	x	x	Input

† Read-only. Any value written to this field is ignored.
‡ $0 \le n \le 7$.

Note: Because the **cbit** and **sbit** registers have interrelated fields, and this section lists the register tables alphabetically, Table 29 duplicates the information in Table 42.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 30. drc (DRAM Control) Register

Bit	15—11	10	9—6	5—3	2—0
Field	Res	CADLY	ACC	PRCH	RFSH

Bit	Field	Description
15—11	Res	Reserved—read as zero, write as zero.
10	CADLY	Column address delay: 0 = delay zero (free-running) CKO cycles. 1 = delay one (free-running) CKO cycle. This field programs the number of free-running CKO cycles before switching the address bus from row address to column address. Typically set to 1 to provide more access time for slow DRAM.
9—6	ACC	Access time = ACC + 2. This field programs the number of free-running CKO cycles for access time. ACC + 2 is the length of a DRAM access, measured in CKO cycles. ACC + 2 is counted from when the row address is driven to when the RASN and CASN strobes are negated.
5—3	PRCH	Precharge: 000 = 0 CKO cycles. 100 = 4 CKO cycles. 001 = 1 CKO cycle. 101 = 5 CKO cycles. 010 = 2 CKO cycles. 110 = 6 CKO cycles. 011 = 3 CKO cycles. 111 = 7 CKO cycles. This field programs the number of free-running CKO cycles to allow for precharge. The next access is not allowed to occur until the precharge time is satisfied.
2—0	RFSH	Refresh interval when high-frequency (XTAL1) clock is selected via CLKSEL bit of **ioc** register: 000 = 8 (f_{XTAL1}/32) cycles. 100 = 16 (f_{XTAL1}/32) cycles. 001 = 14 (f_{XTAL1}/32) cycles. 101 = 154 (f_{XTAL1}/32) cycles. 010 = 126 (f_{XTAL1}/32) cycles. 110 = reserved. 011 = 10 (f_{XTAL1}/32) cycles. 111 = reserved. This field programs how often a refresh request is made to the DRAM controller to perform a RASN before CASN refresh cycle. It is based on a clock that is the input crystal frequency of the XTAL1 clock divided by 32. This field is ignored if the low-frequency (XTAL2) clock is selected and the refresh interval is based on the XTAL2 clock frequency. For more information, see Section 8.10, External DRAM Interface.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 31. inc (Interrupt Control) Register

Bit	15	14	13	12—11	10	9	8	7	6	5	4	3	2	1	0
Field	JINT†	PIBF	POBE	Res	OBEB	IBFB	Res	INTB	Res	TIME0	Res	TIME1	Res	OBE	IBF

† JINT is a JTAG interrupt and is controlled by JTAG logic. It may be made unmaskable by the AT&T development system tools.

Encoding: A 0 in a bit of **inc** disables an interrupt; a 1 enables the interrupt. For more information about the fields in Table 31, see Table 6 on page 27.

Table 32. ins (Interrupt Status) Register

Bit	15	14	13	12—11	10	9	8	7	6	5	4	3	2	1	0
Field	JINT	PIBF	POBE	Res	OBEB	IBFB	Res	INTB	Res	TIME0	Res	TIME1	Res	OBE	IBF

Encoding: A 0 indicates no interrupt. A 1 indicates an interrupt has been recognized and is pending or being serviced. If a 1 is written to bits 3, 5, or 7 of **ins**, the corresponding interrupt is cleared. For more information about the fields in Table 32, see Table 6 on page 27.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 33. ioc (I/O Configuration) Register

Bit	15	14	13	12	11—10	9	8	7—3	2	1	0
Field	UENHSIO	Res	OSCDIS	CLKSEL	CKO[1:0]	Res	DRC	Res	DENB2	Res	DENB0

Bit	Field	Description
15	UENHSIO	Select enhanced SIO: 0 = the SCKB signal is internally tied to the SCKA pin. This results in the same clock signals for the SIO input and output sections in single-channel SIO mode (or in the same clock signals for channels A and B in dual-channel mode). The SCKB/IOP1 pin functions as the IOP1 signal. 1 = enhanced SIO mode. The SCKB signal is enabled onto the SCKB/IOP1 pin. This allows independent clock signals for the input and output sections in single-channel SIO mode (or independent clock signals for channels A and B in dual-channel mode).
14	Res	Reserved—read as zero, write as zero.
13	OSCDIS	0 = enable XTAL1 oscillator. 1 = disable XTAL1 oscillator.
12	CLKSEL	0 = select XTAL1. 1 = select XTAL2.
11—10	CKO[1:0]	These 2 bits determine the state of the CKO† (clock-output) pin: **CKO1 = ioc11 / CKO0 = ioc10 / CKO Output / Description** 0 / 0 / XTAL / Free-running clock 0 / 1 / XTAL/(1 + w) / Wait-stated clock 1 / 0 / 1 / Held high 1 / 1 / 0 / Held low
9	Res	Reserved—read as zero, write as zero.
8	DRC	0 = disable DRAM controller. 1 = enable DRAM controller.
7—3	Res	Reserved—read as zero, write as zero.
2	DENB2	If 1, delay pin ERAMHI approximately one-half instruction cycle.
1	Res	Reserved—read as zero, write as zero.
0	DENB0	If 1, delay pin ERAMLO approximately one-half instruction cycle.

† The CKO pin is available only on the 80-pin MQFP package.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 34. JTAG ID Register (32-Bit)

Bit	31	30	29—28	27—19	18—12	11—0
Field	PUR	SECURE	ROM OPT	ROMCODE	DEVICE	0x03B

Bit	Field	Mask-Programmable Features
31	PUR	Powerup reset options: 0 = 5.0 V 1 = 3.3 V
30	SECURE	0 = unsecured. 1 = secured.
29—28	ROM OPT	00 = 8K ROM. 01 = 16K ROM. 10 = 24K ROM. 11 = reserved.
27—19	ROMCODE	The user's ROMCODE ID (in hexadecimal), as calculated by the following formula using the letter codes from Table 35: ROMCODE ID = 0x[(20 x first letter) + second letter] ROMCODE AA—KZ (single CODEC) ROMCODE LA—ZZ (dual CODEC)
18—12	DEVICE	Device code: 0x0D.
11—0	0x03B	Fixed constant of 0x03B.

Table 35. JTAG ROMCODE Letter Values

ROMCODE Letter	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	V	W
Value	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

Table 36. mwait (External Memory Wait-States Control) Register

Bit	15—12	11—8	7—4	3—0
Field	Res	ERAMHI[3:0]	Res	ERAMLO[3:0]

Bit	Field	Value	Description
15—12	Res	—	Reserved.
11—8	ERAMHI[3:0]	From 0000 to 1111	From zero to 15 ERAMHI wait-states.
7—4	Res	—	Reserved.
3—0	ERAMLO[3:0]	From 0000 to 1111	From zero to 15 ERAMLO wait-states.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 37. phifc (Parallel Host Interface Control) Register

Bit	15—8	7	6	5—4	3	2	1	0
Field	Res	PMUX	PSOBEF	Res	PBSELF	PSTRB	PSTROBE	PMODE

Bit	Field	Value	Description
15—8	Res		Reserved—read as zero, write as zero.
7	PMUX	0	PBSEL input to PHIF internally tied to logic zero (PBSEL input pin ignored and PHIF always enabled). The PBSEL/IOP2 pin is used for the IOP2 function.
		1	PBSEL input pin provides PBSEL input to PHIF. The PBSEL/IOP2 pin is used for the PBSEL function.
6	PSOBEF	0	Normal.
		1	POBE flag as read through PSTAT register is active-low.
5—4	Res		Reserved—read as zero, write as zero.
3	PBSELF		In either mode, PBSEL pin = 0 ≥ **pdx0** low byte. See Table 38.
		0	If PMODE = 0, PBSEL pin = 1 ≥ **pdx0** low byte.
		1	If PMODE = 1, PBSEL pin = 0 ≥ **pdx0** high byte.
2	PSTRB		This bit affects the assertion level of the PDS strobe in *Motorola* mode:
		0	When PSTROBE = 1, PDS active-low.
		1	When PSTROBE = 1, PDS active-high.
1	PSTROBE	0	*Intel* protocol: PIDS and PODS data strobes.
		1	*Motorola* protocol: PRWN and PDS data strobes.
0	PMODE	0	8-bit data transfers.
		1	16-bit data transfers.

Table 38. phifc Register PHIF Function (8-Bit and 16-Bit Modes)

PMODE Field	PSTAT Pin	PBSEL Pin†	PBSELF Field = 0	PBSELF Field = 1	Flag‡
0 (8-bit)	0	0	**pdx0** low byte	Reserved	set
		1	Reserved	**pdx0** low byte	set
	1	0	PSTAT register	Reserved	
		1	Reserved	PSTAT register	
1 (16-bit)	0	0	**pdx0** low byte	**pdx0** high byte	
		1	**pdx0** high byte	**pdx0** low byte	set
	1	0	PSTAT register	Reserved	
		1	Reserved	PSTAT register	

† If bit 7 of the **phifc** register, PMUX, is cleared to zero, the PBSEL input pin is ignored and the PBSEL input to the PHIF section is internally tied to logic zero.

‡ This column indicates the conditions under which the POBE or PIBF flag is set following a read or write of the **pdx0** register. Note that if a reserved condition exists (e.g., PSTAT = PBSEL = 0 and PBSELF = 1) and a read or write operation occurs, no flag is set.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 39. pgreg (Page) Register

Bit	15—0
Field	PAGE

Bit	Field	Description
15—0	PAGE	16-bit page address.

Table 40. PSTAT (PHIF Status) Register

Bit	7—2	1	0
Field	Reserved	PIBF	POBE

Table 41. psw (Processor Status Word) Register

Bit	15—12	11—10	9	8—5	4	3—0
Field	DAU Flags	Res	a1[V]	a1[35:32]	a0[V]	a0[35:32]

Bit	Field	Value	Description
15—12	DAU Flags†	WXXX	LMI—logical minus when set (bit 35 = 1).
		XWXX	LEQ—logical equal when set (bit 35:0 = 0).
		XXWX	LLV—logical overflow when set.
		XXXW	LMV—mathematical overflow when set.
11—10	Res	—	Reserved—read as zero, write as zero.
9	a1[V]	W	Accumulator 1 (**a1**) overflow when set.
8—5	a1[35:32]	WXXX	Accumulator 1 (**a1**) bit 35.
		XWXX	Accumulator 1 (**a1**) bit 34.
		XXWX	Accumulator 1 (**a1**) bit 33.
		XXXW	Accumulator 1 (**a1**) bit 32.
4	a0[V]	W	Accumulator 0 (**a0**) overflow when set.
3—0	a0[35:32]	WXXX	Accumulator 0 (**a0**) bit 35.
		XWXX	Accumulator 0 (**a0**) bit 34.
		XXWX	Accumulator 0 (**a0**) bit 33.
		XXXW	Accumulator 0 (**a0**) bit 32.

† The DAU flags are set by multiply/ALU (F1), conditionals (F2), or ALU (F3) operations involving the accumulators.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 42. sbit (IOP Status Bit) and cbit (IOP Control Bit) Registers

sbit Registers

Bit	15—8	7—0
Field	DIR[7:0]	VALUE[7:0]†

cbit Registers

Bit	15—8	7—0
Field	MODE[7:0]	DATA[7:0]

sbit and cbit Register Fields

DIR[n]‡	MODE[n]‡	DATA[n]‡	Action on IOP[n]‡
1 (Output)	0	0	Clear
1 (Output)	0	1	Set
1 (Output)	1	0	No change
1 (Output)	1	1	Toggle
0 (Input)	x	x	Input

† Read-only. Any value written to this field is ignored.
‡ $0 \le n \le 7$.

Note: Because the **sbit** and **cbit** registers have interrelated fields, and this section lists the register tables alphabetically, Table 42 duplicates the information in Table 29.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 43. sioc (Serial I/O Control) Register

Bit	15	14	13	12	11	10—8	7—5	4	3—2	1—0
Field	DUAL	AOLD	AOCK	OLDP	OLDH	OLD	OCK	MSB	OLEN	ILEN

Bit	Field	Description
15	DUAL	0 = single-channel mode selected. 1 = dual-channel mode selected. The dual-channel mode option is mask-programmable (see Section 11.2 on page 122).
14	AOLD	0 = SLDA is passive. 1 = SLDA is active.
13	AOCK	0 = SCKA is passive. 1 = SCKA is active.
12	OLDP	0 = SLDA has 50% duty cycle (if active). 1 = SLDA is one SCKA clock cycle wide (if active).
11	OLDH	0 = SLDA is active on high-to-low transition. 1 = SLDA is active on low-to-high transition.
10—8	OLD	SLDA frequency (if active): 000 = SCKA ÷ 16. 100 = reserved. 001 = SCKA ÷ 32. 101 = reserved. 010 = SCKA ÷ 256. 110 = reserved. 011 = SCKA ÷ 512. 111 = reserved.
7—5	OCK	SCKA frequency (if active): 000 = f_{XTAL} ÷ 4. 100 = reserved. 001 = f_{XTAL} ÷ 8. 101 = reserved. 010 = f_{XTAL} ÷ 16. 110 = reserved. 011 = reserved. 111 = reserved.
4	MSB	0 = least significant bit (LSB) first. 1 = most significant bit (MSB) first.
3—2	OLEN	Output data length (for channel A only if dual-channel mode selected): 00 = 8 bits. 10 = 32 bits. 01 = 16 bits. 11 = 48 bits.
1—0	ILEN	Input data length (for channel A only if dual-channel mode selected): 00 = 8 bits. 10 = 32 bits. 01 = 16 bits. 11 = reserved.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 44. sioce (Serial I/O Control Extended) Register

Bit	15	14	13	12	11	10—8	7—5	4	3—2	1—0
Field	D50	AILD	AICK	ILDP	ILDH	ILD	ICK	LDD	OLENB	ILENB

Bit	Field	Description
15	D50	If dual-channel mode is selected (see DUAL field of **sioc** register, Table 43): 0 = channel A and B transactions occur back-to-back. 1 = channel B is offset from channel A by 0.5 x (1/channel A load frequency).
14	AILD	0 = SLDB is passive. 1 = SLDB is active.
13	AICK	0 = SCKB is passive. 1 = SCKB is active.
12	ILDP	0 = SLDB has 50% duty cycle (if active). 1 = SLDB is one SCKB clock cycle wide (if active).
11	ILDH	0 = SLDB is active on high-to-low transition. 1 = SLDB is active on low-to-high transition.
10—8	ILD	SLDB frequency (if active): 000 = SCKB ÷ 16. 100 = reserved. 001 = SCKB ÷ 32. 101 = reserved. 010 = SCKB ÷ 256. 110 = reserved. 011 = SCKB ÷ 512. 111 = reserved.
7—5	ICK	SCKB frequency (if active): 000 = f_{XTAL} ÷ 4. 100 = reserved. 001 = f_{XTAL} ÷ 8. 101 = reserved. 010 = f_{XTAL} ÷ 16. 110 = reserved. 011 = reserved. 111 = reserved.
4	LDD	0 = SLDB/SLDA load occurs one clock before first SIO bit. 1 = SLDB/SLDA load occurs with first SIO bit.
3—2	OLENB	For dual-channel mode only, output data length for channel B: 00 = 8 bits. 10 = 32 bits. 01 = 16 bits. 11 = 48 bits.
1—0	ILENB	For dual-channel mode only, input data length for channel B: 00 = 8 bits. 10 = 32 bits. 10 = 16 bits. 11 = reserved.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 45. timerc (Timer Control) Register

Bit	15	14	13	12	11—7	6	5	4	3—0
Field	Res	DISABLE1	RELOAD1	T1EN	Res	DISABLE0	RELOAD0	T0EN	PRESCALE

Bit	Field	Description
15	Res	Reserved—read as zero, write as zero.
14	DISABLE1	0 = Timer1 clocks enabled. 1 = Timer1 clocks off (period register cannot be written with the clock off).
13	RELOAD1	0 = Timer1—Count down and stop. 1 = Timer—Repeat count cycle.
12	T1EN	0 = Timer1—Hold current count. 1 = Timer1—Count toward zero.
11—7	Res	Reserved—read as zero, write as zero.
6	DISABLE0	0 = Timer0 clocks enabled. 1 = Timer0 clocks off (period register cannot be written with the clock off).
5	RELOAD0	0 = Timer0—Count down and stop. 1 = Timer0—Repeat count cycle.
4	T0EN	0 = Timer0—Hold current count. 1 = Timer0—Count toward zero.
3—0	PRESCALE	See Table 46.

Table 46. timerc Register PRESCALE Field

PRESCALE	Frequency	For Example — Period at CKO† = 32.768 MHz
0000	CKO/2	61.0 ns
0001	CKO/4	122.1 ns
0010	CKO/8	244.1 ns
0011	CKO/16	488.3 ns
0100	CKO/32	976.6 ns
0101	CKO/64	1.953 µs
0110	CKO/128	3.906 µs
0111	CKO/256	7.813 µs
1000	CKO/512	15.625 µs
1001	CKO/1024	31.25 µs
1010	CKO/2048	62.5 µs
1011	CKO/4096	125.0 µs
1100	CKO/8192	250.0 µs
1101	CKO/16384	500.0 µs
1110	CKO/32768	1.0 ms
1111	CKO/65536	2.0 ms

† The DSP 1605 68-pin PLCC has no CKO pin. Use either XTALIN1 or XTALIN2.

5 Software Architecture (continued)

5.3 Reset States

Powerup reset occurs when power is applied to the DSP1605. Pin reset occurs when a high-to-low transition is applied to the RSTB pin. The output of the power-loss detect circuit is connected internally to the RSTB pin. Table 47 shows how these resets affect the device. The following bit codes apply to this table:

- Bit code • indicates that this bit is unknown on powerup reset and unaffected on a subsequent pin (RSTB) reset.
- Bit code S indicates that this bit shadows the PC.
- Bit code P indicates that this bit reflects the value on its corresponding input pin. It is unaffected by subsequent pin (RSTB) resets. It is cleared to zero on powerup reset. For the **ins** register, a P indicates that this bit reflects the value on IOP0 or INTB.
- Bit code C indicates that this bit is not changed during pin (RSTB) reset; it holds its previous value.

Table 47. Register States After Reset

Register	Bits 15—0	Register	Bits 15—0	Register	Bits 15—0
a0	•••• •••• •••• ••••	jtag	•••• •••• •••• ••••	rb	0000 0000 0000 0000
a0l	•••• •••• •••• ••••	k	•••• •••• •••• ••••	re	0000 0000 0000 0000
a1	•••• •••• •••• ••••	mwait	1111 1111 1111 1111	sbit	0000 0000 PPPP PPPP
a1l	•••• •••• •••• ••••	p	•••• •••• •••• ••••	sdx0	•••• •••• •••• ••••
alf	00•• •••• •••• ••••	PC	0000 0000 0000 0000	sdx1	•••• •••• •••• ••••
auc	0000 0000 0000 0000	pdx0	0000 0000 0000 0000	sdx2	•••• •••• •••• ••••
c0	•••• •••• •••• ••••	pgreg	•••• •••• •••• ••••	sioc	0000 0000 0000 0000
c1	•••• •••• •••• ••••	phifc	0000 0000 0000 0000	sioce	0000 0000 0000 0000
c2	•••• •••• •••• ••••	pi	SSSS SSSS SSSS SSSS	timer0†	0000 0000 0000 0000
cbit	•••• •••• •••• ••••	pl	•••• •••• •••• ••••	timer1†	0000 0000 0000 0000
cloop	0000 0000 0••• ••••	pr	•••• •••• •••• ••••	timerc	0000 0000 0000 0000
drc	CCCC CCCC CCCC CCCC	psw	•••• 00•• •••• ••••	x	•••• •••• •••• ••••
i	•••• •••• •••• ••••	pt	•••• •••• •••• ••••	y	•••• •••• •••• ••••
inc	0000 0000 0000 0000	r0	•••• •••• •••• ••••	ybase	•••• •••• •••• ••••
ins‡	0011 0101 P101 0010	r1	•••• •••• •••• ••••	yl	•••• •••• •••• ••••
ioc	000C 000C 0000 0000	r2	•••• •••• •••• ••••		
j	•••• •••• •••• ••••	r3	•••• •••• •••• ••••		

† Note that the counters of the timers, but not the timer period registers, are cleared at reset. (An instruction that writes data to **timer<0,1>** loads both the counter and the period register.) The following sequence loads a random count from the period register into the counter, and counts it down:
1. Device reset.
2. Enable timer in RELOAD mode (without writing to **timer<0,1>**).

‡ For the **ins** register, a P indicates that this bit reflects the value on IOP0.

5 Software Architecture (continued)

5.4 Instruction Set Formats

This section defines the hardware-level encoding of the DSP1605 instructions.

5.4.1 Multiply/ALU Instructions

Table 48. Format 1: Multiply/ALU Read/Write Group

Field	T					D	S	F1				X	Y			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 49. Format 1a: Multiply ALU Read/Write Group

Field	T					$\overline{aT}$	S	F1				X	Y			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 50. Format 2: Multiply/ALU Read/Write Group

Field	T					D	S	F1				X	Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 51. Format 2a: Multiply/ALU Read/Write Group

Field	T					$\overline{aT}$	S	F1				X	Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

5.4.2 Special Function Instructions

Table 52. Format 3: F2 ALU Special Functions

Field	T					D	S	F2				CON				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 53. Format 3a: F3 ALU Operations

Field	T					D	S	F3				SRC2		$\overline{aT}$	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

5.4.3 Control Instructions

Table 54. Format 4: Branch Direct Group

Field	T				JA											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

5 Software Architecture (continued)

5.4 Instruction Set Formats (continued)

5.4.3 Control Instructions (continued)

Table 55. Format 5: Branch Indirect Group

Field	T					B			Reserved							0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 56. Format 6: Conditional Branch Qualifier

Field	T					SI	Reserved				CON					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: A branch instruction immediately follows the qualifier.

5.4.4 Data Move Instructions

Table 57. Format 7: Data Move Group

Field	T					$\overline{aT}$	R						Y/Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 58. Format 8: Data Move (16-Bit Immediate Operand—2 Words)

Field	T					D	R						Reserved			
	16-bit Immediate Operand (IM16)															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 59. Format 9: Short Immediate Group

Field	T					I	9-bit Short Immediate Operand (IM9)									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 60. Format 9a: Direct Addressing

Field	T					R/W	DR[3:0]				1	OFFSET				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

5.4.5 Cache Instructions

Table 61. Format 10: Do/Redo

Field	T					NI				K						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

5 Software Architecture (continued)

5.4 Instruction Set Formats (continued)

5.4.6 Field Descriptions

T Field: Specifies the type of instruction.

Table 62. T Field

T	Operation	ALU Type	Format
0000x	goto JA		4
00010	short IM9 j, k, rb, re		9
00011	short IM9 r0, r1, r2, r3		9
00100	Y = a1[l]	F1†	1
00101	Z:aT[l]	F1	2a
00110	Y	F1	1
00111	aT[l] = Y	F1	1a
01000	Bit 0 = 0, aT = R		7
01000	Bit 0 = 1, aTl = R		7
01001	Bit 10 = 0, R = a0		7
01001	Bit 10 = 1, R = a0l		7
01010	R = IM16		8
01011	Bit 10 = 0, R = a1		7
01011	Bit 10 = 1, R = a1l		7
01100	Y = R		7
01101	Z:R		7
01110	Do, Redo		10
01111	R = Y		7
1000x	call JA		4
10010	ifc CON	F2‡	3
10011	if CON	F2	3
10100	Y = y[l]	F1	1
10101	Z:y[l]	F1	2
10110	x = Y	F1	1
10111	y[l] = Y	F1	1
11000	Bit 0 = 0, branch indirect		5
11000	Bit 0 = 1	F3§	3a
11001	y = a0, x = X		1
11010	Conditional branch qualifier		6
11011	y = a1, x = X	F1	1
11100	Y = a0[l]	F1	1
11101	Z:y, x = X	F1	2
11110	Bit 5 = 0, reserved		9a
11110	Bit 5 = 1, direct addressing		9a
11111	y = Y, x = X	F1	1

† See Table 68 on page 66.
‡ See Table 69 on page 66.
§ See Table 70 on page 66.

$\overline{aT}$ Field: Specifies a transfer accumulator.

Table 63. $\overline{aT}$ Field

$\overline{aT}$	Register
0	Accumulator 1
1	Accumulator 0

B Field: Specifies the type of branch instruction.

Table 64. B Field

B	Operation
000	return
001	ireturn
010	goto pt
011	call pt
1xx	Reserved

CON Field: Specifies the condition for special functions and conditional control instructions.

Table 65. CON Field

CON	Condition	CON	Condition
00000	mi	10000	gt
00001	pl	10001	le
00010	eq	10010	Reserved
00011	ne	10011	Reserved
00100	lvs	10100	Reserved
00101	lvc	10101	Reserved
00110	mvs	10110	Reserved
00111	mvc	10111	Reserved
01000	heads	11000	Reserved
01001	tails	11001	Reserved
01010	c0ge	11010	npint
01011	c0lt	11011	njint
01100	c1ge	11100	Reserved
01101	c1lt	11101	Reserved
01110	true	11110	Reserved
01111	false	11111	Reserved

D Field: Specifies a destination register.

Table 66. D Field

D	Register
0	Accumulator 0
1	Accumulator 1

5 Software Architecture (continued)

5.4 Instruction Set Formats (continued)

5.4.6 Field Descriptions (continued)

DR Field: Specifies the data register.

Table 67. DR Field

DR Value	Register
0000	r0
0001	r1
0010	r2
0011	r3
0100	a0
0101	a0l
0110	a1
0111	a1l
1000	y
1001	yl
1010	p
1011	pl
1100	x
1101	pt
1110	pr
1111	psw

F1 Field: Specifies the multiply/ALU function.

Table 68. F1 Field

F1	Operation	
0000	aD = p	p = x * y
0001	aD = aS + p	p = x * y
0010		p = x * y
0011	aD = aS – p	p = x * y
0100	aD = p	
0101	aD = aS + p	
0110	nop	
0111	aD = aS – p	
1000	aD = aS | y	
1001	aD = aS ^ y	
1010	aS & y	
1011	aS – y	
1100	aD = y	
1101	aD = aS + y	
1110	aD = aS & y	
1111	aD = aS – y	

F2 Field: Specifies the special function to be performed.

Table 69. F2 Field

F2	Operation
0000	aD = aS >> 1
0001	aD = aS << 1
0010	aD = aS >> 4
0011	aD = aS << 4
0100	aD = aS >> 8
0101	aD = aS << 8
0110	aD = aS >> 16
0111	aD = aS << 16
1000	aD = p
1001	aDh = aSh + 1
1010	aD = ~aS
1011	aD = rnd(aS)
1100	aD = y
1101	aD = aS + 1
1110	aD = aS
1111	aD = –aS

F3 Field: Specifies the operation in an F3 ALU instruction.

Table 70. F3 Field

F3	Operation
1000	aD = aS[h, l] | (aT, IM16, p)
1001	aD = aS[h, l] ^ (aT, IM16, p)
1010	aS[h, l] & (aT, IM16, p)
1011	aS[h, l] – (aT, IM16, p)
1101	aD = aS[h, l] + (aT, IM16, p)
1110	aD = aS[h, l] & (aT, IM16, p)
1111	aD = aS[h, l] – (aT, IM16, p)

I Field: Specifies a register for short immediate data move instructions.

Table 71. I Field

I	Register
00	r0/j
01	r1/k
10	r2/rb
11	r3/re

5 Software Architecture (continued)

5.4 Instruction Set Formats (continued)

5.4.6 Field Descriptions (continued)

JA Field: 12-bit jump address.

K Field: Number of times the NI instructions in cache are to be executed. Zero specifies use of value in **cloop** register.

NI Field: Number of instructions to be loaded into the cache. Zero implies **redo** operation.

R Field: Specifies the register for data move instructions.

Table 72. R Field

R	Condition	R	Condition
000000	r0	100000	inc
000001	r1	100001	ins
000010	r2	100010	Reserved
000011	r3	100011	Reserved
000100	j	100100	cloop
000101	k	100101	mwait
000110	rb	100110	drc
000111	re	100111	Reserved
001000	pt	101000	cbit
001001	pr	101001	sbit
001010	pi	101010	ioc
001011	i	101011	jtag
001100	p	101100	Reserved
001101	pl	101101	Reserved
001110	Reserved	101110	Reserved
001111	Reserved	101111	Reserved
010000	x	110000	a0
010001	y	110001	a0l
010010	yl	110010	a1
010011	auc	110011	a1l
010100	psw	110100	timerc
010101	c0	110101	timer0
010110	c1	110110	Reserved
010111	c2	110111	Reserved
011000	sioc	111000	Reserved
011001	sioce	111001	Reserved
011010	sdx0	111010	timer1
011011	pgreg	111011	sdx1
011100	phifc	111100	sdx2
011101	pdx0	111101	Reserved
011110	Reserved	111110	Reserved
011111	ybase	111111	alf

R/W Field: A 1 specifies a read, DR = *(OFFSET). A 0 specifies a write, *(OFFSET) = DR.

S Field: Specifies a source accumulator.

Table 73. S Field

S	Register
0	Accumulator 0
1	Accumulator 1

SI Field: Specifies when the conditional branch qualifier instruction should be interpreted as a software interrupt instruction. (Reserved for AT&T hardware development system use.)

Table 74. SI Field

SI	Operation
0	Not a software interrupt
1	Software interrupt

SRC2 Field: Specifies operands in an F3 ALU instruction.

Table 75. SRC2 Field

SRC2	Operands
00	aSl, IM16
01	aSh, IM16
10	aS, aT
11	aS, p

X Field: Specifies the addressing of ROM data in the two-operand multiply/ALU instructions. Specifies the high- or low-half of an accumulator or the **y** register in one-operand multiply/ALU instructions.

Table 76. X Field

X	Operation
Two-Operand Multiply/ALU	
0	*pt++
1	*pt++i
One-Operand Multiply/ALU	
0	aTl, yl
1	aTh, yh

5 Software Architecture (continued)

5.4 Instruction Set Formats (continued)

5.4.6 Field Descriptions (continued)

Y Field: Specifies the form of register-indirect addressing with postmodification.

Table 77. Y Field

Y	Operation
0000	*r0
0001	*r0++
0010	*r0– –
0011	*r0++j
0100	*r1
0101	*r1++
0110	*r1– –
0111	*r1++j
1000	*r2
1001	*r2++
1010	*r2– –
1011	*r2++j
1100	*r3
1101	*r3++
1110	*r3– –
1111	*r3++j

Z Field: Specifies the form of register-indirect compound addressing with postmodification.

Table 78. Z Field

Z	Operation
0000	*r0zp
0001	*r0pz
0010	*r0m2
0011	*r0jk
0100	*r1zp
0101	*r1pz
0110	*r1m2
0111	*r1jk
1000	*r2zp
1001	*r2pz
1010	*r2m2
1011	*r2jk
1100	*r3zp
1101	*r3pz
1110	*r3m2
1111	*r3jk

6 Device Requirements and Characteristics

This section describes DSP1605 device requirements and characteristics.

6.1 Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Absolute Maximum Ratings are the limiting conditions that can be applied to all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded and soldered safely at temperatures of up to 300 °C.

Table 79. Maximum Package Rating Parameters and Values

Parameter	Min	Max	Unit
Voltage on Any Pin with Respect to Ground	–0.5	V_{DD} + 0.5	V
Power Dissipation	—	1	W
Ambient Temperature	–40	85	°C
Storage Temperature	–65	150	°C

6.2 Handling Precautions

All MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. Although input protection circuitry has been incorporated into the devices to minimize the effect of this static build-up, proper precautions should be taken to avoid exposure to electrostatic discharge during handling and mounting.

AT&T employs a human-body model for ESD susceptibility testing. Because the failure voltage of electronic devices is dependent on the current, voltage, and hence, the resistance and capacitance, it is important that standard values be employed to establish a reference by which to compare test data. Values of 100 pF and 1500 Ω are the most common and are the values used in the AT&T human-body model test circuit. The breakdown voltage for the DSP1605 is greater than 2000 V.

6 Device Requirements and Characteristics (continued)

6.3 Recommended Operating Conditions

Table 80. Recommended Voltage and Temperature

Device Speed (T_{MIN})	Temperature Class	Supply Voltage V_{DD} (V)		Ambient Temperature T_A (°C)	
		Min	Max	Min	Max
25 ns	Commercial	4.5	5.5	0	70
30 ns	Industrial	4.5	5.5	–40	85
31.25 ns	Industrial	3.0	3.6	–40	85

6.4 Decoupling Requirements

Install a high-quality ceramic 0.01 pF capacitor between each V_{DD} pin and ground. Install each capacitor as close as possible to the DSP1605 package. Also, install an additional 0.47 µF—1.0 µF capacitor at only one of the V_{DD} pins.

6.5 Package Thermal Considerations

The recommended operating temperature specified in Table 80 is based on the maximum power, package type, and maximum junction temperature. The following equation describes the relationship between these parameters. The maximum power for certain applications may be less than the worst-case value; this relationship can be used to determine the maximum ambient temperature allowed.

$T_A = T_J - P \times \Theta_{JA}$

Maximum Junction Temperature (T_J) . . . . . .125 °C

Maximum Thermal Resistance in Still-air-ambient (Θ_{JA}):

68-pin PLCC. . . . . 43 °C/W
80-pin MQFP . . . . . 58 °C/W

7 Electrical Requirements and Characteristics

The following electrical requirements and characteristics are preliminary and subject to change. Electrical requirements refer to conditions imposed on the user for proper operation of the device. Electrical characteristics refer to the behavior of the device under conditions specified in Section 6, Device Requirements and Characteristics. Tables 81, 82, and 83 describe the valid electrical parameters of these conditions.

Table 81. Electrical Requirements

Parameter	Symbol	V_{DD} = 4.5 V to 5.5 V, T_{MIN} = 25 ns or 30 ns		V_{DD} = 3.0 V to 3.6 V, T_{MIN} = 31.25 ns		Unit
		Min	Max	Min	Max	
Input Voltage (except clocks, INTB, RSTB): Low	V_{IL}	—	0.8	—	0.8	V
High	V_{IH}	2.0	—	2.0	—	V
Input Voltage (INTB): Low	V_{IL}	—	0.6	—	0.6	V
High	V_{IH}	V_{DD} – 0.5	—	V_{DD} – 0.3	—	V
Input Voltage (RSTB): Low	V_{IL}	—	0.5	—	0.5	V
High	V_{IH}	V_{DD} – 0.5	—	V_{DD} – 0.3	—	V

Note: For information about input buffer power dissipation, see Section 7.2.

Table 82. Electrical Characteristics

Parameter	Symbol	V_{DD} = 4.5 V to 5.5 V, T_{MIN} = 25 ns or 30 ns		V_{DD} = 3.0 V to 3.6 V, T_{MIN} = 31.25 ns		Unit
		Min	Max	Min	Max	
Output Low Voltage:						
Low (I_{OL} = 2.0 mA)	V_{OL}	—	0.4	—	0.4	V
Low (I_{OL} = 50 µA)	V_{OL}	—	0.2	—	0.2	V
Output High Voltage:						
High (I_{OH} = –2.0 mA)	V_{OH}	V_{DD} – 0.7	—	V_{DD} – 0.7	—	V
High (I_{OH} = –50 µA)	V_{OH}	V_{DD} – 0.2	—	V_{DD} – 0.2	—	V
Output Tristate Current, V_{DD} = V_{DD} (max): Low (V_{IL} = 0 V)	I_{OZL}	–10	—	–10	—	µA
High [V_{IH} = V_{DD} (max)]	I_{OZH}	—	10	—	10	µA
Schmitt Trigger Hysteresis: INTB	V_{IHL}	300	600	300	600	mV
RSTB	V_{IHL}	1.8	2.2	1.8	2.2	V
VDDPU	V_{IHL}	150	160	280	320	mV
Input Capacitance	C_I	—	10	—	10	pF
Power-loss Detect Circuit:						
Upper Threshold — VDDPU	V_{REC}	3.9	4.5	2.7	3.0	V
Lower Threshold — VDDPU	V_{TRIP}	3.6	4.2	2.5	2.8	V
Slew Rate: VDDPU Rise	—	—	—	1	—	1	V/ms
VDDPU Fall	—	—	—	1	—	1	V/ms
Input Current: VDDPU	I_{PU}	200	320	200	320	µA

7 Electrical Requirements and Characteristics (continued)

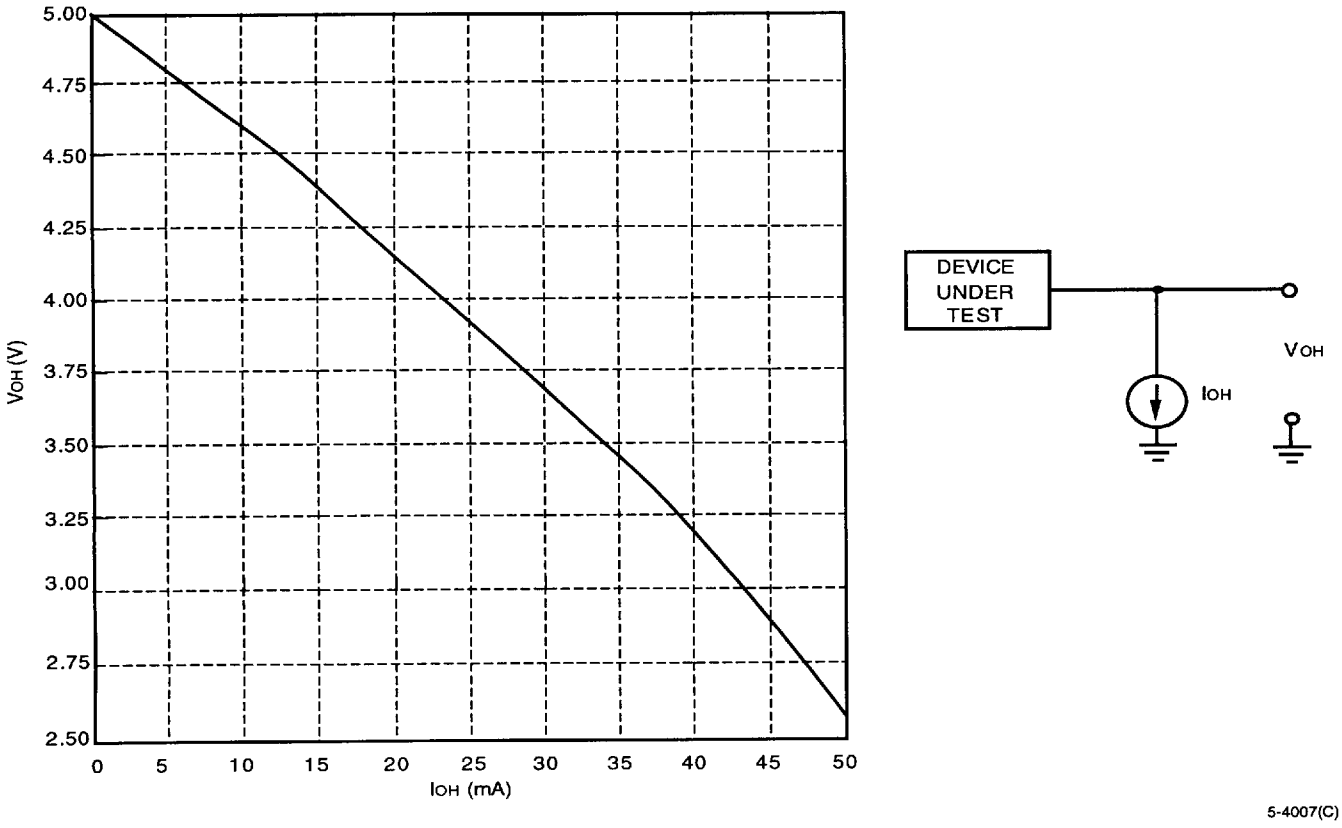


Figure 12. Plot of V_{OH} vs. I_{OH} Under Typical Operating Conditions

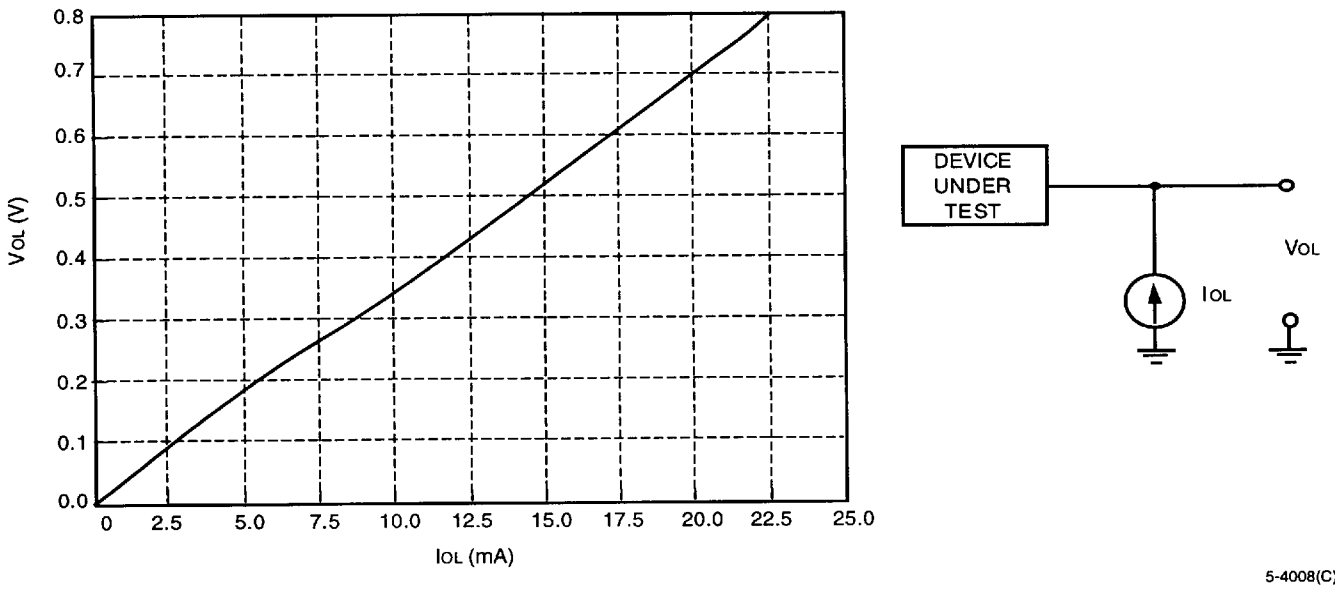


Figure 13. Plot of V_{OL} vs. I_{OL} Under Typical Operating Conditions

7 Electrical Requirements and Characteristics (continued)

Table 83. Electrical Requirements for Clocks

	Parameter	Symbol	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
			T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
			Min	Max	Min	Max	Min	Max	
High-frequency Crystal†	XTAL1IN Input Voltage: Low	V_{IL}	—	0.6	—	0.6	—	0.6	V
	XTAL1IN Input Voltage: High	V_{IH}	V_{DD} – 0.5	—	V_{DD} – 0.5	—	V_{DD} – 0.3	—	V
	Frequency Range of Fundamental Mode Crystal	fx	5	40	5	33	5	32	MHz
	Series Resistance of Fundamental Mode Crystal (pins: XTAL1IN, XTAL1OUT)	Rs	—	40	—	40	—	40	Ω
	Mutual Capacitance of Fundamental Mode Crystal (includes board parasitic capacitance)	Co	—	7	—	7	—	7	pF
Low-frequency Crystal‡	XTAL2IN Input Voltage: Low	V_{IL}	—	0.5	—	0.5	—	0.5	V
	XTAL2IN Input Voltage: High	V_{IH}	V_{DD} – 0.5	—	V_{DD} – 0.5	—	V_{DD} – 0.3	—	V
	Frequency Range of Fundamental Mode Crystal	fx	100	600	100	600	100	600	kHz
	Series Resistance of Fundamental Mode Crystal (pins: XTAL2IN, XTAL2OUT)	Rs	—	100	—	100	—	100	Ω
	Mutual Capacitance of Fundamental Mode Crystal (includes board parasitic capacitance)	Co	—	500	—	500	—	500	pF

† If the external crystal option has been chosen, connect an external capacitor between each pad (XTAL1IN and XTAL1OUT) and ground. $C_1 = C_2 = 30$ pF.

‡ If the low-frequency crystal option has been chosen, connect an external capacitor between each crystal lead and ground. $C_1 = C_2 = 150$ pF. Also, the user must install two resistors. Connect one resistor between pin XTAL2IN and one of the crystal's leads; $R_S = 500\ \Omega$. Connect another resistor between the two crystal leads; $R_f = 10\ M\Omega$.

Note: For more information about crystal oscillators, see Section 9, Crystal Oscillator Electrical Requirements and Characteristics.

7 Electrical Requirements and Characteristics (continued)

7.1 Typical Power Dissipation

Power dissipation is highly dependent on program activity and the frequency of operation. Table 84 lists typical power dissipation for a selected application. These electrical characteristics are preliminary and are subject to change. The power dissipation listed in Table 84 is for internal power dissipation only with VDDPU connected to ground and the I/O pins at quiescent levels.

Table 84. Internal Power Dissipation

Power Dissipation Parameter	XTAL1	Register Contents			Timers	fXTAL1IN (MHz)	fXTAL2IN (kHz)	VDD (V)	Typical Value	Unit
		ioc	alf	timerc						
Active†	Enabled	0x0C00	—	—	—	40	512	5.0	367	mW
						33	512	5.0	310	mW
								3.3	121	mW
Low-power Standby	Disabled	0x3C00	0xC000	0x4040	Off	—	512	5.0	3.0	mW
								3.3	0.4	mW
				0x3036	On	—	512	5.0	6.5	mW
								3.3	1.8	mW
Reset‡	—	—	—	—	—	0	0	5.0	TBD	mW
								3.3	TBD	mW

† Active power dissipation is measured while the DSP is executing an FIR filter program from one bank of memory.
‡ RSTB active (held low).

Total power dissipation can be calculated on the basis of the application by adding C x V_{DD}^2 x f x p for each output, where C is the additional load capacitance, f is the frequency of the output, and p is the percentage of activity.

7.2 Input and I/O Buffer Power Dissipation

Power dissipation due to the input and I/O buffers is highly dependent on the input voltage level. At full CMOS levels, essentially no dc current is drawn. However, for levels near the threshold of 1.4 V, high current can flow. Therefore, all unused input pins should be tied inactive to VDD or VSS, and all unused I/O pins should be tied inactive through a 10 kΩ resistor to VDD or VSS. Tables 85 and 86 show the input buffer power dissipation for 43 inputs biased at dc level, VIN, with VDD at 5.0 V.

Table 85. Input Buffer Maximum Power Dissipation

VIN (V)	5.0	3.6	2.8	2.4	2.0	1.4	0.8	0.4	0
PD (mW)	<1.0	13.5	140	180	180	High	80	7.5	<1.0

WARNING: The device needs to be clocked for at least six fXTAL1 cycles during reset after powerup; otherwise, high current may flow.

Table 86. Schmitt Trigger Input Buffer Maximum Power Dissipation

VIN (V)	5.0	3.6	2.8	2.4	2.0	1.4	0.8	0.4	0
PD (mW)	<1.0	13.5	140	180	180	180	80	7.5	<1.0

8 Timing Requirements and Characteristics

Requirements are restrictions on the external device connected to the DSP1605. Characteristics are properties of the DSP1605. For details, see Section 6, Device Requirements and Characteristics, and Section 7, Electrical Requirements and Characteristics.

The characteristics listed are valid under the following conditions:

- V_{SS} = 0 V, V_{DD} = 5.0 V ± 0.5 V, T_A = 0 °C to 70 °C, C_{LOAD} = 50 pF, T_{MIN} = 25 ns
- V_{SS} = 0 V, V_{DD} = 5.0 V ± 0.5 V, T_A = –40 °C to +85 °C, C_{LOAD} = 50 pF, T_{MIN} = 30 ns
- V_{SS} = 0 V, V_{DD} = 3.3 V ± 0.3 V, T_A = –40 °C to +85 °C, C_{LOAD} = 50 pF, T_{MIN} = 31.25 ns

Output characteristics can be derated as a function of load capacitance (C_L):

- For all rising edge outputs, $dt/dC_L \le 0.06$ ns/pF for $0 \le C_L \le 100$ pF at 2.0 V
- For all falling edge outputs, $dt/dC_L \le 0.05$ ns/pF for $0 \le C_L < 100$ pF at 0.8 V

For example, the derating for a time delay that includes a rising edge with an external load of 20 pF is as follows:

$$\Delta t = (C_L - C_{LOAD})\ dt/dC_L = (20 - 50)\ 0.06 = -1.8 \text{ ns}$$

Table 87. Test Conditions

Test Conditions for Inputs	Test Conditions for Outputs
Rise and fall times of 4 ns or less.	C_{LOAD} = 50 pF.
Timing reference levels for delays = V_{IH}, V_{IL}.	Timing reference levels for delays = V_{OH}, V_{OL}. Tristate delays are measured to the high-impedance state of the output driver.

For definitions of the V_{IH}, V_{IL}, V_{OH}, and V_{OL} labels, see Table 81 on page 71. In this section's timing diagrams, these labels distinguish inputs and outputs.

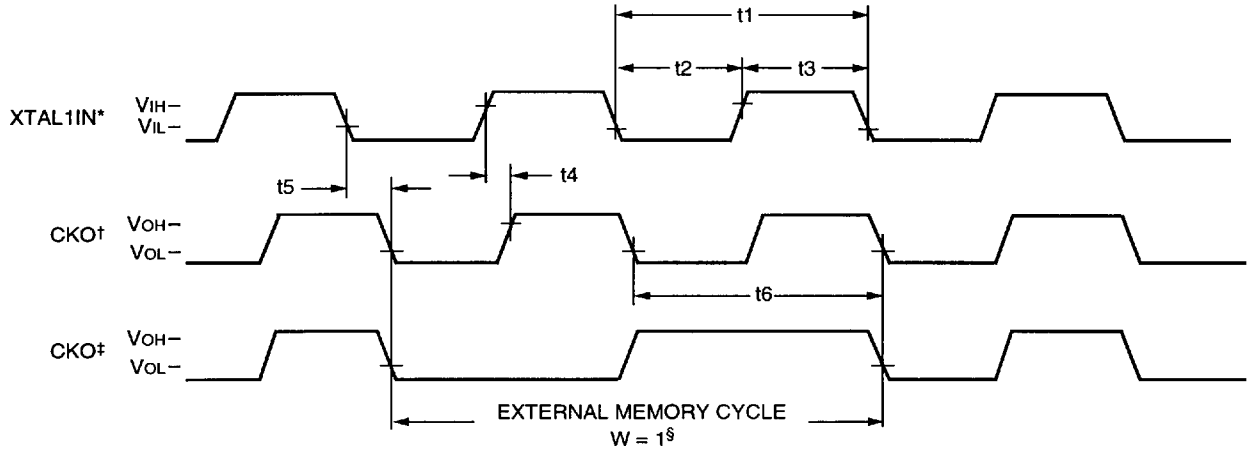
8.1 Input Clock Options

The input clocks to the DSP1605 allow for the use of either CMOS level input signals or an internal crystal oscillator with an external crystal. This allows the user to select either both clock inputs to use the internal crystal oscillators, one clock input to use the internal oscillator and the other to have a CMOS level external input, or both clock inputs driven by external CMOS level clock signals.

Note: In the following sections, all timing requirements and characteristics are given for the three device speed options, T_{MIN} = 25 ns, T_{MIN} = 30 ns, and T_{MIN} = 31.25 ns, where T_{MIN} is the minimum instruction cycle time (see Table 83 on page 73).

8 Timing Requirements and Characteristics (continued)

8.2 DSP Clock Generation



5-4009(C)

* If the low-speed clock is selected, the signal shown is XTAL2IN.
† Free-running clock; CKO may be inverted with respect to XTAL1IN.
‡ Wait-stated clock.
§ W = number of wait-states.
Note: The CKO pin is available only on the 80-pin MQFP package.

Figure 14. I/O Clock Timing Diagram

Note: For Tables 88 to 131, TMIN is the minimum instruction cycle time (see Section 8.1 on page 75).

Table 88. Timing Requirements for Input Clock

Ref	Parameter	VDD = 4.5 V to 5.5 V				VDD = 3.0 V to 3.6 V		Unit
		TMIN = 25 ns		TMIN = 30 ns		TMIN = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t1	Clock In Period (low to low)	25	—*	30	—*	31.25	—*	ns
t2	Clock In Low Time (low to high)	11	—	13	—	14	—	ns
t3	Clock In High Time (high to low)	11	—	13	—	14	—	ns

* Device is fully static; t1 is tested at 125 ns, and memory hold time is tested at 0.1 s.

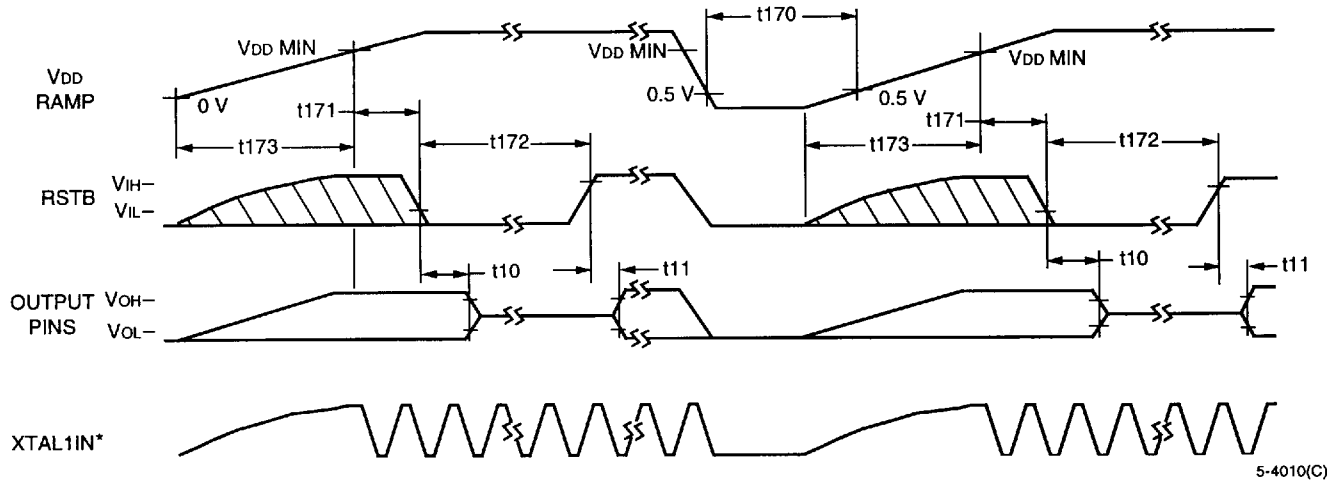
Table 89. Timing Requirements for Input Clock and Output Clock

Ref	Parameter	VDD = 4.5 V to 5.5 V				VDD = 3.0 V to 3.6 V		Unit
		TMIN = 25 ns		TMIN = 30 ns		TMIN = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t4	Clock Out High Delay (high to high)	—	21	—	24	—	25	ns
t5	Clock Out Low Delay (low to low)	—	21	—	24	—	25	ns
t6	Clock Out Period (low to low)	25	—	30	—	31.25	—	ns

8 Timing Requirements and Characteristics (continued)

8.3 Powerup Reset (Assuming VDDPU Is Disabled)

The DSP1605 has a powerup reset circuit that automatically clears the JTAG controller upon powerup. If the supply voltage falls below the V_{DD} minimum value, a reset is required—the JTAG controller must be reset with another powerup reset, followed by the usual RSTB and XTAL1IN reset sequence (see the Warning in Section 7.2). Figure 15 shows two separate events: an initial powerup and a powerup following a drop in the power supply.



* See Table 83 for input clock electrical requirements.

Figure 15. Powerup Reset and Device Reset Timing Diagram

8 Timing Requirements and Characteristics (continued)

8.3 Powerup Reset (continued)

Note: In Table 90, T = the period of XTAL1IN (t1).

Table 90. Timing Requirements for Powerup Reset and Device Reset

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t172	Reset Pulse (low to high)	6T	—	6T	—	6T	—	ns
t173	V_{DD} Ramp	—	40	—	40	—	40	ms
t170	V_{DD} Low*	3	—	3	—	3	—	s
t171	V_{DD} MIN to RSTB Low (with input clock driven externally)	0	—	0	—	0	—	ms
t171	V_{DD} MIN to RSTB Low (with crystal oscillator input clock option†)	20	—	20	—	20	—	ms

* Time below 0.5 V required to activate the internal powerup reset circuit that resets the JTAG controller. Following a reset of the JTAG controller, the device must also be reset with the usual RSTB and XTAL1IN sequence.
† With external components as specified in Table 83 on page 73.

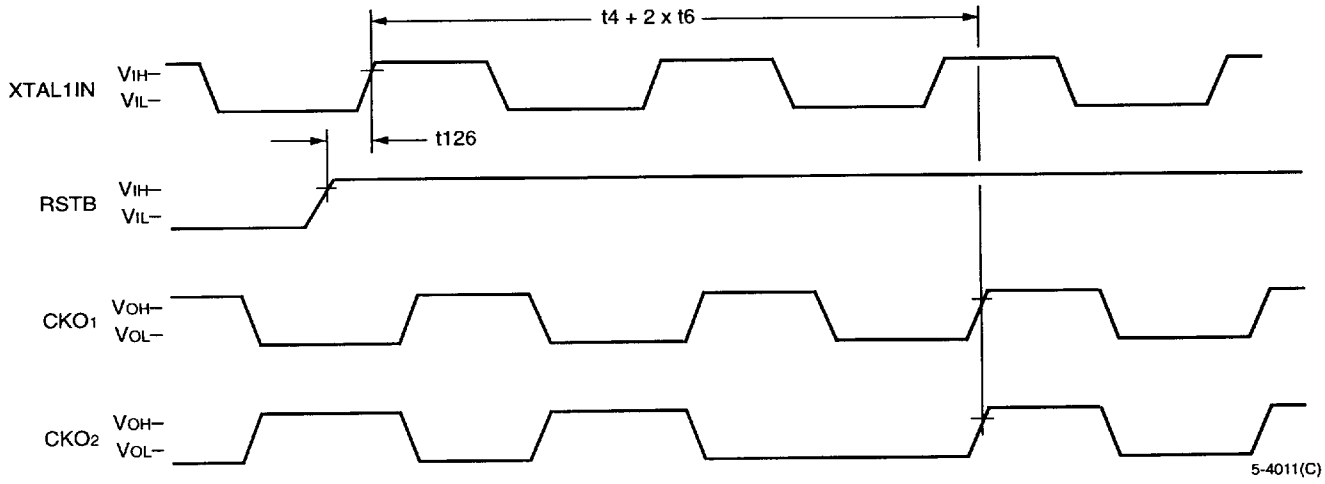
Table 91. Timing Characteristics for Powerup Reset and Device Reset

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t10	RSTB Disable Time (low to tristate)	—	100	—	100	—	100	ns
t11	RSTB Enable Time (high to valid)	—	100	—	100	—	100	ns

WARNING: The device needs to be clocked for at least six f_{XTAL1} cycles during reset after powerup; otherwise, high current may flow.

8 Timing Requirements and Characteristics (continued)

8.4 Reset Synchronization



Note: The CKO pin is available only on the 80-pin MQFP package.

Figure 16. Reset Synchronization Timing

Note: In Figure 16, CKO1 and CKO2 are two possible CKO states before reset. CKO is free-running after reset.

Table 92. Timing Requirements and Characteristics for Reset Synchronization Timing

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t126	Reset Setup (high to high)	10	—	10	—	10	—	ns
t4	Clock Out High Delay (high to high)	—	19	—	24	—	25	ns
t6	Clock Out Period (low to low)	25	—	30	—	31.25	—	ns

8.5 Powerup and Power-Loss Detect Circuit Reset

The DSP1605 has an alternate powerup reset and power-loss detect circuit that automatically clears the JTAG and DRAM controllers, the DSP1600 core, and the remaining internal peripherals. This circuit functions properly with fast power supply ramps and quick power supply drops and recoveries. A powerup reset is considered the condition that the DSP power supply ramps from 0 V to its operating voltage. A power-loss detect reset is considered the condition in which the DSP is operating at a proper voltage and then DSP power supply drops below maximum V_{TRIP} (see Table 95). The DSP stays in full-device reset until the DSP power supply rises at least 300 mV above the V_{TRIP} point.

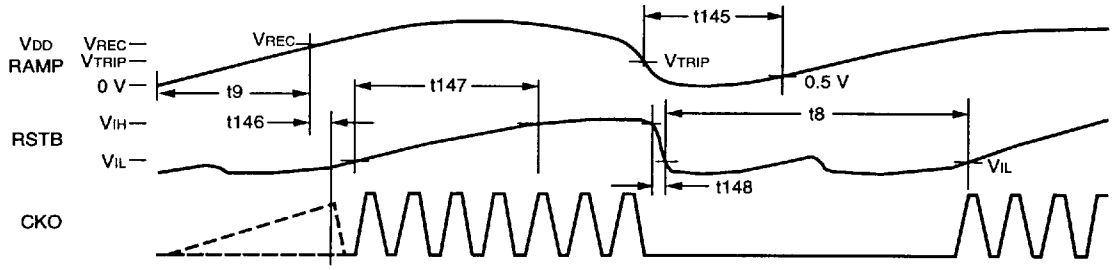
The power-loss detect circuit is enabled by connecting the VDDPU pin to the power supply, V_{DD}. If the supply voltage falls below the minimum required value, the bidirectional RSTB has an open-drain output that is pulled low. The power-loss detect circuit is disabled by connecting the VDDPU pin to ground.

8 Timing Requirements and Characteristics (continued)

8.5 Powerup and Power-Loss Detect Circuit Reset (continued)

The RSTB pin is internally connected to the VDDPU power-loss detect circuit. With proper external components, the power-loss detect circuit can be tunable for use as an automatic powerup reset and a power-loss detect circuit. This external circuit must detect the power-loss condition from the RSTB pin and enable it for its low duration and at least 3T after it returns high. (T is the period of the free-running CKO.) Figure 18 shows an RC network configuration that can fulfill all necessary RSTB timing requirements.

8.5.1 Powerup Reset Specifications (VDDPU Connected to VDD)



5-4012(C).a

Note: The CKO pin is available only on the 80-pin MQFP package.

Figure 17. Powerup Reset

Note: In Figure 17, VDDPU is enabled. RSTB timing determined by an RC network. See Figure 18.

Table 93. Timing Requirements for Powerup Reset with VDDPU Enabled

Ref	Parameter	VDD = 4.5 V to 5.5 V				VDD = 3.0 V to 3.6 V		Unit
		TMIN = 25 ns		TMIN = 30 ns		TMIN = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t8	Powerup Reset Pulse	50	—	50	—	50	—	ms
t9	VDD Ramp	500	—	500	—	500	—	µs
t145	VDD Low	200	—	200	—	200	—	µs

Table 94. Timing Characteristics for Powerup Reset with VDDPU Enabled

Ref	Parameter	VDD = 4.5 V to 5.5 V				VDD = 3.0 V to 3.6 V		Unit
		TMIN = 25 ns		TMIN = 30 ns		TMIN = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t146	VREC to PURSTO High (internal)	0	20	0	20	0	20	ns
t147	RSTB Ramp (low to high)	50	500	50	500	50	500	ms
t148	RSTB Ramp (high to low)	—	500	—	500	—	500	µs

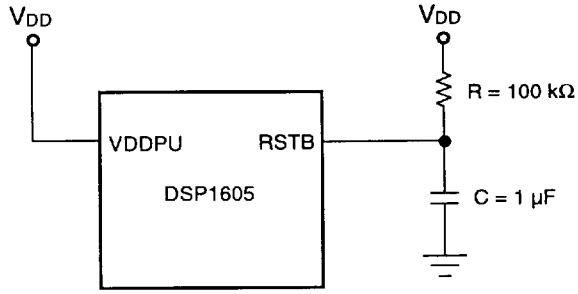
8 Timing Requirements and Characteristics (continued)

8.5 Powerup and Power-Loss Detect Circuit Reset (continued)

8.5.1 Powerup Reset Specifications (continued)

Table 95. Power-Loss Detect Voltage Levels

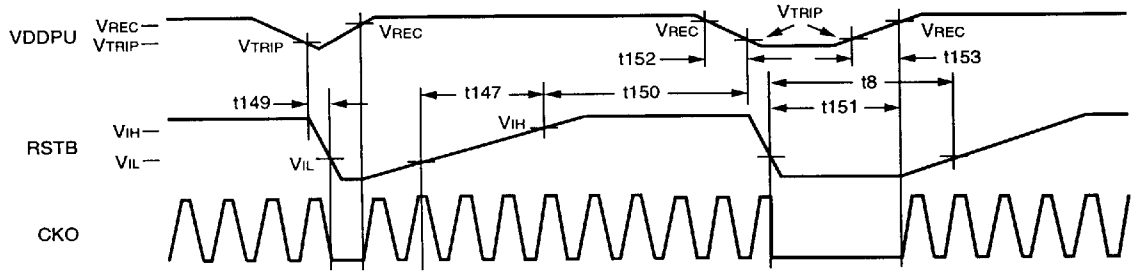
Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
V_{TRIP}	Power-loss Detect Enable Point	3.6	4.2	3.6	4.2	2.50	2.90	V
V_{REC}	Power-loss Detect Disable Point	3.9	4.5	3.9	4.5	2.65	3.05	V



5-4013(C).a

Figure 18. Example of Power-Loss Detect External Component Configuration

8.5.2 Power-Loss Detect Specifications (VDDPU Not Connected to V_{DD})



5-4014(C).a

Note: The CKO pin is available only on the 80-pin MQFP package.

Figure 19. Power-Loss Detect Reset

Note: In Figure 19, VDDPU is enabled (connected to V_{DD} from a separate, independent supply). RSTB timing is determined by an RC network. See Figure 18.

8 Timing Requirements and Characteristics (continued)

8.5 Powerup and Power-Loss Detect Circuit Reset (continued)

8.5.2 Power-Loss Detect Specifications (continued)

Table 96. Timing Requirements for Powerup Reset with VDDPU Enabled

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t8	Reset Pulse	50	—	50	—	50	—	ms
t150	RSTB High to V_{TRIP} Setup	0	—	0	—	0	—	ns
t151	PURSTO Low to V_{REC} Setup	20	—	20	—	20	—	ns
t152	VDDPU Fall Rate	200	—	200	—	200	—	µs/V
t153	VDDPU Rise Rate	200	—	200	—	200	—	µs/V

Table 97. Timing Characteristics for Powerup Reset with VDDPU Enabled

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t147	RSTB Ramp (low to high)	50	500	50	500	50	500	ms
t149	V_{TRIP} to RSTB Low	0.02	500	0.02	500	0.02	500	µs

8 Timing Requirements and Characteristics (continued)

8.6 JTAG I/O Specifications

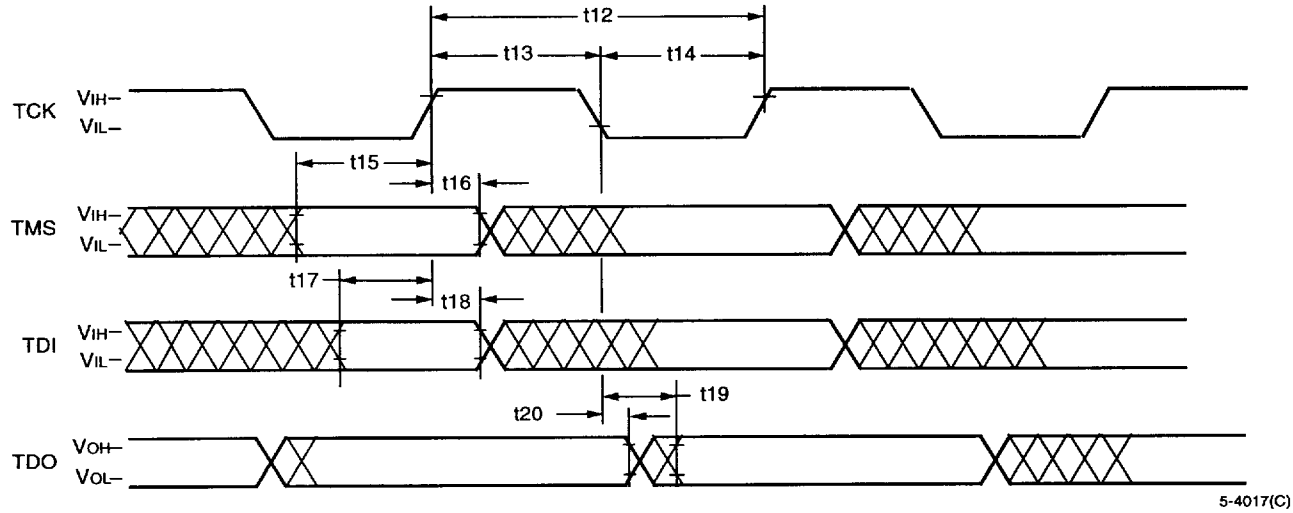


Figure 20. JTAG Timing Diagram

Table 98. Timing Requirements for JTAG Input/Output

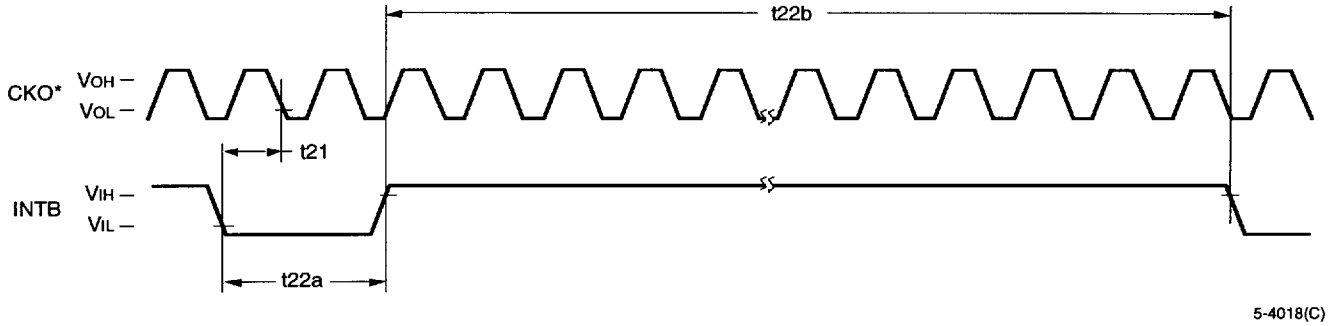
Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t12	TCK Period (high to high)	50	—	60	—	62.5	—	ns
t13	TCK High Time (high to low)	22	—	27	—	28	—	ns
t14	TCK Low Time (low to high)	22	—	27	—	28	—	ns
t15	TMS Setup Time (valid to high)	7	—	10	—	11	—	ns
t16	TMS Hold Time (high to invalid)	0	—	0	—	0	—	ns
t17	TDI Setup Time (valid to high)	7	—	10	—	11	—	ns
t18	TDI Hold Time (high to invalid)	0	—	0	—	0	—	ns

Table 99. Timing Characteristics for JTAG Input/Output

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t19	TDO Delay (low to valid)	—	22	—	25	—	26	ns
t20	TDO Hold (low to invalid)	0	—	0	—	0	—	ns

8 Timing Requirements and Characteristics (continued)

8.7 Interrupt



* CKO is free-running.
Note: The CKO pin is available only on the 80-pin MQFP package.

Figure 21. Interrupt Timing Diagram

Note: Interrupt is asserted during an interruptible instruction and no other pending interrupts.

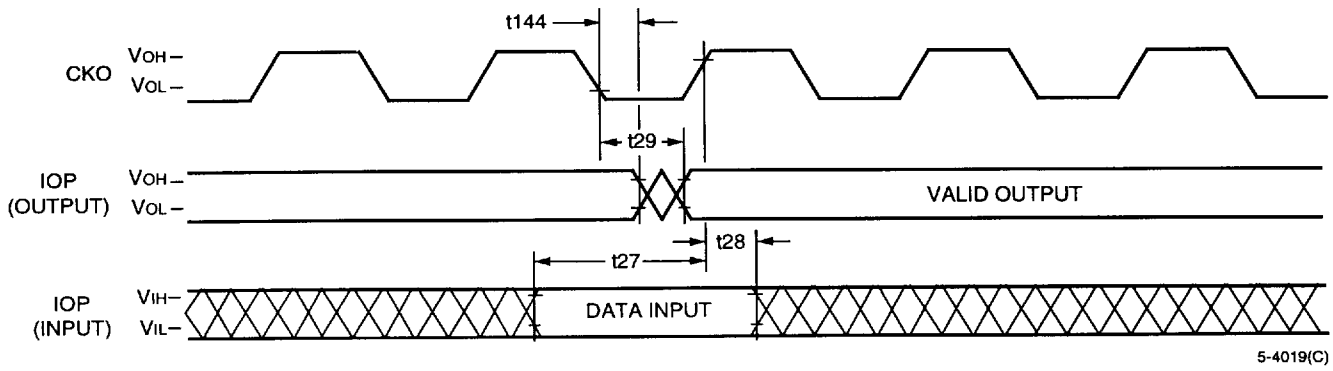
Table 100. Timing Requirements for Interrupt

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t21	Interrupt Setup (low to low)	17	—	19	—	20	—	ns
t22a	INTB Assertion Time (low to high)	2T	—	2T	—	2T	—	ns
t22b	INTB Deassertion Time (high to low)	2T	—	2T	—	2T	—	ns

Note: In Table 100, T = the period of the free-running clock, CKO.

8 Timing Requirements and Characteristics (continued)

8.8 Input/Output Ports (IOP)



Note: The CKO pin is available only on the 80-pin MQFP package.

Figure 22. Write Outputs Followed by Read Inputs (cbit = Immediate; a1 = sbit)

Table 101. Timing Requirements for IOP Input Read

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t27	IOP Input Setup Time (valid to high)	20	—	20	—	20	—	ns
t28	IOP Input Hold Time (high to invalid)	—	0	—	0	—	0	ns

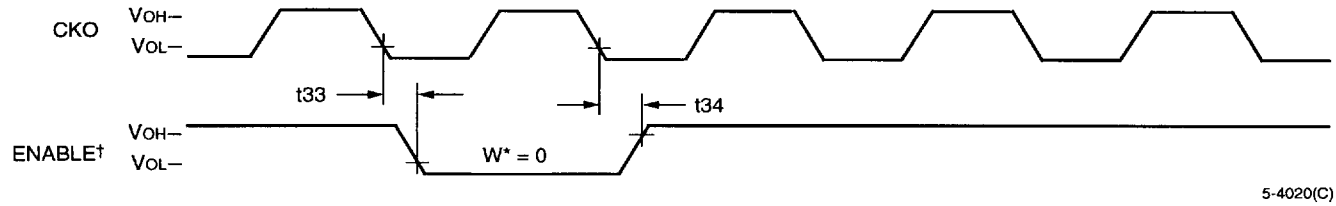
Table 102. Timing Characteristics for IOP Output

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t29	IOP Output Valid Time (low to valid)	—	4	—	5	—	6	ns
t144	IOP Output Hold Time (low to invalid)	–4	—	–5	—	–6	—	ns

8 Timing Requirements and Characteristics (continued)

8.9 External Memory Interface

The following timing diagrams, characteristics, and specifications do not apply to interactions with delayed external memory enables unless otherwise stated. See the *DSP160X Digital Signal Processor Information Manual* for a more detailed description of the external memory interface, including complete functional diagrams.



* W = number of wait-states selected through the **mwait** register.
† ENABLE is any one of the memory segment enable signals, ERAMHI or ERAMLO.
Note: The CKO pin is available only on the 80-pin MQFP package.

Figure 23. Enable Transition Timing

Table 103. Timing Characteristics for External Memory Enables (ERAMHI or ERAMLO)

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t33	Enable Assert (low to low)	0	4	0	5	0	6	ns
t34	Enable Deassert (low to high)	0	4	0	5	0	6	ns

Table 104. Timing Characteristics for Delayed External Memory Enables (ioc = 0x000F)

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t33	Delayed Enable Assert Time	T/2	T/2 + 9	T/2	T/2 + 9	T/2	T/2 + 9	ns

Note: In Table 104, T = the period of the free-running clock, CKO.

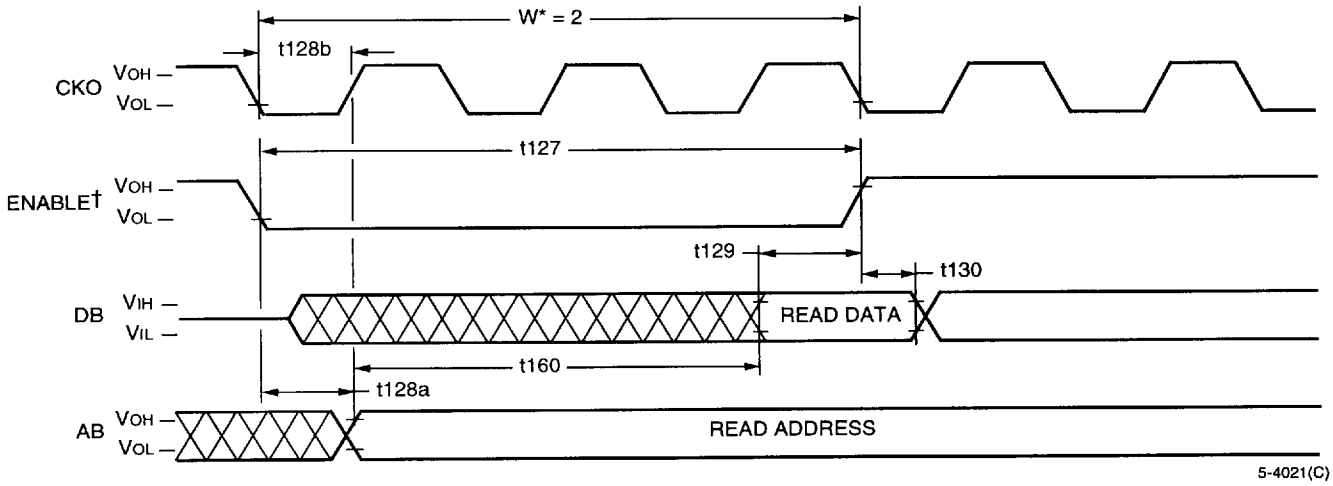
Table 105. Timing Characteristics for Delayed Device Enable (ioc = 0x0010)

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t33	Delayed Enable Assert Time	T/2	T/2 + 10	T/2	T/2 + 10	T/2	T/2 + 10	ns

Note: In Table 105, T = the period of the free-running clock, CKO.

8 Timing Requirements and Characteristics (continued)

8.9 External Memory Interface (continued)



* W = number of wait-states selected through the **mwait** register.
† ENABLE indicates any one of the memory segment enable signals, ERAMHI or ERAMLO.
Note: The CKO pin is available only on the 80-pin MQFP package.

Figure 24. External Memory Data Read Timing Diagram

Table 106. Timing Characteristics for External Memory Access

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t127	Enable Width (low to high)	T(1 + W) – 1	—	T(1 + W) – 1	—	T(1 + W) – 1	—	ns
t128a	Address Valid (enable low to valid)	—	1	—	1	—	1	ns
t128b	Address Valid (CKO low to valid)	—	1	—	1	—	1	ns

Note: In Table 106: T = the period of the free-running clock, CKO.
W = the number of wait-states selected through the **mwait** register.

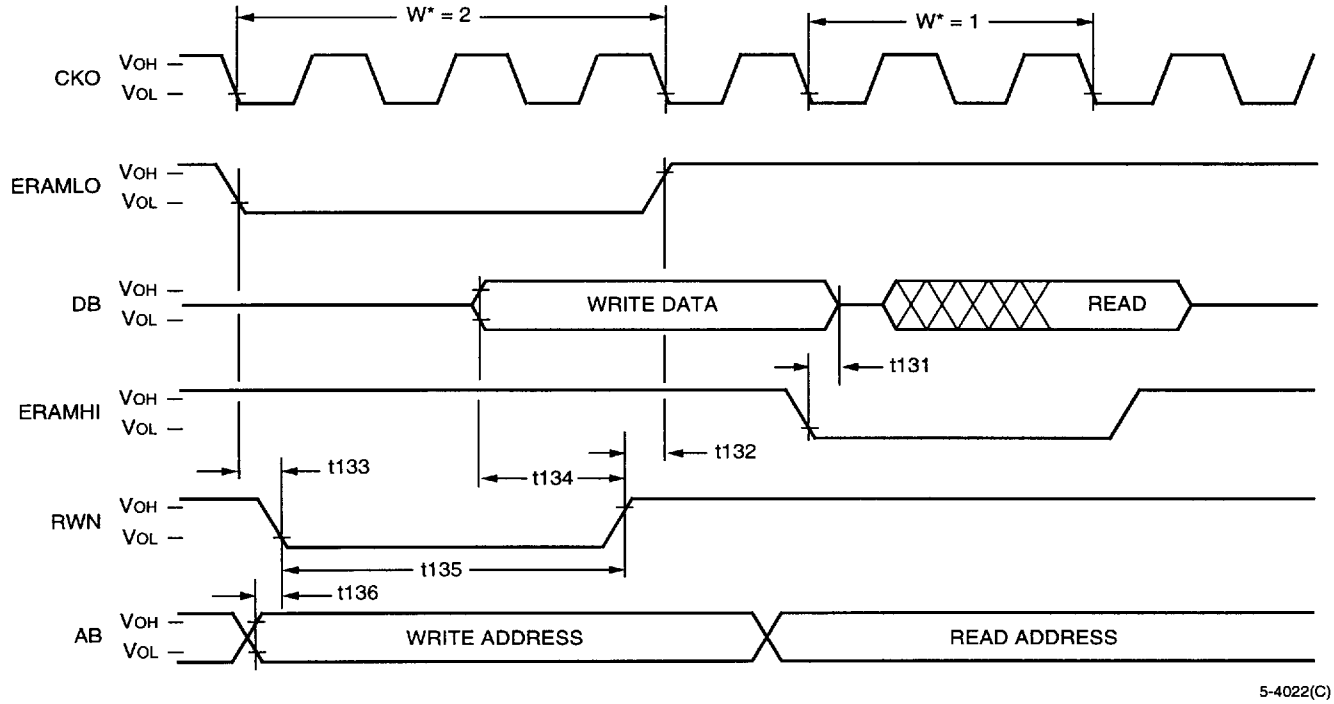
8 Timing Requirements and Characteristics (continued)

8.9 External Memory Interface (continued)

Table 107. Timing Requirements for External Memory Read (ERAMHI or ERAMLO)

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t129	Read Data Setup (valid to enable high)	17	—	17	—	17	—	ns
t130	Read Data Hold (enable high to hold)	0	—	0	—	0	—	ns
T160	External Memory Access Time (valid to valid)	—	T(1 + W) – 17	—	T(1 + W) – 17	—	T(1 + W) – 17	ns

Note: In Table 107: T = the period of the free-running clock, CKO.
W = the number of wait-states selected through the **mwait** register.



* W = number of wait-states selected through the **mwait** register. In this example, ERAMLO is programmed for two wait-states and ERAMHI is programmed for one wait-state (**mwait** = 0x0102).

Note: The CKO pin is available only on the 80-pin MQFP package.

Figure 25. External Memory Data Write, Read Timing Diagram

8 Timing Requirements and Characteristics (continued)

8.9 External Memory Interface (continued)

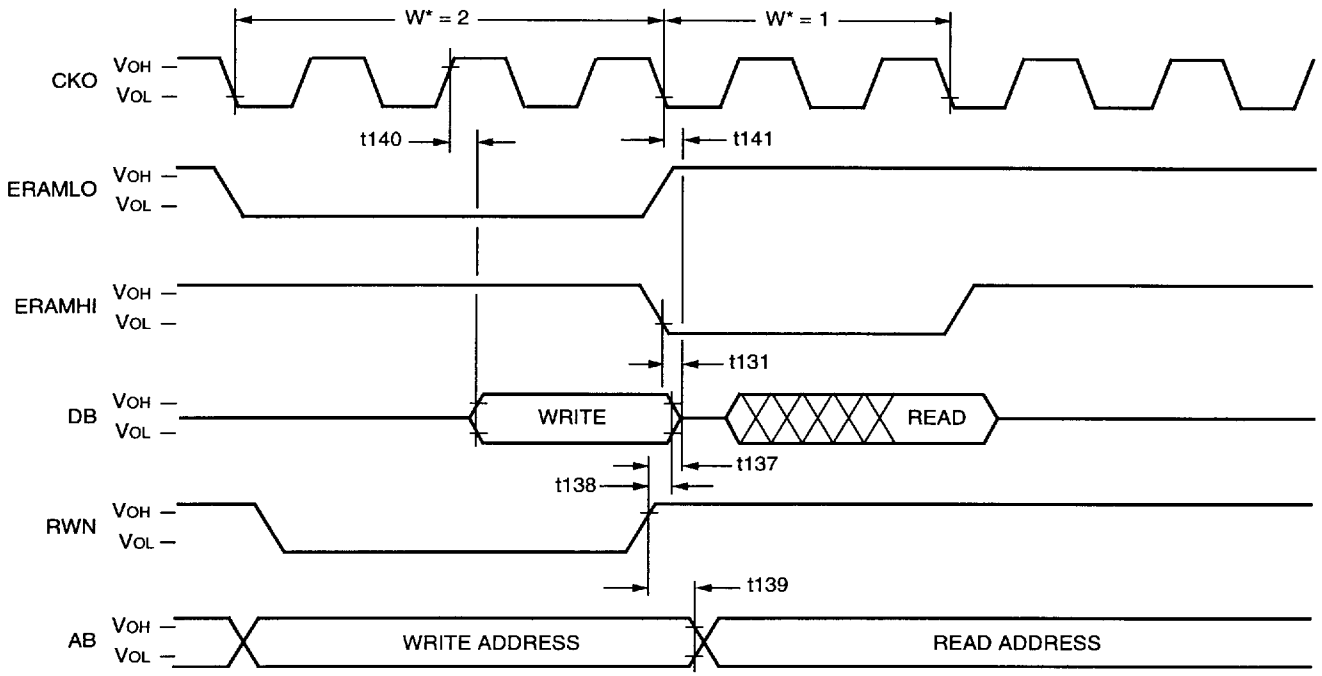
Table 108. Timing Characteristics for External Memory Data Write (All Enables)

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t131	Write Overlap (enable low to tristate)	—	0	—	0	—	0	ns
t132	RWN Advance (RWN high to enable high)	0	—	0	—	0	—	ns
t133	RWN Delay (enable low to RWN low)	0	—	0	—	0	—	ns
t134	Write Data Setup (data valid to RWN high)	T(1 + W)/2 – 10	—	T(1 + W)/2 – 10	—	T(1 + W)/2 – 10	—	ns
t135	RWN Width (low to high)	T(1 + W) – 8	—	T(1 + W) – 8	—	T(1 + W) – 8	—	ns
t136	Write Address Setup (address valid to RWN low)	0	—	0	—	0	—	ns

Note: In Table 108: T = the period of the free-running clock, CKO.
W = the number of wait-states selected through the **mwait** register.

8 Timing Requirements and Characteristics (continued)

8.9 External Memory Interface (continued)



* W = number of wait-states selected through the **mwait** register. In this example, ERAMLO is programmed for two wait-states and ERAMHI is programmed for one wait-state (**mwait** = 0x0102).

Note: The CKO pin is available only on the 80-pin MQFP package.

Figure 26. Write Cycle Followed by Read Cycle

Table 109. Timing Characteristics for Write Cycle Followed by Read Cycle

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t137	Write Data Tristate (RWN high to tristate)	—	2	—	2	—	2	ns
t138	Write Data Hold (RWN high to data hold)	0	—	0	—	0	—	ns
t139	Write Address Hold (RWN high to address hold)	0	—	0	—	0	—	ns
t140	Write Data Valid (CKO high to valid)	0	—	0	—	0	—	ns
t141	Write Data Tristate (CKO low to tristate)	0	—	0	—	0	—	ns

8 Timing Requirements and Characteristics (continued)

8.10 External DRAM Interface

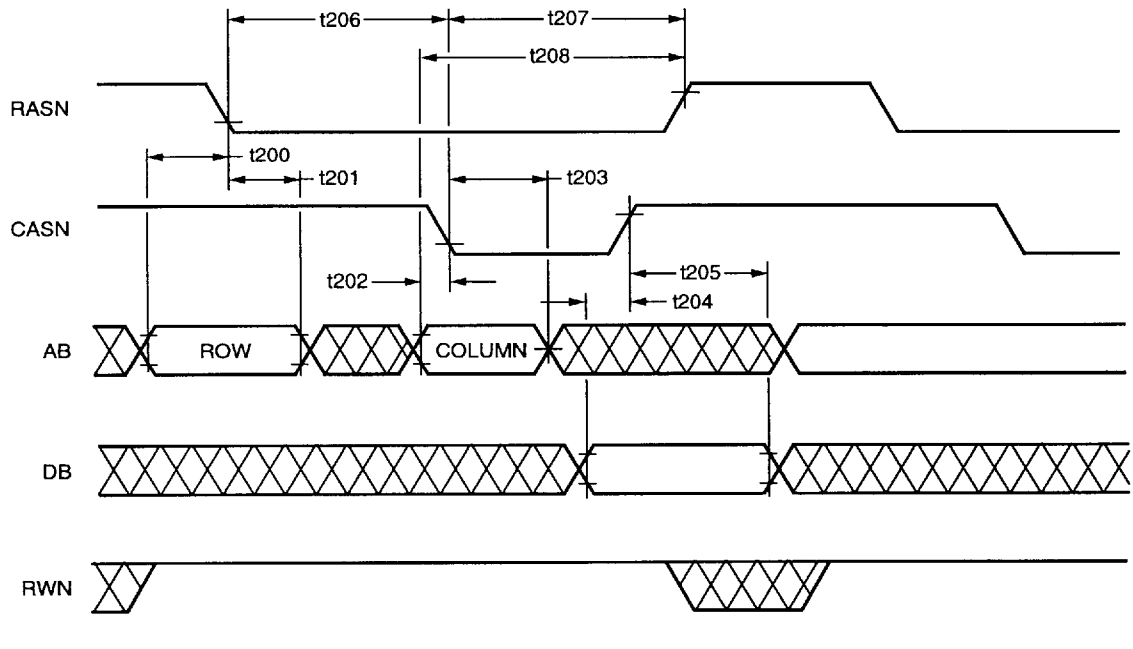


Figure 27. Read Cycle Timing (Relative) Diagram

8 Timing Requirements and Characteristics (continued)

8.10 External DRAM Interface (continued)

Table 110. Timing Specification for a DRAM Read Cycle

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t200	Address Setup to RASN Low	0.5T – 3	—	0.5T – 3	—	0.5T – 3	—	ns
t201	Address Hold to RASN Low	(C + 0.5)T – 3	—	(C + 0.5)T – 3	—	(C + 0.5)T – 3	—	ns
t202	Address Setup to CASN Low	0.5T – 3	—	0.5T – 3	—	0.5T – 3	—	ns
t203	Address Hold to CASN Low	(0.5 + P + A)T	—	(0.5 + P + A)T	—	(0.5 + P + A)T	—	ns
t204	DATA Setup to CASN High	20	—	20	—	20	—	ns
t205	DATA Hold to CASN High	0	—	0	—	0	—	ns
t206	RASN Low to CASN Low	(C + 1)T – 3	—	(C + 1)T – 3	—	(C + 1)T – 3	—	ns
t207	CASN Low to RASN High	(0.5 + A – C)T – 1	—	(0.5 + A – C)T – 1	—	(0.5 + A – C)T – 1	—	ns
t208	Column Address Valid to RASN High	(A + 1 – C)T – 3	—	(A + 1 – C)T – 3	—	(A + 1 – C)T – 3	—	ns

Note: The following definitions apply to the T_{MIN} columns in Table 110. For more information, see Table 30 on page 52.

C = CADLY, column address delay, 0 or 1 CKO cycle.
A = ACC, access time, 0 to 15 CKO cycles.
P = PRCH, precharge time, 0 to 7 CKO cycles.
T = the period of the free-running clock, CKO.

8 Timing Requirements and Characteristics (continued)

8.10 External DRAM Interface (continued)

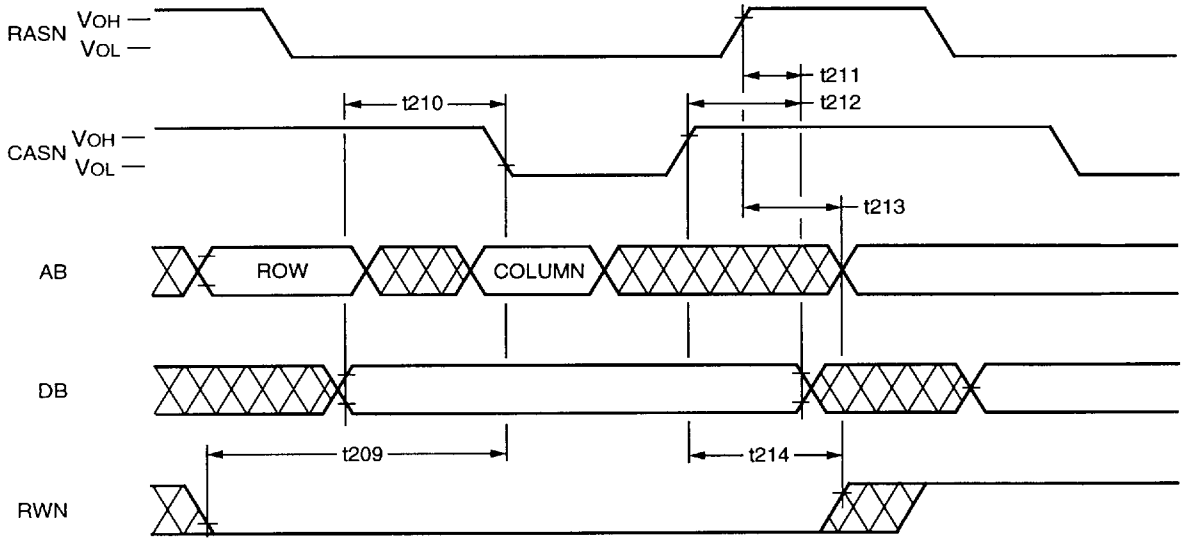


Figure 28. Early Write Cycle Timing (Relative) Diagram

Table 111. Timing Specification for a DRAM Write Cycle

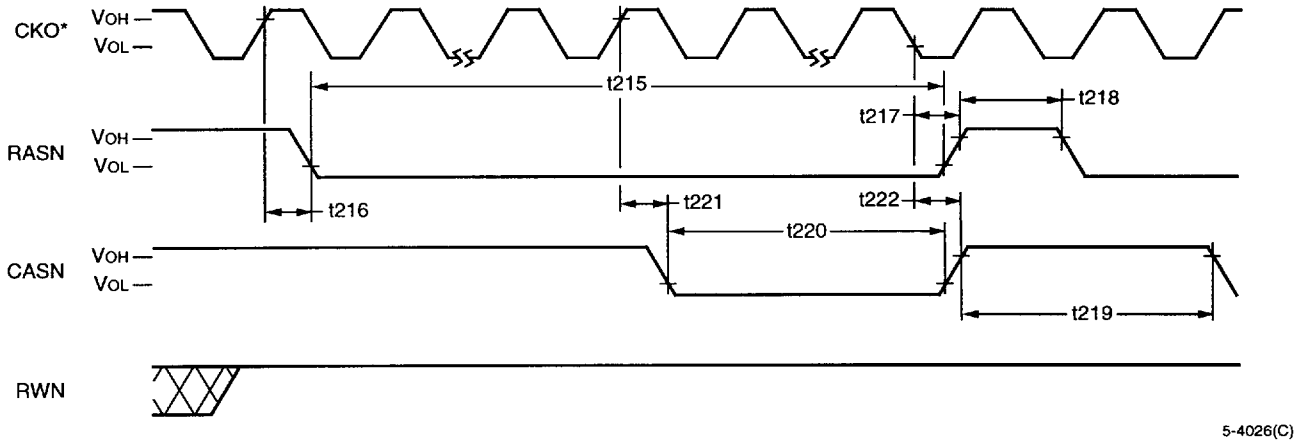
Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t209	RW Low to CASN Low	(1.5 + C)T – 1	—	(1.5 + C)T – 1	—	(1.5 + C)T – 1	—	ns
t210	DB Valid to CASN Low	(0.5 + C)T – 3	—	(0.5 + C)T – 3	—	(0.5 + C)T – 3	—	ns
t211	RASN High to DB Invalid	0	—	0	—	0	—	ns
t212	CASN High to DB Invalid	0	—	0	—	0	—	ns
t213	RASN High to RWN High	0	—	0	—	0	—	ns
t214	CASN High to RWN High	0	—	0	—	0	—	ns

Note: The following definitions apply to the T_{MIN} columns in Table 111. For more information, see Table 30 on page 52.

C = CADLY, column address delay, 0 or 1 CKO cycle.
T = the period of the free-running clock, CKO.

8 Timing Requirements and Characteristics (continued)

8.10 External DRAM Interface (continued)



* CKO is a free-running clock.
Note: The CKO pin is available only on the 80-pin MQFP package.

Figure 29. Synchronous Delay DRAM Interface Timing Diagram

Table 112. Timing Specification for DRAM Control Signals

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t215	Pulse RASN Low	(A + 1.5)T – 1	—	(A + 1.5)T – 1	—	(A + 1.5)T – 1	—	ns
t216	CKO High to RASN Low	—	5	—	5	—	5	ns
t217	CKO Low to RASN High	—	5	—	5	—	5	ns
t218	Pulse RASN High	(P + 0.5)T – 1	—	(P + 0.5)T – 1	—	(P + 0.5)T – 1	—	ns
t219	Pulse CASN High	(P + 1.5 + C)T – 1	—	(P + 1.5 + C)T – 1	—	(P + 1.5 + C)T – 1	—	ns
t220	Pulse CASN Low	(A + 0.5 – C)T – 1	—	(A + 0.5 – C)T – 1	—	(A + 0.5 – C)T – 1	—	ns
t221	CKO High to CASN Low	—	5	—	5	—	5	ns
t222	CKO Low to CASN High	—	5	—	5	—	5	ns

Note: The following definitions apply to the T_{MIN} columns in Table 112. For more information, see Table 30 on page 52.

C = CADLY, column address delay, 0 or 1 CKO cycle.
A = ACC, access time, 0 to 15 CKO cycles.
P = PRCH, precharge time, 0 to 7 CKO cycles.
T = the period of the free-running clock, CKO.

8 Timing Requirements and Characteristics (continued)

8.10 External DRAM Interface (continued)

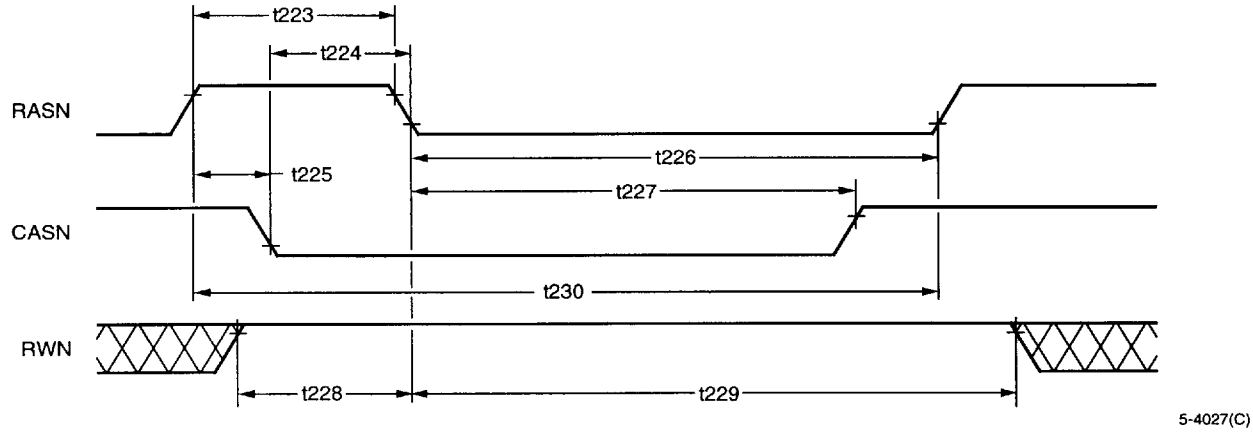


Figure 30. CASN Before RASN Refresh Cycle Timing Diagram

Table 113. Timing Specification for Refresh with XTAL1 Clock

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t223	Pulse RASN High (precharge)	5T – 1	—	5T – 1	—	5T – 1	—	ns
t224	CASN Low to RASN Low	T – 1	—	T – 1	—	T – 1	—	ns
t225	RASN High to CASN Low	5.5T – 1	—	5.5T – 1	—	5.5T – 1	—	ns
t226	Pulse RASN Low (refresh)	5.5T – 1	—	5.5T – 1	—	5.5T – 1	—	ns
t227	RASN Low to CASN High	5.5T – 1	—	5.5T – 1	—	5.5T – 1	—	ns
t228	RWN Setup with Respect to RASN Low	1.5T – 1	—	1.5T – 1	—	1.5T – 1	—	ns
t229	RWN Hold with Respect to Low	10.5T – 1	—	10.5T – 1	—	10.5T – 1	—	ns

Note: In Table 113, T = the period of the free-running clock, CKO.

Table 114. Timing Specification for Refresh Under XTAL2 Clock

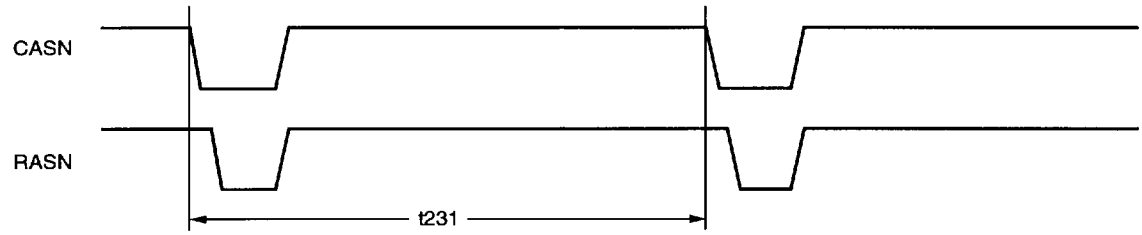
Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t223	Pulse RASN High (precharge)	$2T_2 - 1$	—	$2T_2 - 1$	—	$2T_2 - 1$	—	ns
t224	CASN Low to RASN Low	$T_2 - 1$	—	$T_2 - 1$	—	$T_2 - 1$	—	ns
t225	RASN High to CASN Low	$T_2 - 1$	—	$T_2 - 1$	—	$T_2 - 1$	—	ns
t226	Pulse RASN Low (refresh)	$2T_2 - 1$	—	$2T_2 - 1$	—	$2T_2 - 1$	—	ns
t227	RASN Low to CASN High	$T_2 - 1$	—	$T_2 - 1$	—	$T_2 - 1$	—	ns
t230	Refresh Cycle	$4T_2 - 1$	—	$4T_2 - 1$	—	$4T_2 - 1$	—	ns

Note: In Table 114, T_2 = XTAL2 period.

8 Timing Requirements and Characteristics (continued)

8.10 External DRAM Interface (continued)

The refresh interval is programmed by the RFSH field in the **drc** control register. The shortest interval at 32.768 MHz is 7.68 µs (RFSH = 000). The longest interval at 32.768 MHz is 145 µs (RFSH = 101).



5-4028(C)

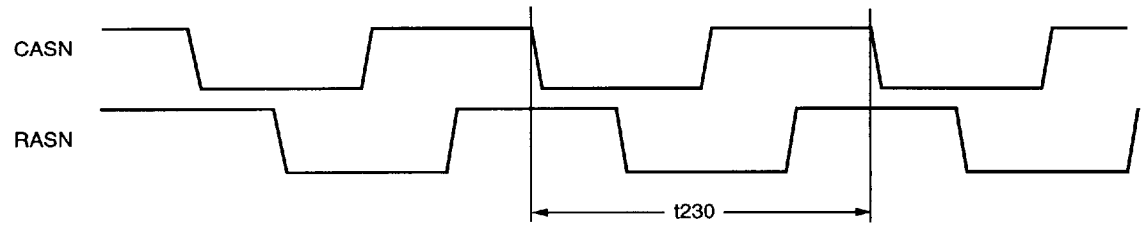
Figure 31. Refresh Interval Timing with XTAL1 Clocking

Table 115. Timing Specifications for Refresh Interval Under XTAL1 Clocking

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t231	Refresh Interval with XTAL1	—	32 × TR	—	32 × TR	—	32 × TR	ns

Note: In Table 115, T = XTAL1 period. R = count number in **drc** register field RFSH: 8, 14, 126, 10, 16, 154.

The refresh interval is set by the XTAL2 clock when clocking has switched to the XTAL2 clock.



5-4029(C)

Figure 32. Refresh Interval Timing with XTAL2 Clocking

Table 116. Timing Specifications for Refresh Interval with XTAL2 Clocking

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t230	Refresh Interval with XTAL2	—	4 × T_2*	—	4 × T_2	—	4 × T_2	ns

* T2 = XTAL2 period.

8 Timing Requirements and Characteristics (continued)

8.11 Serial I/O Specifications

The following figures show a single-cycle load pulse (SCK). However, the timing still applies to a 50% duty cycle.

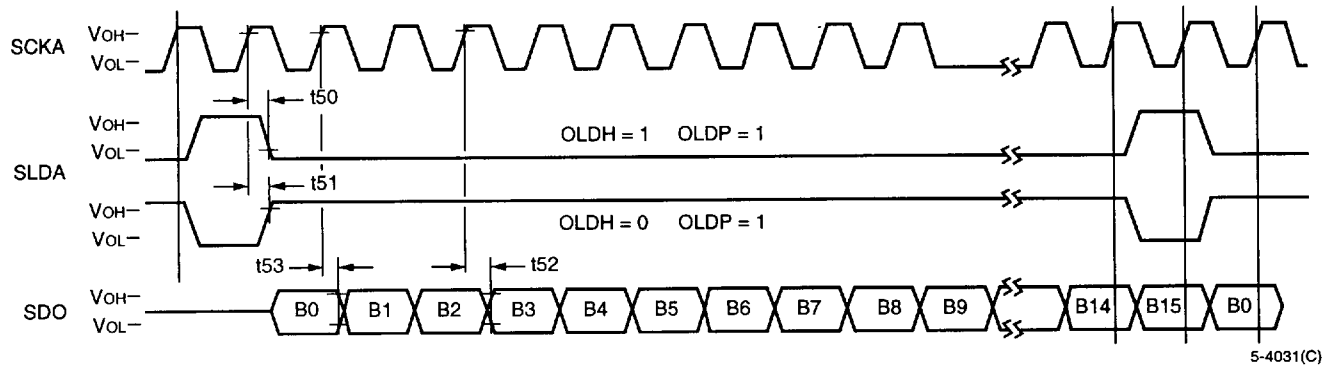


Figure 33. SIO Active Output Timing Diagram

Table 117. Timing Characteristics for Serial Active Output*

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t50	SLDA Delay (high to low)	—	16	—	16	—	16	ns
t51	SLDA Delay (high to high)	—	16	—	16	—	16	ns
t52	Data Delay (high to valid)	—	22	—	22	—	22	ns
t53	Data Hold (high to invalid)	3	—	3	—	3	—	ns

* Capacitance load on SCKA and SDO equals 100 pF.

8 Timing Requirements and Characteristics (continued)

8.11 Serial I/O Specifications (continued)

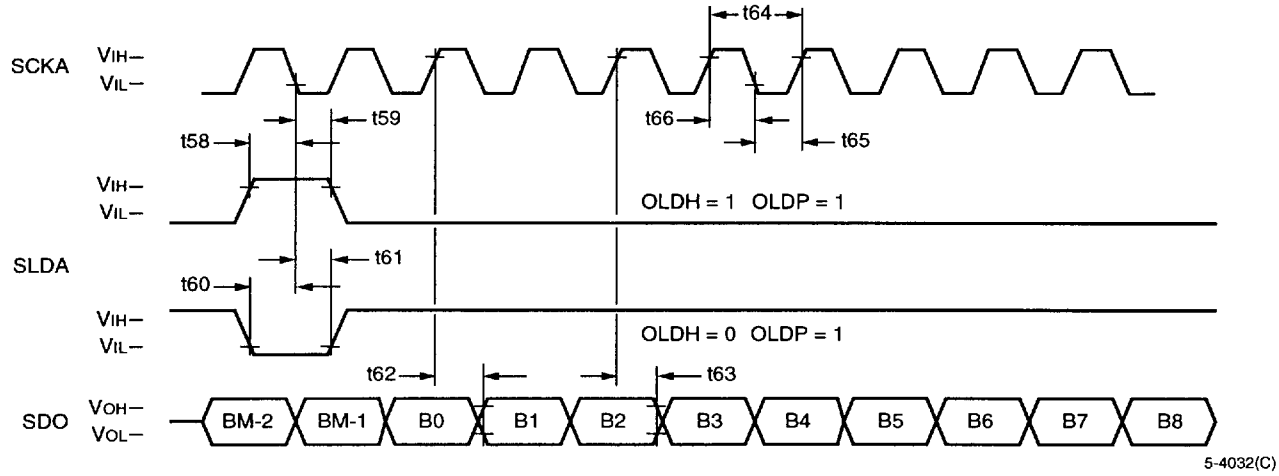


Figure 34. SIO Passive Output Timing Diagram

Table 118. Timing Requirements for Serial Passive Output

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t58	SLDA Setup (high to low)	4	—	4	—	4	—	ns
t59	SLDA Hold (low to invalid)	4	—	4	—	4	—	ns
t60	SLDA Setup (high to low)	4	—	4	—	4	—	ns
t61	SLDA Hold (low to invalid)	4	—	4	—	4	—	ns
t64	Clock Period (high to high)	50	—*	50	—*	50	—*	ns
t65	Clock Low Time (low to high)	22	—	22	—	22	—	ns
t66	Clock High Time (high to low)	22	—	22	—	22	—	ns

* Device is fully static; t64 is tested at 2000 ns.

Table 119. Timing Characteristics for Serial Passive Output

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t62	Data Delay (high to valid)	—	22	—	22	—	22	ns
t63	Data Hold (high to invalid)	4	—	4	—	4	—	ns

8 Timing Requirements and Characteristics (continued)

8.11 Serial I/O Specifications (continued)

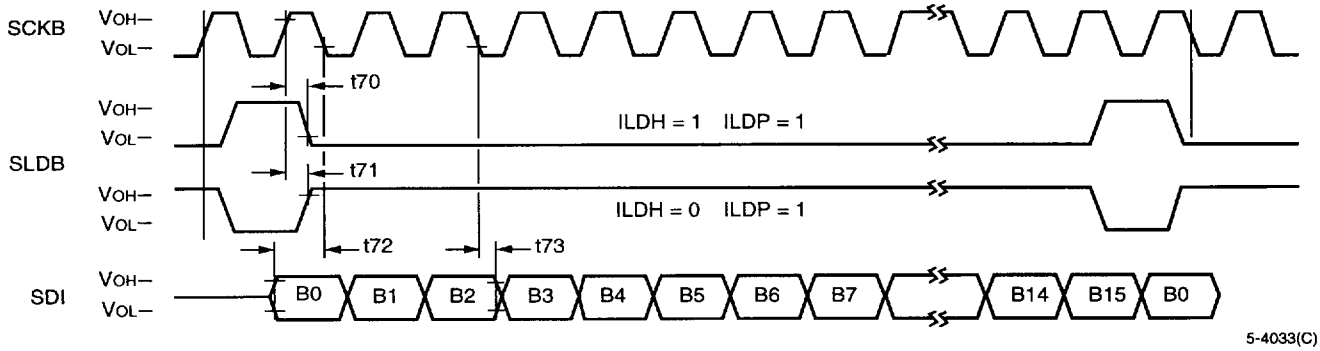


Figure 35. SIO Active Input Timing Diagram

Table 120. Timing Characteristics for Serial Active Input Clocks

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t70	SLDB Delay (high to low)	—	13	—	15	—	16	ns
t71	SLDB Delay (high to high)	—	14	—	16	—	17	ns

Table 121. Timing Requirements for Serial Active Input

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t72	Data Setup (valid to low)	2	—	2	—	2	—	ns
t73	Data Hold (low to invalid)	4	—	4	—	4	—	ns

8 Timing Requirements and Characteristics (continued)

8.11 Serial I/O Specifications (continued)

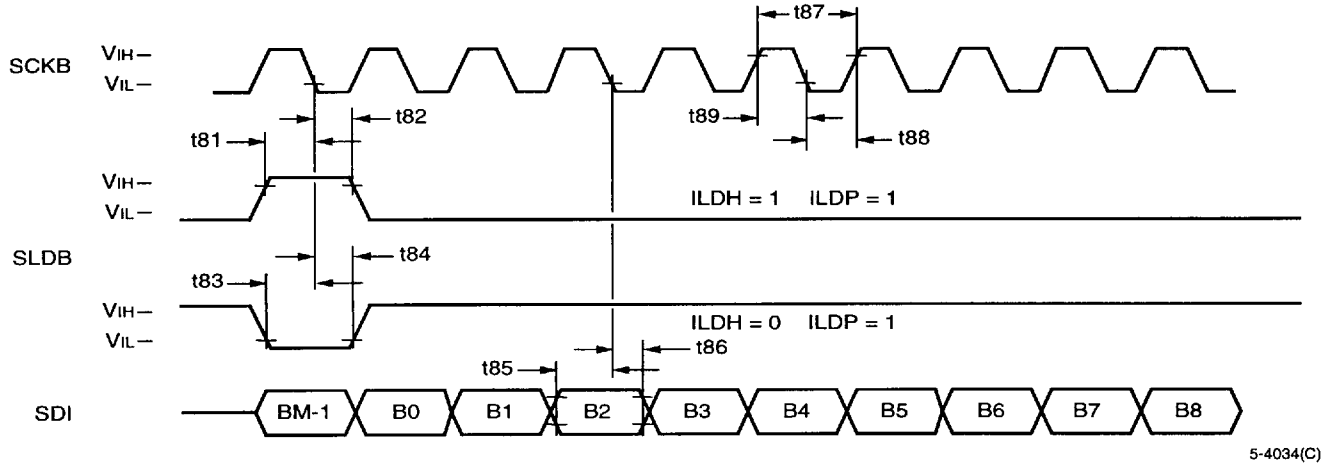


Figure 36. SIO Passive Input Timing Diagram

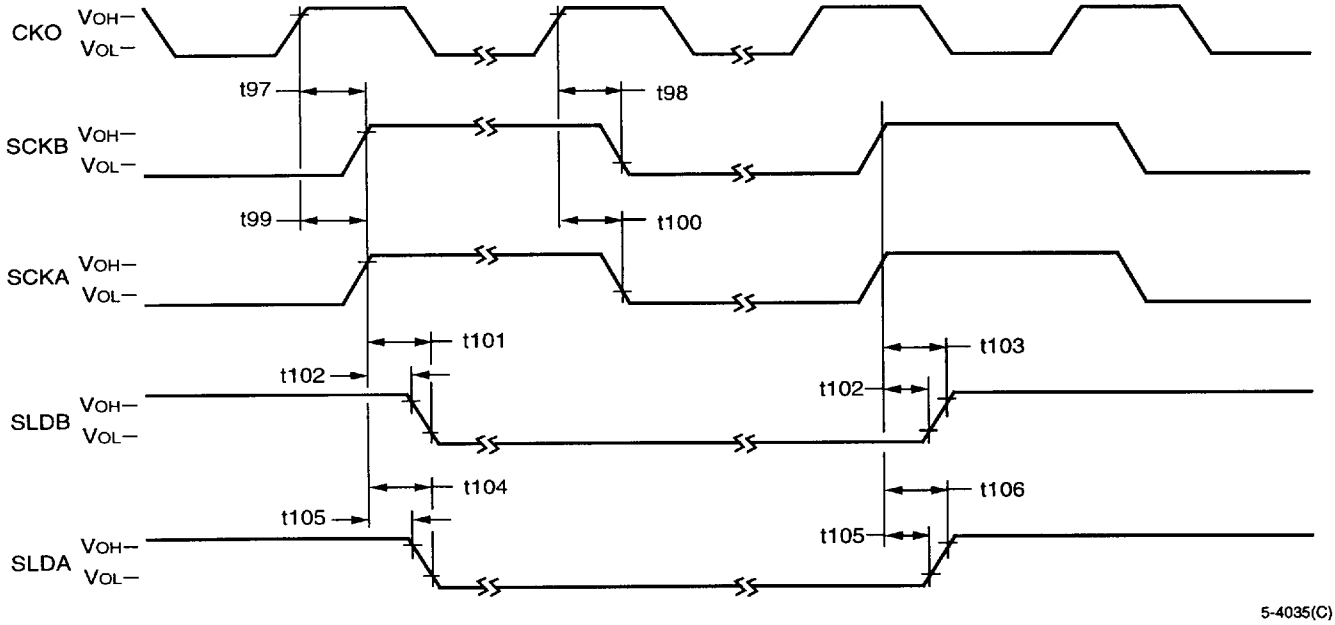
Table 122. Timing Requirements for Serial Passive Input

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t81	SLDB Setup (high to low)	4	—	4	—	4	—	ns
t82	SLDB Hold (low to invalid)	4	—	4	—	4	—	ns
t83	SLDB Setup (low to low)	4	—	4	—	4	—	ns
t84	SLDB Hold (low to invalid)	4	—	4	—	4	—	ns
t85	Data Setup (valid to low)	2	—	2	—	2	—	ns
t86	Data Hold (low to invalid)	4	—	4	—	4	—	ns
t87	Clock Period (high to high)	50	—*	50	—*	50	—*	ns
t88	Clock Low Time (low to high)	22	—	22	—	22	—	ns
t89	Clock High Time (high to low)	22	—	22	—	22	—	ns

* Device is fully static; t87 is tested at 2000 ns.

8 Timing Requirements and Characteristics (continued)

8.11 Serial I/O Specifications (continued)



Note: The CKO pin is available only on the 80-pin MQFP package.

Figure 37. Serial I/O Active Clocks Timing Diagram

Table 123. Timing Characteristics for Signal Generation

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t97	SCKB Delay (high to high)	—	16	—	18	—	19	ns
t98	SCKB Delay (high to low)	—	16	—	18	—	19	ns
t99	SCKA Delay (high to high)	—	16	—	18	—	19	ns
t100	SCKA Delay (high to low)	—	16	—	18	—	19	ns
t101	SLDB Delay (high to low)	—	38	—	40	—	41	ns
t102	SLDB Hold (high to invalid)	2	—	4	—	5	—	ns
t103	SLDB Delay (high to high)	—	38	—	40	—	41	ns
t104	SLDA Delay (high to low)	—	38	—	40	—	41	ns
t105	SLDA Hold (high to invalid)	2	—	4	—	5	—	ns
t106	SLDA Delay (high to high)	—	38	—	40	—	41	ns

8 Timing Requirements and Characteristics (continued)

8.12 PHIF Specifications

For the PHIF, READ means read by the external user (output by the DSP); WRITE is similarly defined. The 8-bit reads/writes are identical to one-half of a 16-bit access.

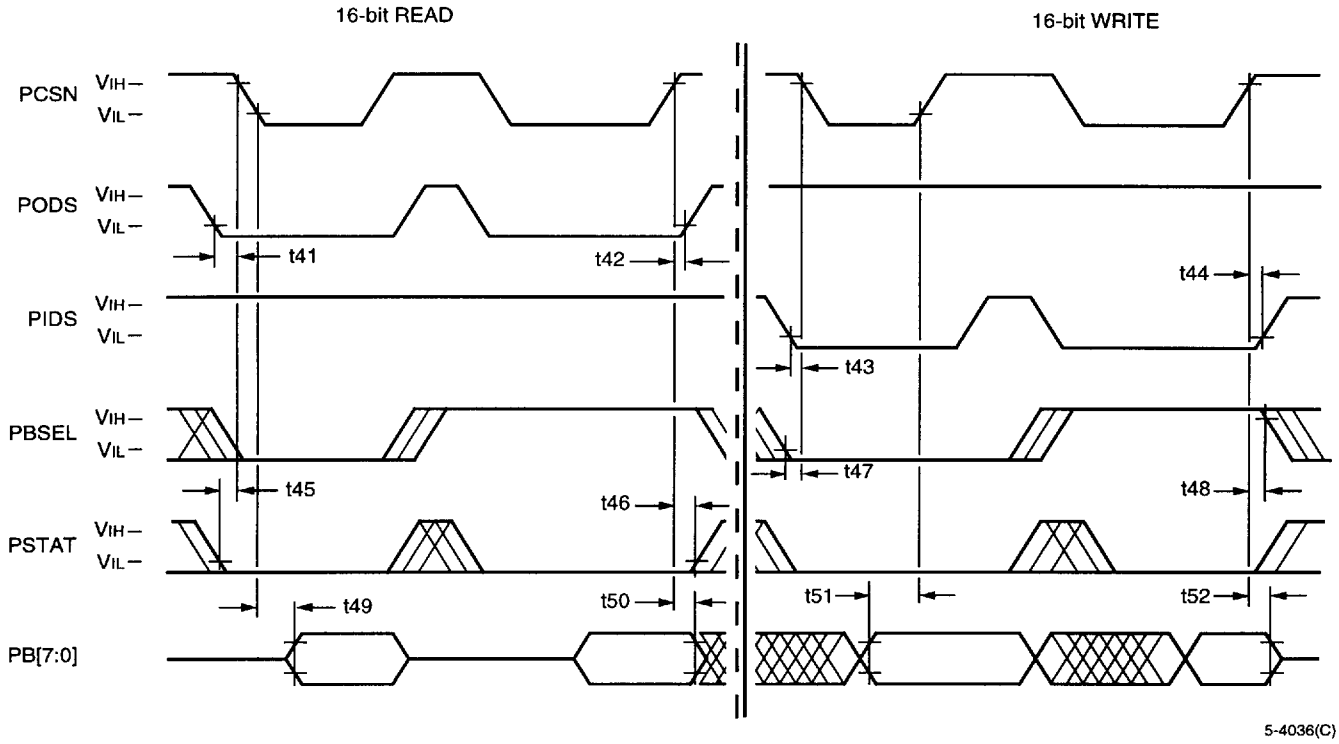


Figure 38. PHIF *Intel* Mode Signaling (Read and Write) Timing Diagram

As shown in Figure 38 and Tables 124 and 125, the PHIF port uses the PCSN signal to initiate and complete a transaction. The transactions can also be initiated and completed with the PIDS and PODS signals. An output transaction (read) is initiated by PCSN or PODS going low, whichever comes last. For example, the timing requirements referenced to PCSN going low, t45 and t49, should be referenced to PODS going low, if PODS goes low after PCSN. An output transaction is completed by PCSN or PODS going high, whichever comes first. An input transaction is initiated by PCSN or PIDS going low, whichever comes last. An input transaction is completed by PCSN or PIDS going high, whichever comes first. All requirements referenced to PCSN apply to PIDS or PODS, if PIDS or PODS is the controlling signal.

8 Timing Requirements and Characteristics (continued)

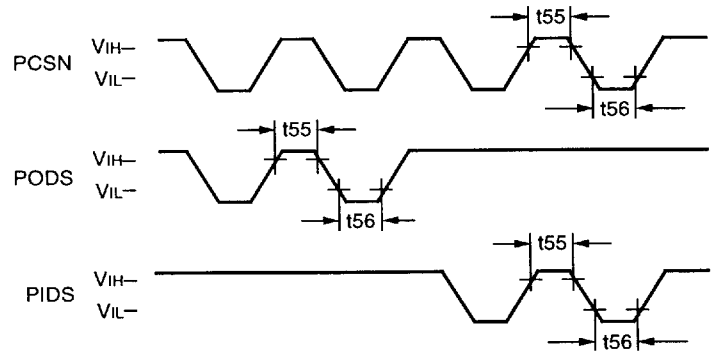
8.12 PHIF Specifications (continued)

Table 124. Timing Requirements for PHIF *Intel* Mode Signaling

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t41	PODS to PCSN Setup (low to valid)	0	—	0	—	0	—	ns
t42	PCSN to PODS Hold (high to invalid)	0	—	0	—	0	—	ns
t43	PIDS to PCSN Setup (low to valid)	0	—	0	—	0	—	ns
t44	PCSN to PIDS Hold (high to invalid)	0	—	0	—	0	—	ns
t45	PSTAT to PCSN Setup (low to valid)	6	—	6	—	6	—	ns
t46	PCSN to PSTAT Hold (high to invalid)	0	—	0	—	0	—	ns
t47	PBSEL to PCSN Setup (valid to valid)	6	—	6	—	6	—	ns
t48	PCSN to PBSEL Hold (high to invalid)	0	—	0	—	0	—	ns
t51	PB Write to PCSN Setup (valid to invalid)	10	—	10	—	10	—	ns
t52	PCSN to PB Write Hold (high to invalid)	5	—	5	—	5	—	ns

Table 125. Timing Characteristics for PHIF *Intel* Mode Signaling

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t49	PCSN to PB Read (low to valid)	—	16	—	17	—	17	ns
t50	PCSN to PB Read Hold (high to invalid)	2	—	3	—	3	—	ns



5-4037(C)

Figure 39. PHIF *Intel* Mode Signaling Pulse Period Timing Diagram

8 Timing Requirements and Characteristics (continued)

8.12 PHIF Specifications (continued)

Table 126. Pulse Period Requirements for PHIF *Intel* Mode Signaling

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t55	PCSN/PODS/PIDS Pulse High	18	—	20	—	20	—	ns
t56	PCSN/PODS/PIDS Pulse Low	18	—	20	—	20	—	ns

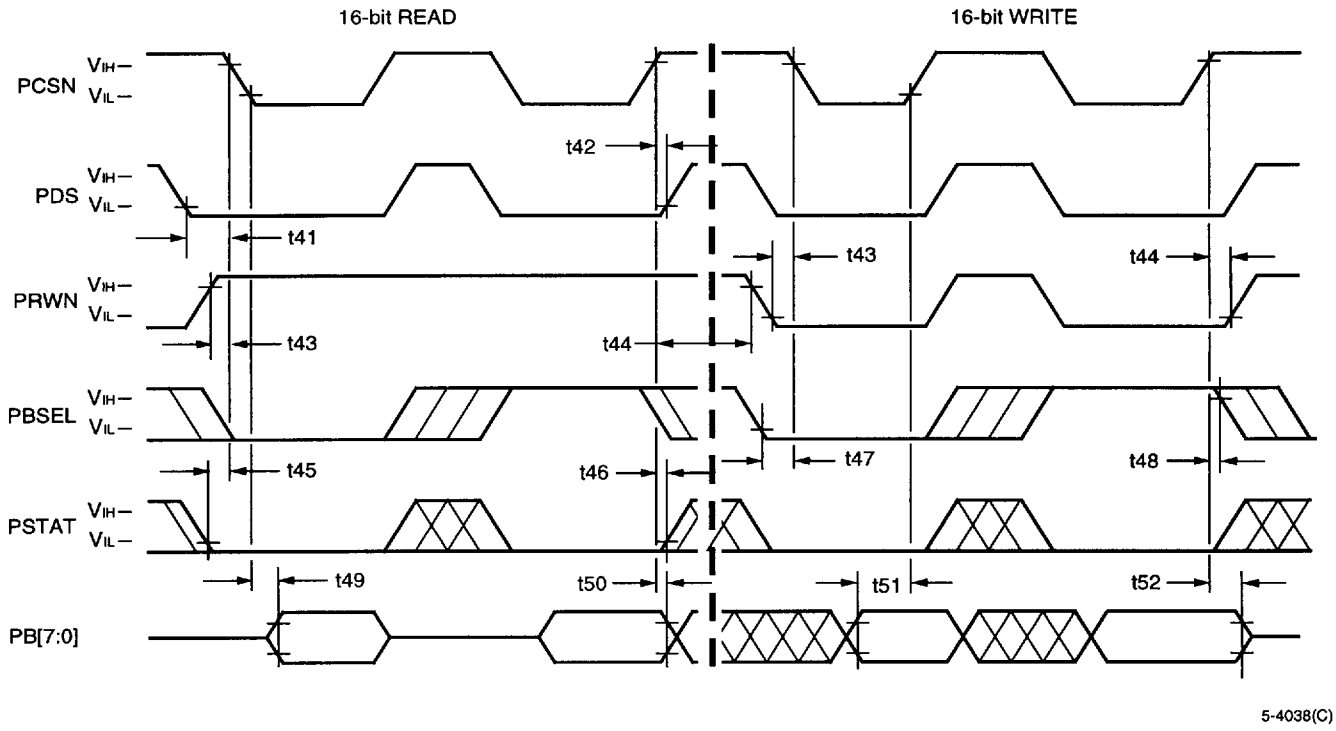


Figure 40. PHIF *Motorola* Mode Signaling (Read and Write) Timing Diagram

As shown in Figure 40 and Tables 127 and 128, the PHIF port uses the PCSN signal to initiate and complete a transaction. The transactions can also be initiated and completed with the PDS signal. An input/output transaction is initiated by PCSN or PDS going low, whichever comes last. For example, the timing requirements referenced to PCSN going low, t45 and t49, should be referenced to PDS going low, if PDS goes low after PCSN. An input/output transaction is completed by PCSN or PDS going high, whichever comes first. All requirements referenced to PCSN should be referenced to PDS, if PDS is the controlling signal. PRWN should never be used to initiate or complete a transaction.

8 Timing Requirements and Characteristics (continued)

8.12 PHIF Specifications (continued)

Table 127. Timing Requirements for PHIF *Motorola* Mode Signaling

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t41	PDS* to PCSN Setup (low to valid)	0	—	0	—	0	—	ns
t42	PCSN to PDS Hold (high to invalid)	0	—	0	—	0	—	ns
t43	PRWN to PCSN Setup (low to valid)	6	—	6	—	6	—	ns
t44	PCSN to PRWN Hold (high to invalid)	0	—	0	—	0	—	ns
t45	PSTAT to PCSN Setup (low to low)	6	—	6	—	6	—	ns
t46	PCSN to PSTAT Hold (high to invalid)	0	—	0	—	0	—	ns
t47	PBSEL to PCSN Setup (valid to valid)	6	—	6	—	6	—	ns
t48	PCSN to PBSEL Hold (high to invalid)	0	—	0	—	0	—	ns
t51	PB Write to PCSN Setup (valid to invalid)	10	—	10	—	10	—	ns
t52	PCSN to PB Write Hold (high to invalid)	5	—	5	—	5	—	ns

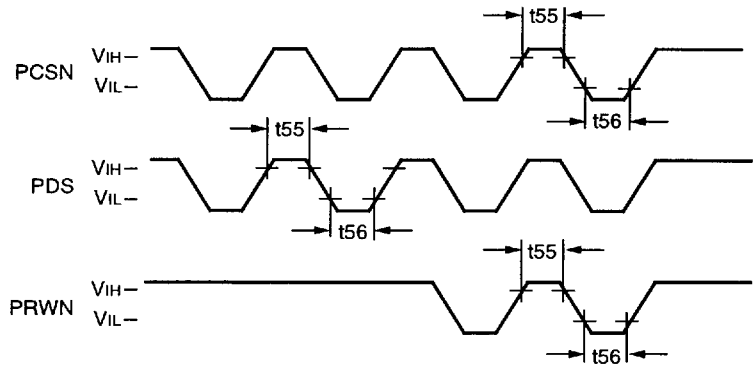
* PDS is programmable to be active-high or active-low. It is shown active-low in Figures 46 and 47. References t41 and t42 apply to the active-high level as well.

Table 128. Timing Characteristics for PHIF *Motorola* Mode Signaling

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t49	PCSN to PB Read (low to valid)	—	15	—	17	—	17	ns
t50	PCSN to PB Read (high to invalid)	2	—	3	—	3	—	ns

8 Timing Requirements and Characteristics (continued)

8.12 PHIF Specifications (continued)



5-4039(C)

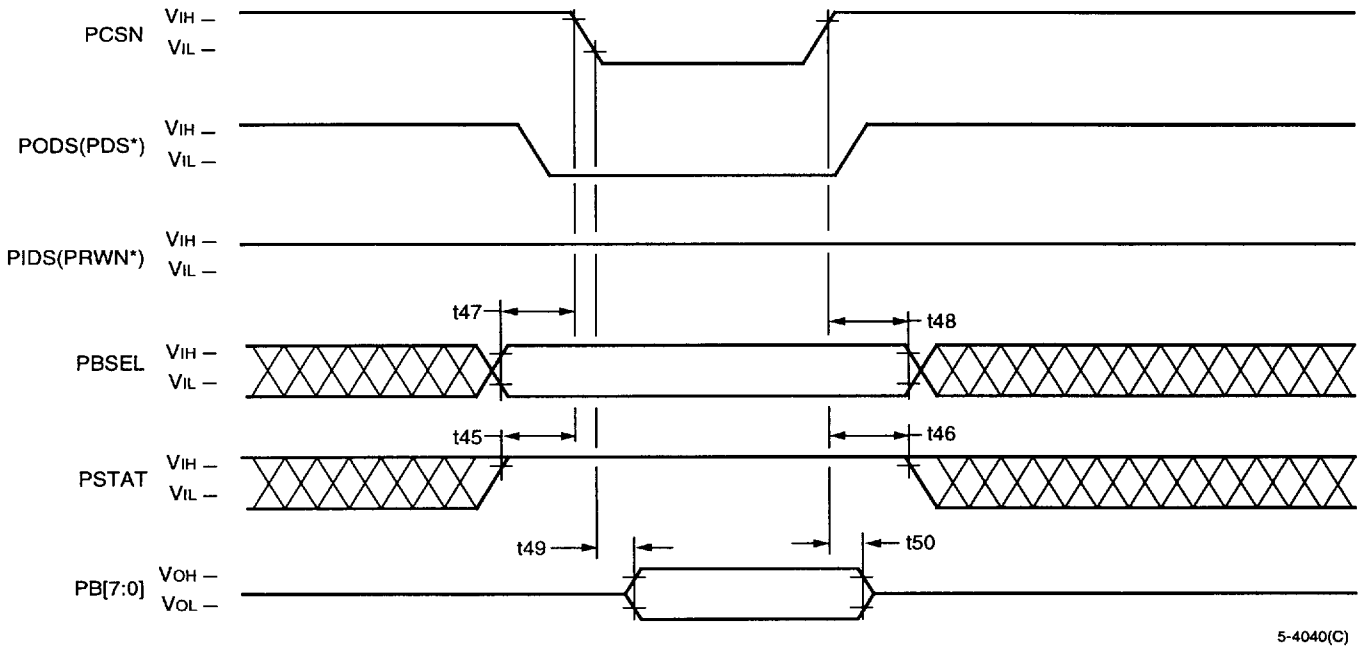
Figure 41. PHIF *Motorola* Mode Signaling Pulse Period Timing Diagram

Table 129. Pulse Period Requirements for PHIF *Motorola* Mode Signaling

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t55	PCSN/PDS/PRWN Pulse High	18	—	20	—	20	—	ns
t56	PCSN/PDS/PRWN Pulse Low	18	—	20	—	20	—	ns

8 Timing Requirements and Characteristics (continued)

8.12 PHIF Specifications (continued)



* *Motorola* mode signal name.

Figure 42. PHIF *Intel* or *Motorola* Mode Signaling (Status Register Read) Timing Diagram

Table 130. Timing Requirements for *Intel* and *Motorola* Mode Signaling (Status Register Read)

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t45*	PSTAT to PCSN Setup (high to valid)	6	—	6	—	6	—	ns
t46†	PCSN to PSTAT Hold (high to invalid)	0	—	0	—	0	—	ns
t47*	PBSEL to PCSN Setup (valid to valid)	6	—	6	—	6	—	ns
t48†	PCSN to PBSEL Hold (high to invalid)	0	—	0	—	0	—	ns

* t45, t47, and t49 are referenced to the falling edge of PCSN or PODS(PDS), whichever occurs last.
† t46, t48, and t50 are referenced to the rising edge of PCSN or PODS(PDS), whichever occurs first.

Table 131. Timing Characteristics for *Intel* and *Motorola* Mode Signaling (Status Register Read)

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t49*	PCSN to PB Read (low to valid)	—	15	—	17	—	17	ns
t50†	PCSN to PB Read Hold (high to invalid)	2	—	3	—	3	—	ns

* t45, t47, and t49 are referenced to the falling edge of PCSN or PODS(PDS), whichever occurs last.
† t46, t48, and t50 are referenced to the rising edge of PCSN or PODS(PDS), whichever occurs first.

9 Crystal Oscillator Electrical Requirements and Characteristics

This section describes electrical requirements and characteristics for high- and low-frequency crystal oscillator circuits.

9.1 High-Frequency Crystal Oscillator

If the option for using the external high-frequency crystal, XTAL1, is chosen, the electrical requirements and characteristics described in this section apply.

9.1.1 High-Frequency Crystal Oscillator Power Dissipation

The typical power dissipation at 32 MHz of the internal high-frequency crystal oscillator circuit is below 20 mW. The maximum power dissipation is below 50 mW at 5 V.

9.1.2 High-Frequency Crystal Oscillator External Components

The crystal oscillator is enabled by connecting a crystal across XTAL1IN and XTAL1OUT, along with one external capacitor from each of these pins to ground (see Figure 43). For most applications, 30 pF external capacitors are recommended; however, larger values may be necessary if precise frequency tolerance is required (see Section 9.3, Frequency Accuracy Considerations). The crystal should be either fundamental or overtone mode, parallel resonant, with a power dissipation of at least 1 mW, and be specified at a load capacitance equal to the total capacitance seen by the crystal (including external capacitors and strays).

The series resistance of the crystal should be specified to be less than half the absolute value of the negative resistance shown in Figures 44 and 45 for the crystal frequency. Internal clock (XTAL1) and clock output (CKO) frequencies are both equal to the crystal frequency.

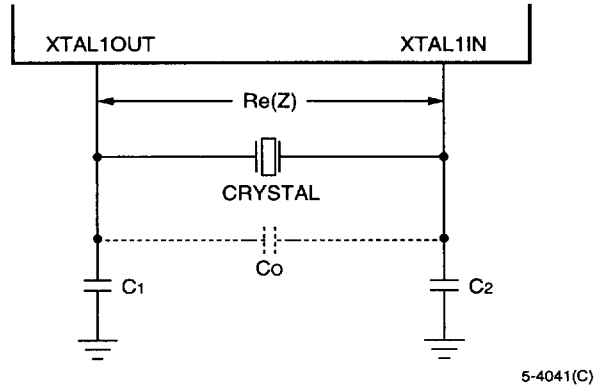


Figure 43. Fundamental Crystal Configuration

The following guidelines should be followed when designing the printed-circuit board layout for a crystal-based application:

- Keep crystal and external capacitors as close to XTAL1IN and XTAL1OUT pins as possible to minimize board stray capacitance.
- Keep high-frequency digital signals such as CKO* away from XTAL1IN and XTAL1OUT traces to avoid coupling.

* The CKO pin is available only on the 80-pin MQFP package.

9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.1 High-Frequency Crystal Oscillator (continued)

9.1.3 High-Frequency Crystal Oscillator Negative Resistance Curves

Figure 44 shows worst-case negative resistance curves for a high-frequency crystal oscillator operating with a 5 V power supply (V_{DD} = 4.5 V to 5.5 V). These worst-case conditions are as follows:

- Maximum Temperature = 120 °C
- Minimum V_{DD} = 4.5 V
- Maximum C_O = 7 pF

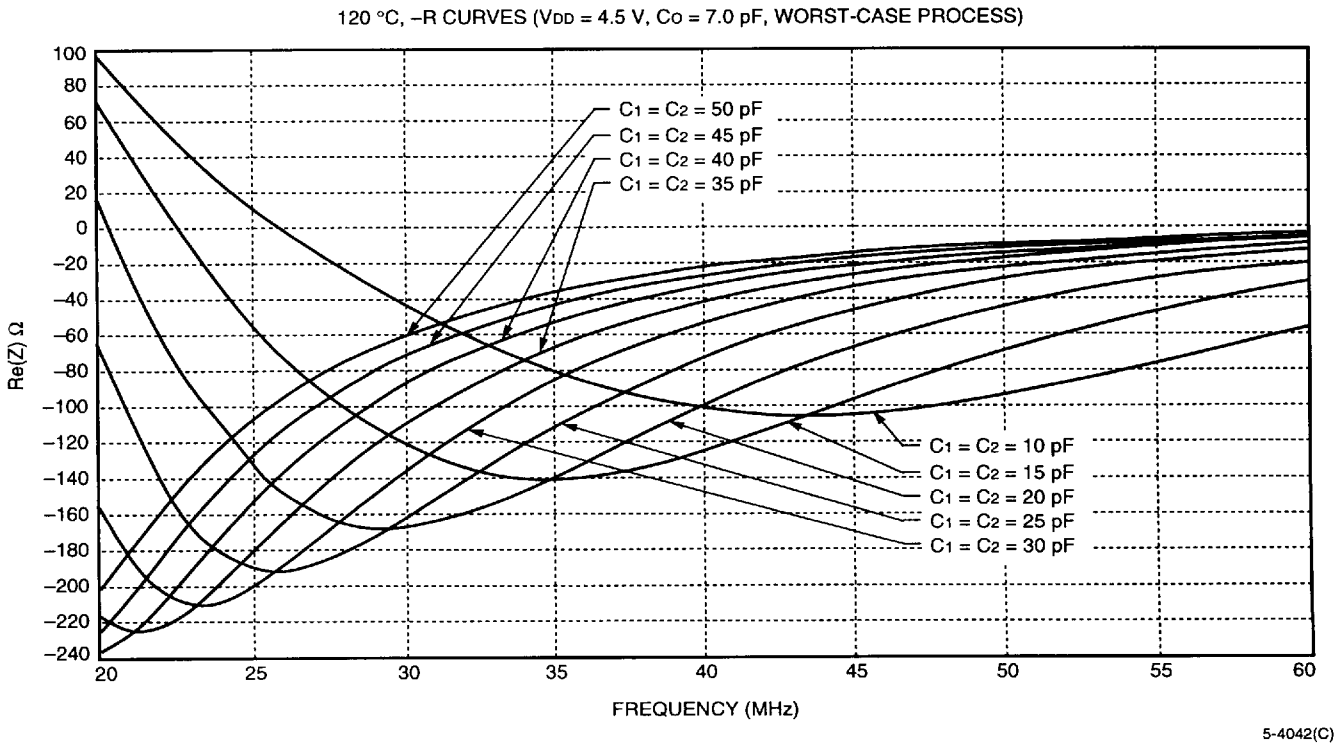


Figure 44. 5 V High-Frequency Crystal Oscillator Negative Resistance Curves

9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.1 High-Frequency Crystal Oscillator (continued)

9.1.3 High-Frequency Crystal Oscillator Negative Resistance Curves (continued)

Figure 45 shows worst-case negative resistance curves for a high-frequency crystal oscillator operating with a 3.3 V power supply (V_{DD} = 3.0 V to 3.6 V). These worst-case conditions are as follows:

- Maximum Temperature = 120 °C
- Minimum V_{DD} = 2.7 V
- Maximum C_O = 7 pF

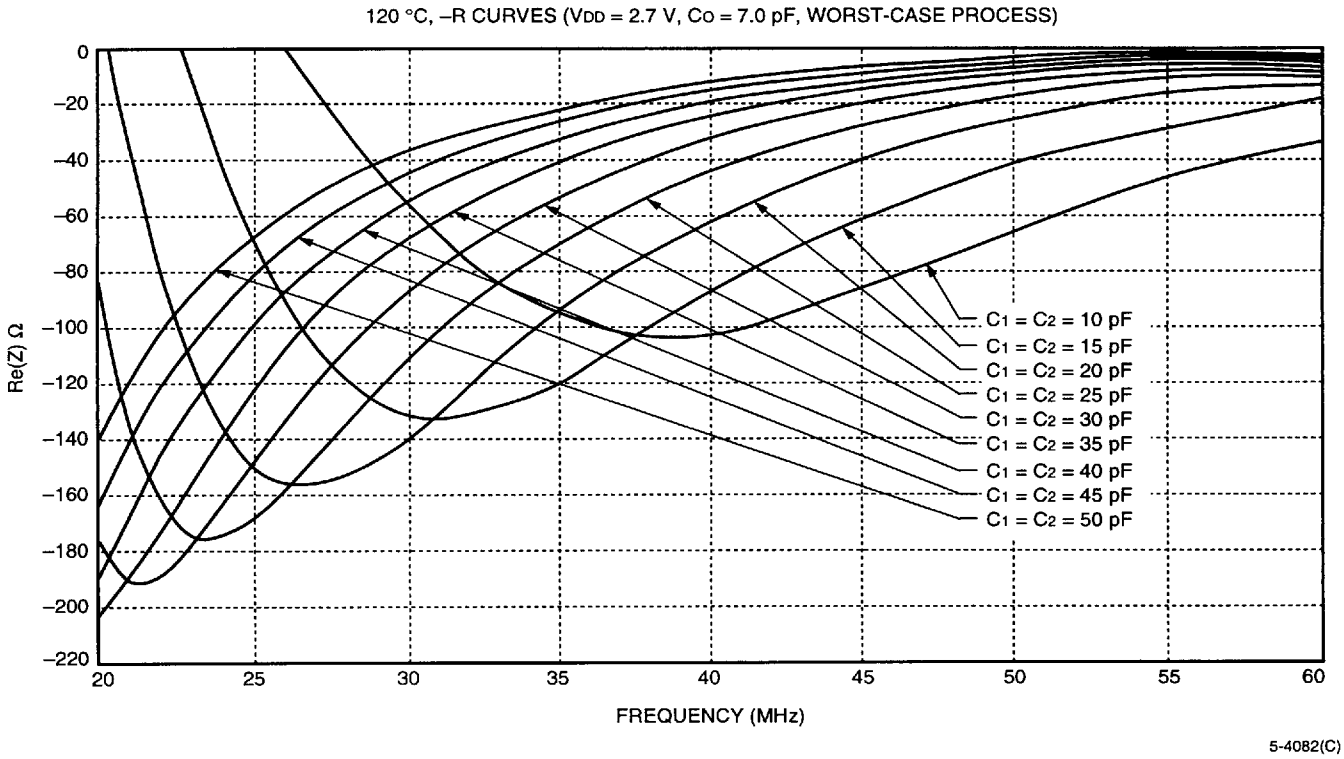


Figure 45. 3.3 V High-Frequency Crystal Oscillator Negative Resistance Curves

9 Crystal Oscillator Electrical Requirements and Characteristics

(continued)

9.1 High-Frequency Crystal Oscillator

(continued)

9.1.4 LC Network Design for Third Overtone Crystal Circuits

For operating frequencies of greater than 30 MHz, it is usually cost advantageous to use a third overtone crystal as opposed to a fundamental mode crystal. When using third overtone crystals, it is necessary, however, to filter out the fundamental frequency so that the circuit oscillates only at the third overtone. There are several techniques that accomplish this; one of these is described in this section. Figure 46 shows the basic setup for third overtone operation.

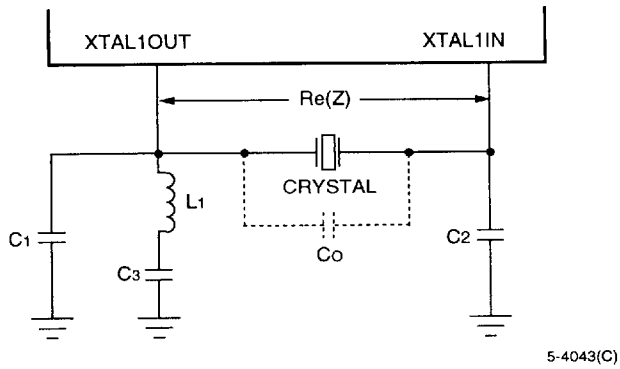


Figure 46. Third Overtone Crystal Configuration

The parallel combination of L_1 and C_1 forms a resonant circuit with a resonant frequency between the first and third harmonic of the crystal such that the LC network appears inductive at the fundamental frequency and capacitive at the third harmonic. This ensures that a 360 phase shift around the oscillator loop occurs at the third overtone frequency but not at the fundamental. The blocking capacitor, C_3, provides dc isolation for the trap circuit and should be chosen to be large compared to C_1.

For example, suppose it is desired to operate with a 32.768 MHz, third overtone, crystal:

Let: f_3 = operating frequency of third overtone crystal (32.768 MHz in this example)

f_1 = fundamental frequency of third overtone crystal, or $f_3/3$ (10.92 MHz in this example)

f_T = resonant frequency of trap, as follows:

$$\frac{1}{2\pi\sqrt{L_1C_1}}$$

C_2 = external load capacitor (30 pF in this example)

C_3 = dc blocking capacitor (1000 pF in this example)

Arbitrarily set trap resonance to geometric mean of f_1 and f_3. Because $f_1 = f_3/3$, the geometric mean would be:

$$f_T = \frac{f_3}{\sqrt{3}} = \frac{32.768\ \text{MHz}}{\sqrt{3}} = 18.92\ \text{MHz}$$

At the third overtone frequency, f_3, it is desirable to have the net impedance of the trap circuit (X_T) equal to the impedance of C_2 (X_{C2}), i.e.,

$$X_T = X_{C2} = X_{C1} \parallel (X_{C3} + X_{L1})$$

Selecting C_3 so that $X_{C3} << X_{L1}$ yields:

$$X_T = X_{C2} = X_{C1} \parallel X_{L1}$$

For a capacitor,

$$X_C = \frac{-j}{\omega C}$$

where $\omega = 2\pi f$

For an inductor,

$$X_L = j\omega L$$

Solving for C_1, and realizing that $L_1C_1 = 3/(2\pi f_3)^2$ yields:

$$C_1 = \frac{3}{2}C_2$$

9 Crystal Oscillator Electrical Requirements and Characteristics

(continued)

9.1 High-Frequency Crystal Oscillator

(continued)

9.1.4 LC Network Design for Third Overtone Crystal Circuits (continued)

Therefore, for C_2 = 30 pF, C_1 = 45 pF. Because the impedance of the trap circuit in this example would be equal to the impedance of a 30 pF capacitor, the negative resistance and supply current curves for $C_1 = C_2$ = 30 pF at 32.768 MHz would apply to this example.

Finally, solving for the inductor value, L_1:

$$L_1 = \frac{1}{4\pi^2 f_T^2 C_2}$$

For the preceding example, L_1 would be 2.36 µH.

9.2 Low-Frequency Crystal Oscillator or Resonator

If the option for using the external crystal or resonator XTAL2 (low frequency/low power) is chosen, the electrical requirements and characteristics described in this section apply.

9.2.1 Low-Frequency Crystal Oscillator or Resonator Power Dissipation

The typical power dissipation of the internal low-frequency crystal oscillator or resonator circuit is less than 1 mW at 500 kHz.

9.2.2 External Components for the Low-Frequency Crystal Oscillator or Resonator

The crystal oscillator or resonator is enabled by connecting a crystal or resonator across XTAL2IN and XTAL2OUT, along with a resistor across these two pins and one external capacitor from each of these pins to ground (see Figure 45). Another resistor can be added in series to the oscillator or resonator to reduce power or to help dissipate excess power. For most crystal applications, 30 pF external capacitors are recommended; however, larger values may be necessary if precise frequency tolerance is required (see Section 9.3, Frequency Accuracy Considerations).

For resonator applications, 150 pF external capacitors are recommended. The crystal should be fundamental mode with a power dissipation of at least 1 mW, and be specified at a load capacitance equal to the total capacitance seen by the crystal (including external capacitors and parasitic capacitance).

The series resistance of the crystal should be specified to be less than half the absolute value of the negative resistance shown in Figure 48 for the crystal frequency. If a resonator is to be used, the series resistance should be specified to be less than half the absolute value of the negative resistance shown in Figure 50. The frequency of the internal slow/low-power clock is equal to the crystal/resonator frequency. When the software selects this clock to be the main DSP clock, the frequency of CKO* is equal to that frequency.

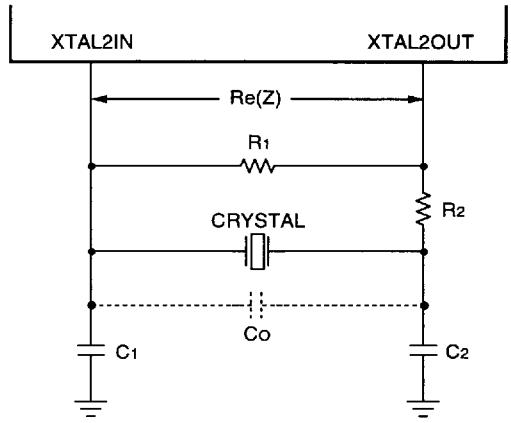


Figure 47. Fundamental Crystal/Resonator Configuration

The following guidelines should be followed when designing the printed-circuit board layout and choosing resistor values.

- Resistor R_1 = 10 MΩ. R_2 = 500 Ω. C_1 and C_2 are chosen based on Figures 48 and 50.
- Keep crystal and external capacitors as close to XTAL2IN and XTAL2OUT pins as possible to minimize board stray capacitance.
- Keep high-frequency digital signals such as CKO* away from XTAL2IN and XTAL2OUT traces to avoid coupling.

* The CKO pin is available only on the 80-pin MQFP package.

9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.2 Low-Frequency Crystal Oscillator or Resonator (continued)

9.2.3 Low-Frequency Crystal Oscillator Negative Resistance Curves

Figure 48 shows worst-case negative resistance curves for a low-frequency crystal oscillator operating with a 5 V power supply (V_{DD} = 4.5 V to 5.5 V). These worst-case conditions are as follows:

- Maximum Temperature = 120 °C
- Minimum V_{DD} = 4.5 V
- Maximum C_O = 200 pF

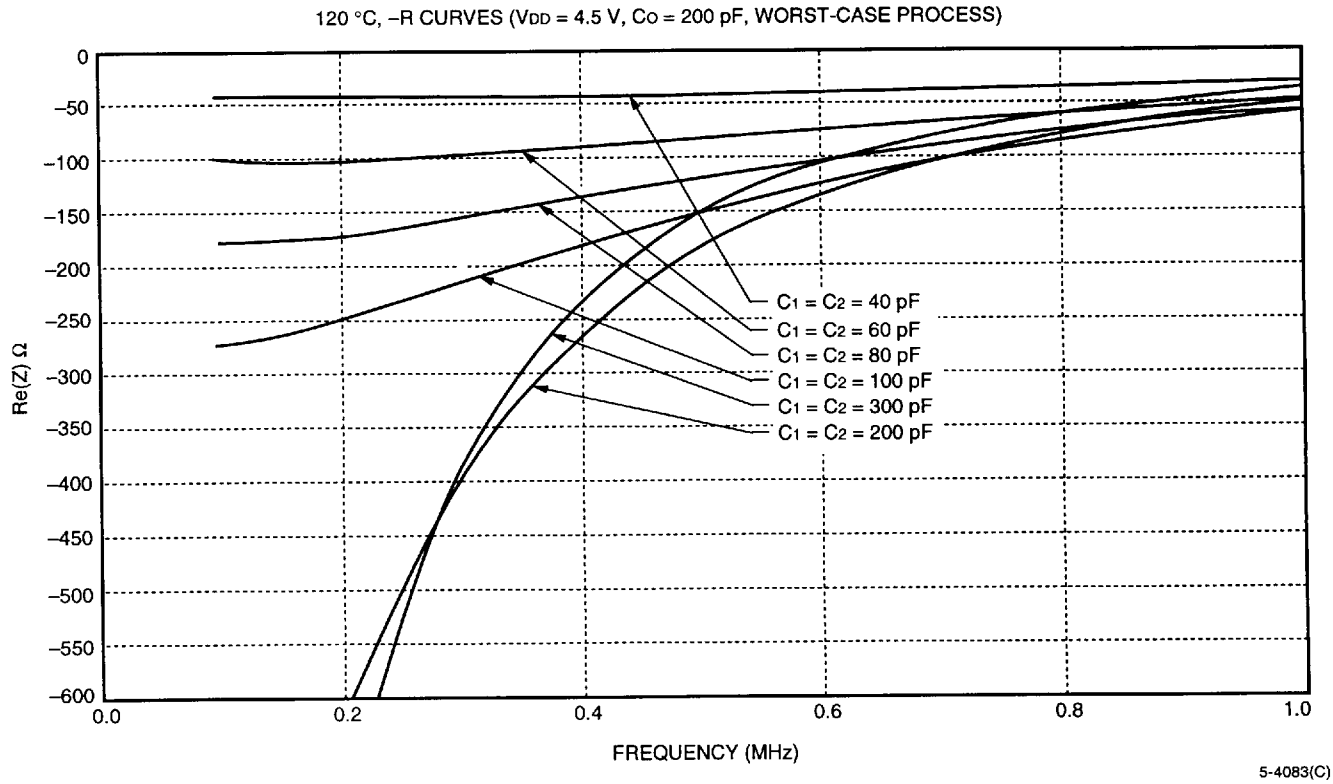


Figure 48. 5 V Low-Frequency Crystal Oscillator Negative Resistance Curves

9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.2 Low-Frequency Crystal Oscillator or Resonator (continued)

9.2.3 Low-Frequency Crystal Oscillator Negative Resistance Curves (continued)

Figure 49 shows worst-case negative resistance curves for a low-frequency crystal oscillator operating with a 3.3 V power supply (V_{DD} = 3.0 V to 3.6 V). These worst-case conditions are as follows:

- Maximum Temperature = 120 °C
- Minimum V_{DD} = 3.0 V
- Maximum C_O = 200 pF

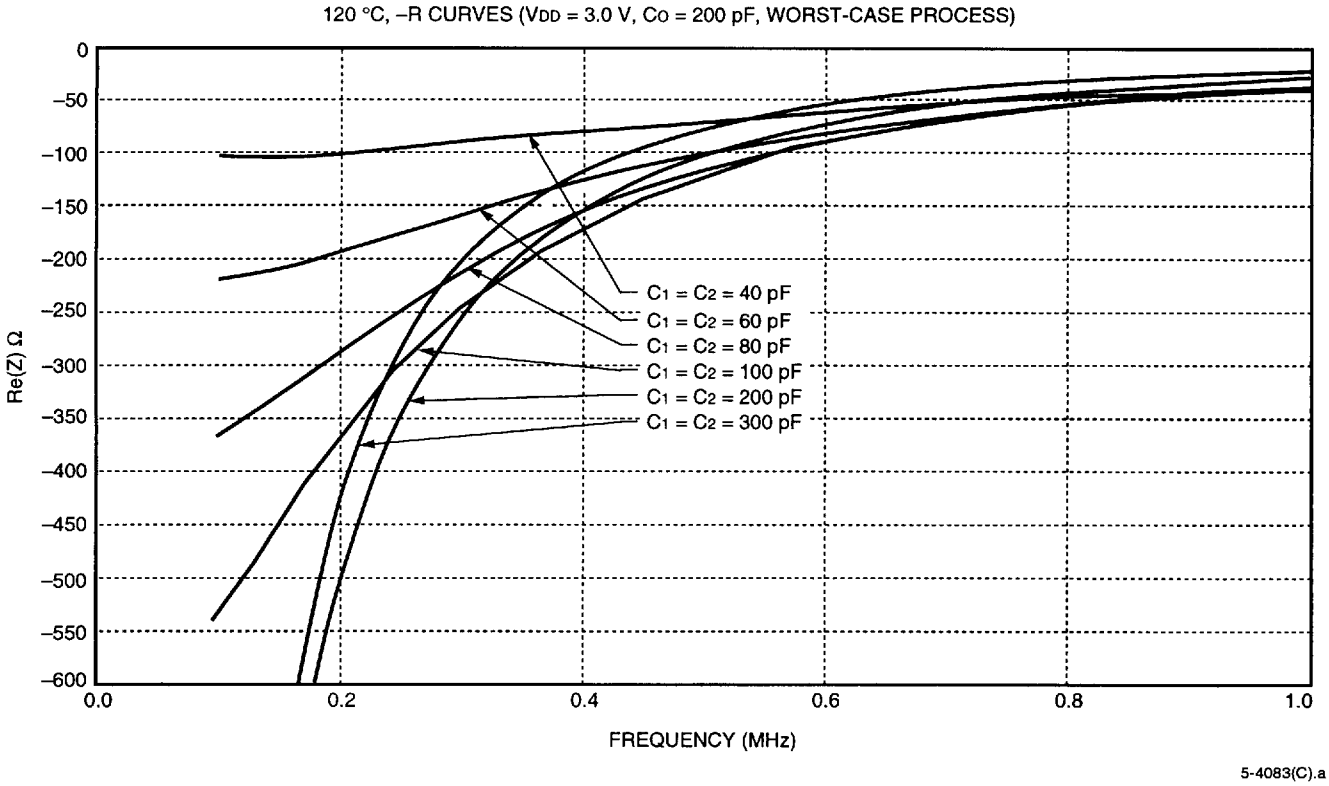


Figure 49. 3.3 V Low-Frequency Crystal Oscillator Negative Resistance Curves

9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.2 Low-Frequency Crystal Oscillator or Resonator (continued)

9.2.4 Low-Frequency Crystal Resonator Negative Resistance Curves

Figure 50 shows worst-case negative resistance curves for a low-frequency crystal resonator operating with a 5 V power supply (V_{DD} = 4.5 V to 5.5 V). These worst-case conditions are as follows:

- Maximum Temperature = 120 °C
- Minimum V_{DD} = 4.5 V
- Maximum C_O = 15 pF

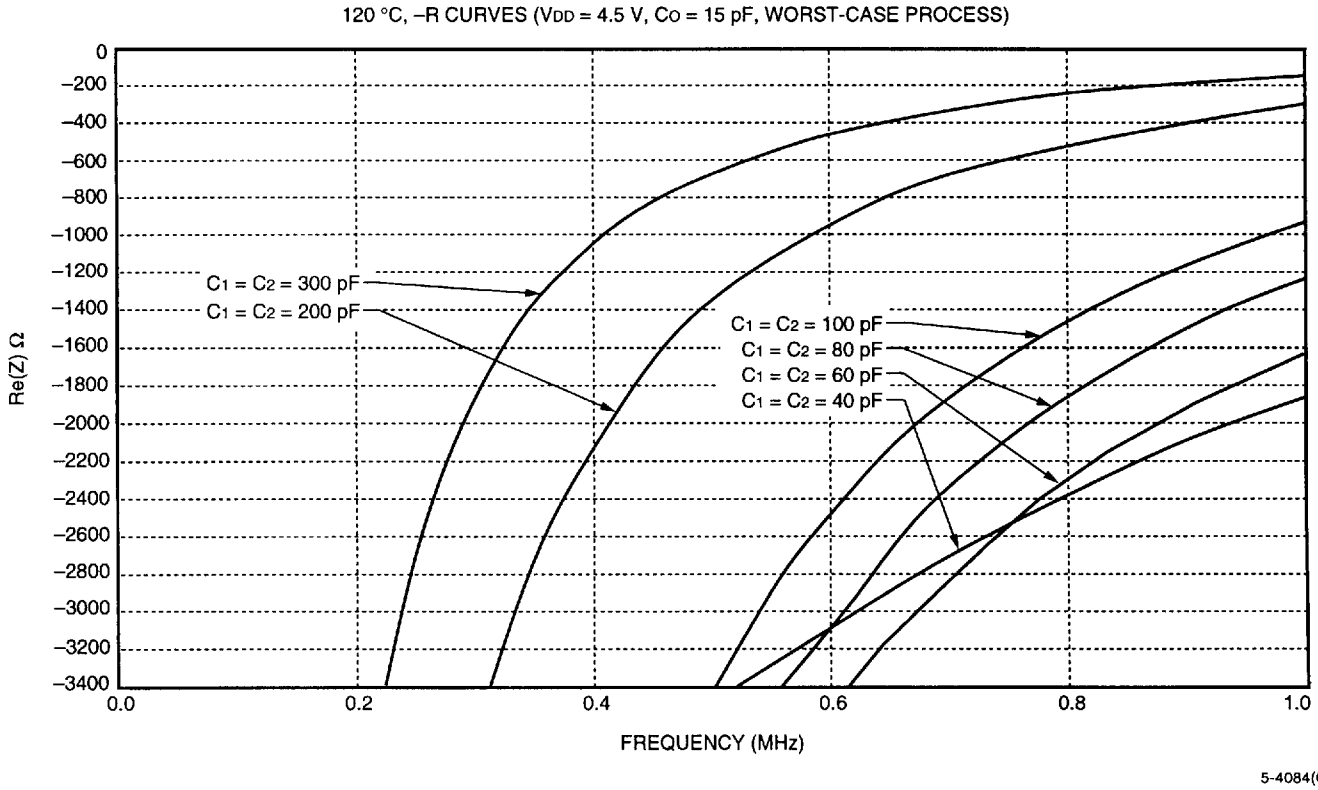


Figure 50. 5 V Low-Frequency Crystal Resonator Negative Resistance Curves

9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.2 Low-Frequency Crystal Oscillator or Resonator (continued)

9.2.4 Low-Frequency Crystal Resonator Negative Resistance Curves (continued)

Figure 51 shows worst-case negative resistance curves for a low-frequency crystal resonator operating with a 3.3 V power supply (V_{DD} = 3.0 V to 3.6 V). These worst-case conditions are as follows:

- Maximum Temperature = 120 °C
- Minimum V_{DD} = 3.0 V
- Maximum C_O = 15 pF

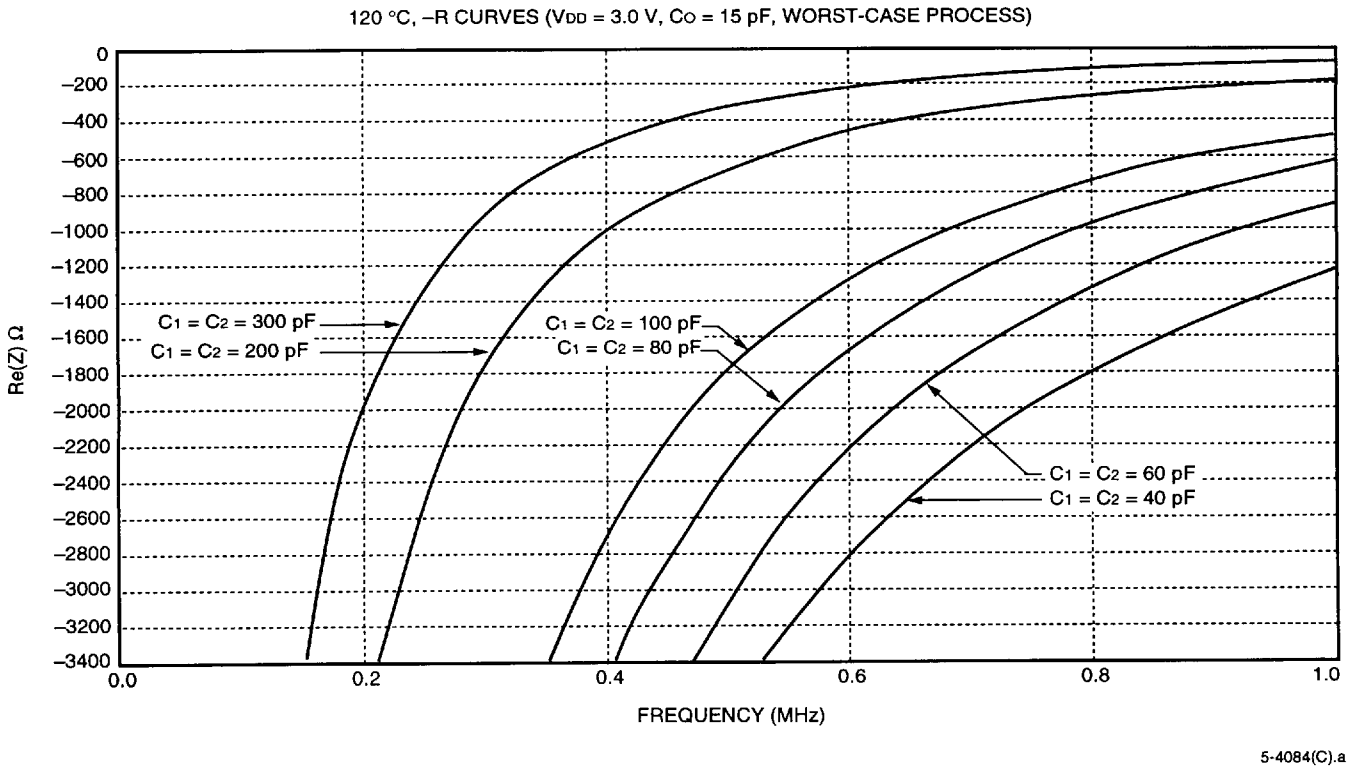


Figure 51. 3.3 V Low-Frequency Crystal Resonator Negative Resistance Curves

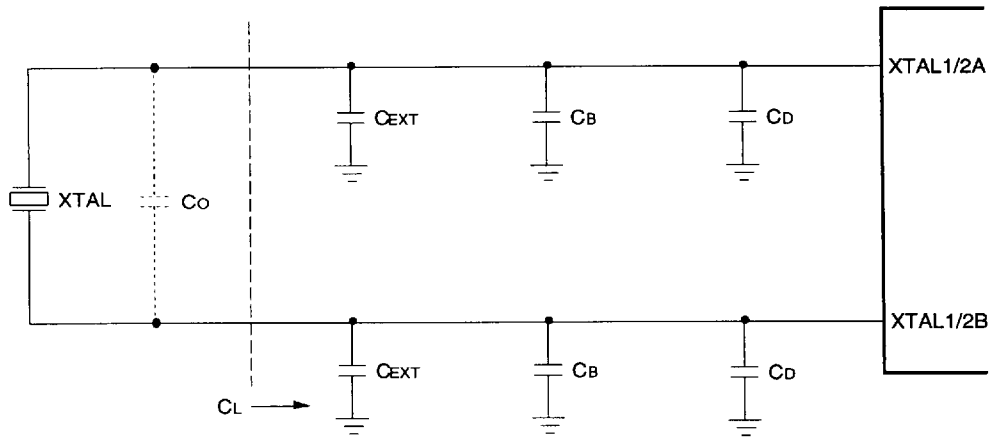
9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.3 Frequency Accuracy Considerations

For most applications, clock frequency errors in the hundreds of parts per million (ppm) can be tolerated with no adverse effect. However, for applications where precise frequency tolerance on the order 100 ppm is required, care must be taken in the choice of external components (crystal and capacitors) as well as in the layout of the printed-circuit board. Several factors determine the frequency accuracy of a crystal-based oscillator circuit. Some of these factors are determined by the properties of the crystal itself. Generally, a low-cost, standard crystal is not sufficient for a high-accuracy application, and a custom crystal must be specified. Most crystal manufacturers provide extensive information concerning the accuracy of their crystals, and an applications engineer from the crystal vendor should be consulted prior to specifying a crystal for a given application.

In addition to absolute, temperature, and aging tolerances of a crystal, the operating frequency of a crystal is also determined by the total load capacitance seen by the crystal. When ordering a crystal from a vendor, it is necessary to specify a load capacitance at which crystal operating frequency is measured. Variations in this load capacitance due to temperature and manufacturing variations cause variations in the operating frequency of the oscillator. Figure 52 illustrates some of the sources of this variation.

C_{EXT} = External load capacitor (one each required for XTAL1IN and XTAL1OUT)
C_D = Parasitic capacitance of the DSP1605 itself
C_B = Parasitic capacitance of the printed-wiring board
C_O = Parasitic capacitance of crystal (not part of C_L, but still a source of frequency variation)



5-4045(C)

Figure 52. Components of Load Capacitance for Crystal Oscillator

The load capacitance, C_L, must be specified to the crystal vendor. The crystal manufacturer cuts the crystal so that the frequency of oscillation is correct when the crystal sees this load capacitance. Note that C_L refers to a capacitance seen across the crystal leads, meaning that for the circuit shown in Figure 52, C_L is the series combination of the two external capacitors ($C_{EXT}/2$) plus the equivalent board and device strays ($C_B/2 + C_D/2$). For example, if 10 pF external capacitors were used and parasitic capacitance is neglected, the crystal should be specified for a load capacitance of 5 pF. If the load capacitance deviates from this value due to the tolerance on the external capacitors or the presence of parasitic capacitance, the frequency also deviates. This change in frequency as a function of load capacitance is known as pullability, which is expressed in units of ppm/pF.

9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.3 Frequency Accuracy Considerations (continued)

For small deviations of a few pF, pullability can be determined by the following equation.

$$\text{pullability(ppm/pF)} = \frac{(C_1)\,(10^6)}{2\,(C_O + C_L)^2}$$

where: C_O = parasitic capacitance of crystal
C_1 = motional capacitance of crystal (usually around 1 fF—25 fF, value can be obtained from crystal vendor)
C_L = total load capacitance seen by crystal

Note: For a given crystal, making C_L as large as possible can reduce pullability and improve frequency stability, while still maintaining sufficient negative resistance to ensure start-up according to the curves shown in Figures 44, 45, 48, and 50.

Because the exact values of the parasitic capacitance in a crystal-based oscillator system are unknown, the external capacitors are usually selected empirically to null out the frequency offset on a typical prototype board. Thus, if a crystal is specified to operate with a load capacitance of 15 pF, each external capacitor would have to be slightly less than 30 pF to account for parasitic capacitance. Suppose, for instance, that a crystal for which C_L = 15 pF is specified is plugged into the system and it is determined empirically that the best frequency accuracy occurs with C_{EXT} = 28 pF. This would mean that the equivalent board and device parasitic capacitance from each lead to ground would be 2 pF.

As an example, suppose it is desired to design a 26 MHz, 5.0 V system with 100 ppm frequency accuracy. The parameters for a typical high-accuracy, custom, 26 MHz fundamental mode crystal are as follows:

Initial Tolerance	10 ppm
Temperature Tolerance	25 ppm
Aging Tolerance	6 ppm
Series Resistance	20 Ω max.
Motional Capacitance (C_1)	5 fF max.
Parasitic Capacitance (C_O)	7 pF max.

To ensure oscillator start-up, the negative resistance of the oscillator with load and parasitic capacitance must be at least twice the series resistance of the crystal, or 40 Ω. Interpolating from Figure 44 on page 109, external capacitors plus strays can be made as large as 80 pF while still achieving 40 Ω of negative resistance. Assume for this example that external capacitors are chosen so that the total load capacitance including strays is 80 pF per lead, or 40 pF total. Thus, a load capacitance, C_L = 40 pF would be specified to the crystal manufacturer.

From the preceding equation, the pullability would be calculated as follows:

$$\text{pullability (ppm/pF)} = \frac{(C_1)\,(10^6)}{2\,(C_O + C_L)^2} = \frac{(0.015)\,(10^6)}{2\,(7 + 40)^2} = 3.4 \text{ ppm/pF}$$

If 2% external capacitors are used, the frequency deviation due to this variation is equal to:

(0.02)(40 pF)(3.4 ppm/pF) = 2.8 ppm

Note: To simplify analysis, C_{EXT} is considered to be 40 pF. In practice, it would be slightly less than this value to account for strays. Also, temperature and aging tolerance on the capacitors has been neglected.

9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.3 Frequency Accuracy Considerations (continued)

Typical capacitance variation of oscillator circuit in the DSP1605 itself across process, temperature, and supply voltage is ±1 pF. Thus, the expected frequency variation due to the DSP1605 is:

(1 pF)(3.4 ppm/pF) = 3.4 ppm

Other frequency accuracy considerations include the following:

- Approximate variation in parasitic capacitance of crystal = ±0.5 pF
- Frequency shift due to variation in Co = (0.5 pF)(3.4 ppm/pF) = 1.7 ppm
- Approximate variation in parasitic capacitance of printed-circuit board = ±1.5 pF
- Frequency shift due to variation in board capacitance = (1.5 pF)(3.4 ppm/pF) = 5.1 ppm

Therefore, the contributions to frequency variation add up as follows:

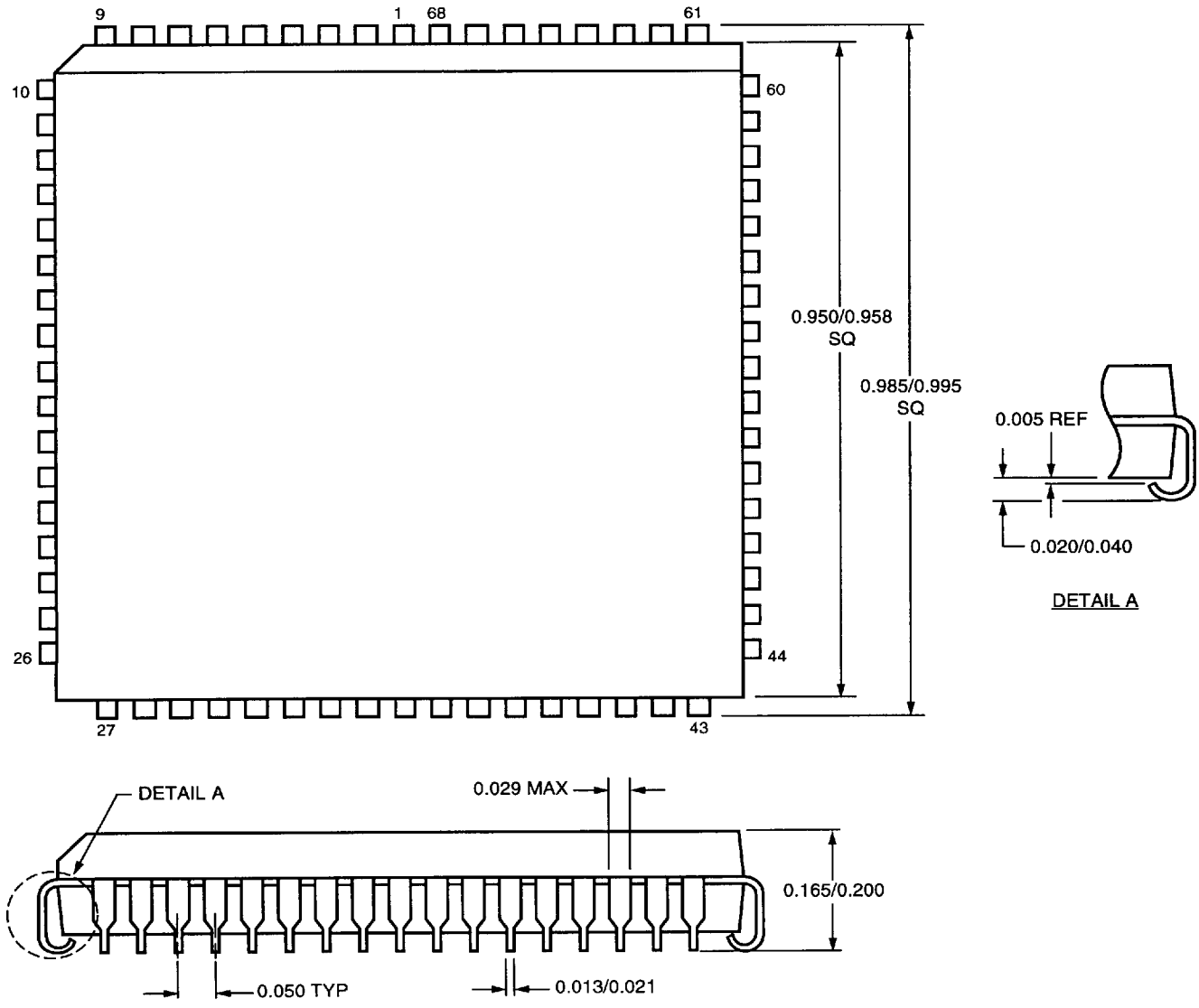
Initial Tolerance of Crystal =	10.0 ppm
Temperature Tolerance of Crystal =	25.0 ppm
Aging Tolerance of Crystal =	6.0 ppm
Load Capacitor Variation =	2.8 ppm
DSP1605 Circuit Variation =	3.4 ppm
Co Variation =	1.7 ppm
Board Variation =	5.1 ppm
Total =	54.0 ppm

This type of detailed analysis should be performed for any crystal-based application where frequency accuracy is critical.

10 Outline Diagrams

10.1 68-Pin PLCC Outline Diagram

Dimensions are in millimeters.

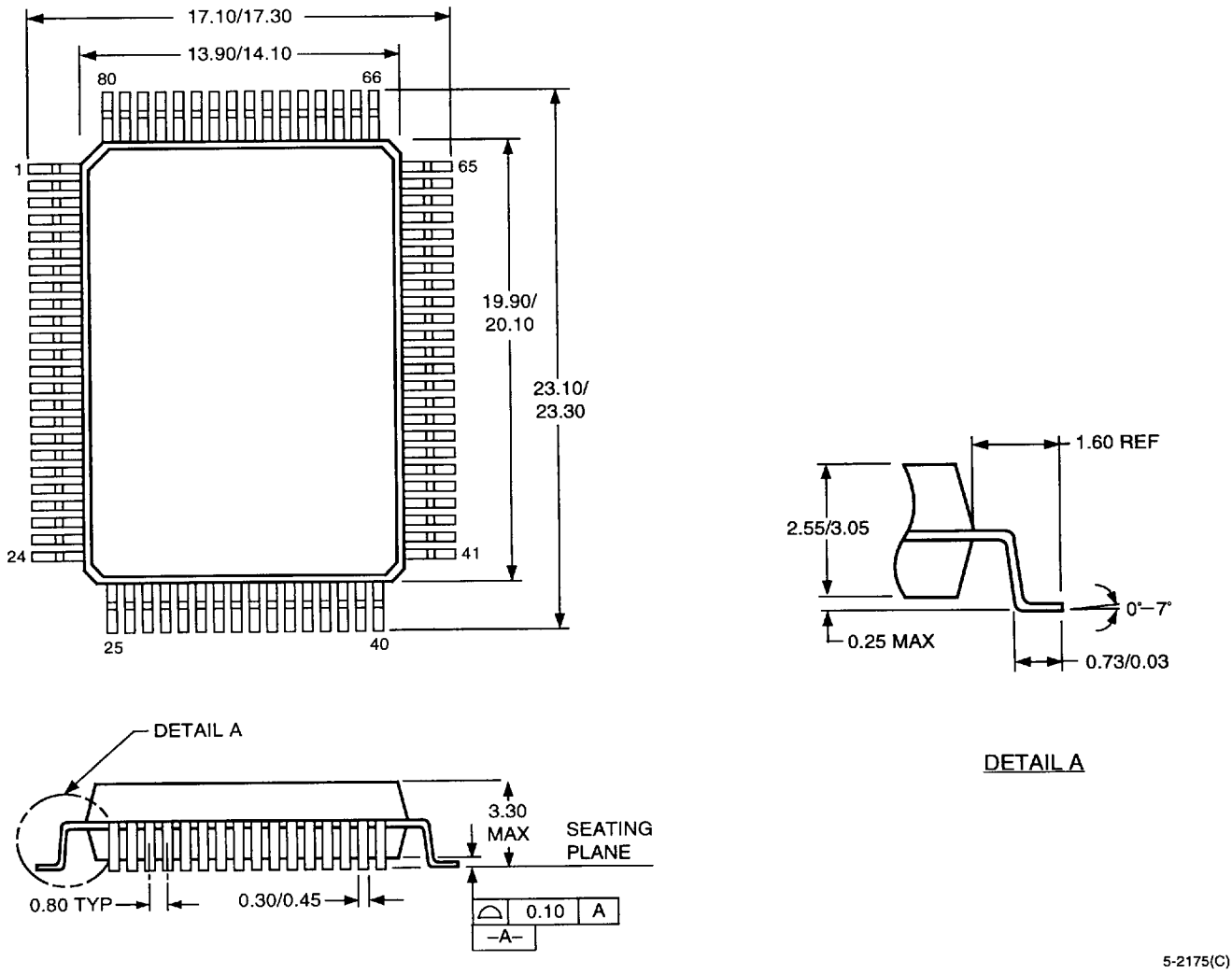


5-2139(C)

10 Outline Diagrams (continued)

10.2 80-Pin MQFP Outline Diagram

Dimensions are in millimeters.



11 Ordering Information

This section describes DSP160X device coding and mask-programmable options.

11.1 Device Coding

Table 132 defines each DSP160X part number character.

Table 132. DSP160X Device Coding

Part Number Character Positions (Left to Right)							
1—4	5	6—7	8	9—10	11—12	13	14
160X Family	Package (J = MQFP M = PLCC T = TQFP)	ROM Size (Number of 16-bit Kwords)	Designator (H = HD, – or A = No Designation, F = Flash ROM)	ROM Code ID (AA—ZZ) or Flash Pinout Option (P0 = 1604/06, P1 = 1605)	Instruction Cycle Time (ns)	Temperature Class (– or Blank = Commercial, I = Industrial)	Supply Voltage [Blank (V_{DD} = 4.5 V to 5.5 V) or T (V_{DD} = 3.0 V to 3.6 V)]
1603	J, M, or T	24	F	P0 or P1	30	– or Blank	Blank
					33	– or Blank	T
1604	J, M, or T	24 (maximum)	H, –, or A	AA—ZZ	25	– or Blank	Blank
					30	I, –, or Blank	
					31	I, –, or Blank	T
1605	J or M	16 (maximum)	H or –	AA—ZZ	25	– or Blank	Blank
					30	I, –, or Blank	
					31	I, –, or Blank	T
1605	J or M	16 (maximum)	F	– –	25	– or Blank	Blank
					30	– or Blank	
					33	– or Blank	T
1606	J, M, or T	24 (maximum)	H or –	AA—ZZ	25	– or Blank	Blank
					30	I, –, or Blank	
					31	I, –, or Blank	T

11.2 Mask-Programmable Options

The DSP1605 contains a ROM which is mask-programmable. Encoding a custom ROM selects the following programming options:

- Dual-channel/single-channel SIO. This feature allows the use of the SIO in dual-channel mode. Setting bit 15 (the DUAL bit) in the **sioc** register has no effect unless the dual-channel SIO mode was selected when the mask was encoded.
- Power supply. This option selects the operating voltage range for the device. The power-loss detect circuit for low V_{DD} is programmed through the mask to the proper voltage range. Testing is performed at the specified operating voltage.
- ROM security. This option protects the internal ROM contents by not allowing access to the instruction/coefficient memory map 3. Restricting access to memory map 3 makes it impossible to access IROM space when running from IRAM space.