Ordering number : EN7497A

SANYO Semiconductors
DATA SHEET

LB11922 — Monolithic Digital IC For OA Products Three-Phase Brushless Motor Driver

Overview

The LB11922 is a pre-driver IC designed for constantspeed control of 3-phase brushless motors. It can be used to implement a motor drive circuit with the desired output capacity (voltage, current) by using discrete transistors for the output stage. It implements direct PWM drive for minimal power loss.

Features

- Direct PWM drive output
- Speed discriminator + PLL speed control circuit
- Speed lock detection output
- Built-in crystal oscillator circuit
- Forward/reverse switching circuit
- Braking circuit (short braking)
- Full complement of on-chip protection circuits, including lock protection, current limiter, and thermal shutdown protection circuits.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		8	V
Maximum input current	IREG max	VREG pin	2	mA
Output current	I_O max	UH, VH, WH, UL, VL, and WL outputs	30	mA
Allowable power dissipation	Pd max1	Independent IC	0.62	W
	Pd max2	When Mounted on the specified PCB	1.36	W
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified circuit board : 114.3 × 76.1 × 1.6mm³ : glass epoxy board

Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		4.4 to 7.0	V
Input current range	IREG	VREG pin (7V)	0.2 to 1.5	mA
FG Schmitt output applied voltage	VFGS		0 to 7	V
FG Schmitt output current	IFGS		0 to 5	mA
Lock detection applied voltage	VLD		0 to 7	V
Lock detection output current	ILD		0 to 20	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 6.3V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	$I_{CC}1$			22	30.5	mA
	$I_{CC}2$	In stop mode		2.4	3.4	mA
	$I_{CC}3$	V_{CC} = 5V		21	28	mA
	$I_{CC}4$	V_{CC} = 5V, In stop mode		2.1	2.9	mA
Output saturation voltage 1-1	V_O sat1-1	At low level : I_O = 400μA		0.1	0.3	V
Output saturation voltage 1-2	V_O sat1-2	At low level : I_O = 10mA		0.8	1.2	V
Output saturation voltage 2	V_O sat2	At high level : I_O = -20mA	V_{CC}-1.2	V_{CC}-0.9		V
Hall Amplifier						
Input bias current	IHB (HA)		-2	-0.1		μA
Common-mode input voltage range 1	VICM1	When Hall-effect sensors are used	0.5		V_{CC}-2.0	V
Common-mode input voltage range 2	VICM2	When one-side biased inputs are used (Hall-effect IC applications)	0		V_{CC}	V
Hall input sensitivity		Sine wave	100			mVp-p
Hysteresis width	ΔVIN (HA)		20	30	50	mV
Input voltage low → high	VSLH		9	17	29	mV
Input voltage high → low	VSHL		-25	-13	-5	mV
PWM oscillator						
Output high-level voltage 1	V_{OH} (PWM)1		3.5	3.8	4.1	V
Output high-level voltage 2	V_{OH} (PWM)2	V_{CC} = 5V	2.75	3.0	3.25	V
Output low-level voltage 1	V_{OL} (PWM)1		1.8	2.1	2.4	V
Output low-level voltage 2	V_{OL} (PWM)2	V_{CC} = 5V	1.45	1.65	1.9	V
Oscillator frequency	f (PWM)	C = 560pF		22		kHz
Amplitude 1	V (PWM)1		1.4	1.7	2.0	Vp-p
Amplitude 2	V (PWM)2	V_{CC} = 5V	1.1	1.35	1.6	Vp-p
CSD circuit						
Output high-level voltage 1	V_{OH} (CSD)1		3.95	4.4	4.85	V
Output high-level voltage 2	V_{OH} (CSD)2	V_{CC} = 5V	3.15	3.5	3.85	V
Output low-level voltage 1	V_{OL} (CSD)1		1.1	1.4	1.7	V
Output low-level voltage 2	V_{OL} (CSD)2	V_{CC} = 5V	0.9	1.1	1.3	V
External capacitor charge current	ICHG1		-13	-9	-6	μA
External capacitor discharge current	ICHG2		8	12	16	μA
Oscillator frequency	f (RK)	C = 0.068μF		22		kHz
Amplitude 1	V (RK)1		2.65	3.0	3.35	Vp-p
Amplitude 2	V (RK)2	V_{CC} = 5V	2.1	2.4	2.65	Vp-p
Crystal Oscillator						
Operating frequency range	f_{OSC}		3		10	MHz
Low-level pin voltage	$V_{OSC}L$	I_{OSC} = -0.3mA		1.65		V
High-level pin current	$I_{OSC}H$	V_{OSC} = $V_{OSC}L$ + 0.3V		0.35		mA
Current Limiter Operation						
Limiter	VRF		0.235	0.260	0.285	V

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Thermal Shutdown Operation						
Thermal shutdown operating temperature	TSD	Design target value *	150	180		°C
Hysteresis width	ΔTSD	Design target value *		30		°C
VREG Pin						
VREG pin voltage	VREG	I = 500μA	6.6	7.0	7.4	V
Low-voltage Protection Circuit						
Operating voltage	VSDL		3.55	3.75	4.00	V
Release voltage	VSDH		3.85	4.03	4.25	V
Hysteresis width	ΔVSD		0.18	0.28	0.38	V
FG Amplifier						
Input offset voltage	V_{IO} (FG)		-10		+10	mV
Input bias current	IB (FG)		-1		+1	μA
Output high-level voltage 1	V_{OH} (FG)1	IFGI = -0.1mA, No load	4.2	4.6	5.0	V
Output high-level voltage 2	V_{OH} (FG)2	IFGI = -0.1mA, No load, V_{CC} = 5V	3.6	3.95	4.3	V
Output low-level voltage 1	V_{OL} (FG)1	IFGI = 0.1mA, No load	1.3	1.7	2.1	V
Output low-level voltage 2	V_{OL} (FG)2	IFGI = 0.1mA, No load, V_{CC} = 5V	0.7	1.05	1.4	V
FG input sensitivity		Gain : 100 ×	3			mV
Schmitt amplitude for the next stage			100	180	250	mV
Operating frequency range					2	kHz
Open-loop gain		f (FG) = 2kHz	45	51		dB
Reference voltage	VB (FG)		-5%	V_{CC}/2	5%	V
FGS Output						
Output saturation voltage	V_O (FGS)	I_O (FGS) = 2mA		0.2	0.4	V
Output low-level voltage	I_L (FGS)	V_O = V_{CC}			10	μA
Speed Discriminator Output						
Output high-level voltage	V_{OH} (D)		V_{CC}-1.0	V_{CC}-0.7		V
Output low-level voltage	V_{OL} (D)			0.8	1.1	V
Speed Control PLL Output						
Output high-level voltage	V_{OH} (P)1		4.05	4.30	4.65	V
	V_{OH} (P)2	V_{CC} = 5V	3.25	3.50	3.85	V
Output low-level voltage	V_{OL} (P)1		1.85	2.15	2.45	V
	V_{OL} (P)2	V_{CC} = 5V	1.25	1.60	1.85	V
Lock Detection						
Output saturation voltage	V_{OL} (LD)	ILD = 10mA		0.25	0.4	V
Output leakage current	I_L (LD)	V_O = V_{CC}			10	μA
Lock range			-6.25		+6.25	%
Integrator						
Input offset voltage	V_{IO} (INT)	Design target value *	-10		+10	mV
Input bias current	IB (INT)		-0.4		+0.4	μA
Output high-level voltage 1	V_{OH} (INT)1	IINTI = -0.1mA, No load	4.1	4.4	4.7	V
Output high-level voltage 2	V_{OH} (INT)2	IINTI = -0.1mA, No load, V_{CC} = 5V	3.45	3.7	3.95	V
Output low-level voltage 1	V_{OL} (INT)1	IINTI = 0.1mA, No load	1.2	1.4	1.65	V
Output low-level voltage 2	V_{OL} (INT)2	IINTI = 0.1mA, No load, V_{CC} = 5V	1.1	1.3	1.5	V
Open-loop gain			45	51		dB
Gain-bandwidth product		Design target value *		1.0		MHz
Reference voltage	VB (INT)	Design target value *	-5%	V_{CC}/2	5%	V

Note : * These items are design target values and are not tested.

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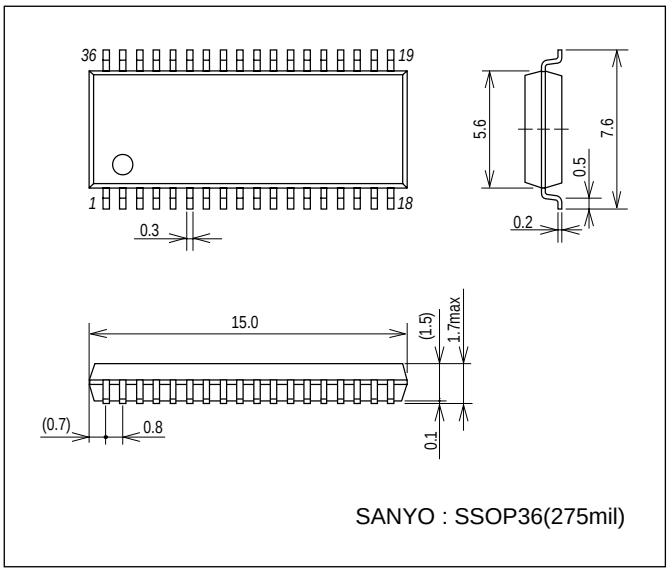
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
S/S Pin						
Input high-level voltage	V_{IH} (S/S)	V_{CC} = 6.3V, 5V	2.0		V_{CC}	V
Input low-level voltage	V_{IL} (S/S)	V_{CC} = 6.3V, 5V	0		1.0	V
Input open voltage	V_{IO} (S/S)		V_{CC}-0.5		V_{CC}	V
Hysteresis width	ΔV_{IN} (S/S)	V_{CC} = 6.3V, 5V	0.13	0.22	0.31	V
Input high-level current	I_{IH} (S/S)	VS/S = V_{CC}	-10	0	+10	µA
Input low-level current	I_{IL} (S/S)	VS/S = 0V	-170	-118		µA
Pull-up resistance	RU (S/S)		37	53.5	70	kΩ
F/R Pin						
Input high-level voltage	V_{IH} (F/R)	V_{CC} = 6.3V, 5V	2.0		V_{CC}	V
Input low-level voltage	V_{IL} (F/R)	V_{CC} = 6.3V, 5V	0		1.0	V
Input open voltage	V_{IO} (F/R)		V_{CC}-0.5		V_{CC}	V
Hysteresis width	ΔV_{IN} (F/R)	V_{CC} = 6.3V, 5V	0.13	0.22	0.31	V
Input high-level current	I_{IH} (F/R)	VF/R = V_{CC}	-10	0	+10	µA
Input low-level current	I_{IL} (F/R)	VF/R = 0V	-170	-118		µA
Pull-up resistance	RU (F/R)		37	53.5	70	kΩ
BR Pin						
Input high-level voltage	V_{IH} (BR)	V_{CC} = 6.3V, 5V	2.0		V_{CC}	V
Input low-level voltage	V_{IL} (BR)	V_{CC} = 6.3V, 5V	0		1.0	V
Input open voltage	V_{IO} (BR)		V_{CC}-0.5		V_{CC}	V
Hysteresis width	ΔV_{IN} (BR)	V_{CC} = 6.3V, 5V	0.13	0.22	0.31	V
Input high-level current	I_{IH} (BR)	VBR = V_{CC}	-10	0	+10	µA
Input low-level current	I_{IL} (BR)	VBR = 0V	-170	-118		µA
Pull-up resistance	RU (BR)		37	53.5	70	kΩ
N Pin						
Input high-level voltage	V_{IH} (N)	V_{CC} = 6.3V, 5V	2.0		V_{CC}	V
Input low-level voltage	V_{IL} (N)	V_{CC} = 6.3V, 5V	0		1.0	V
Input open voltage	V_{IO} (N)		V_{CC}-0.5		V_{CC}	V
Hysteresis width	ΔV_{IN} (N)	V_{CC} = 6.3V, 5V, Design target value *	0.13	0.22	0.31	V
Input high-level current	I_{IH} (N)	V_N = V_{CC}	-10	0	+10	µA
Input low-level current	I_{IL} (N)	V_N = 0V	-170	-118		µA
Pull-up resistance	RU (N)		37	53.5	70	kΩ

Note : * These items are design target values and are not tested.

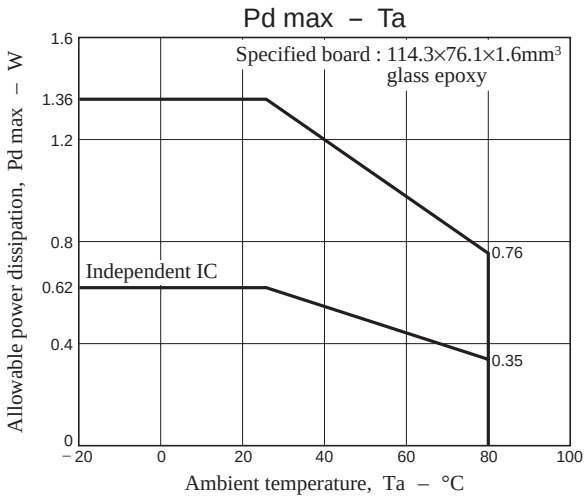
Package Dimensions

unit : mm (typ)

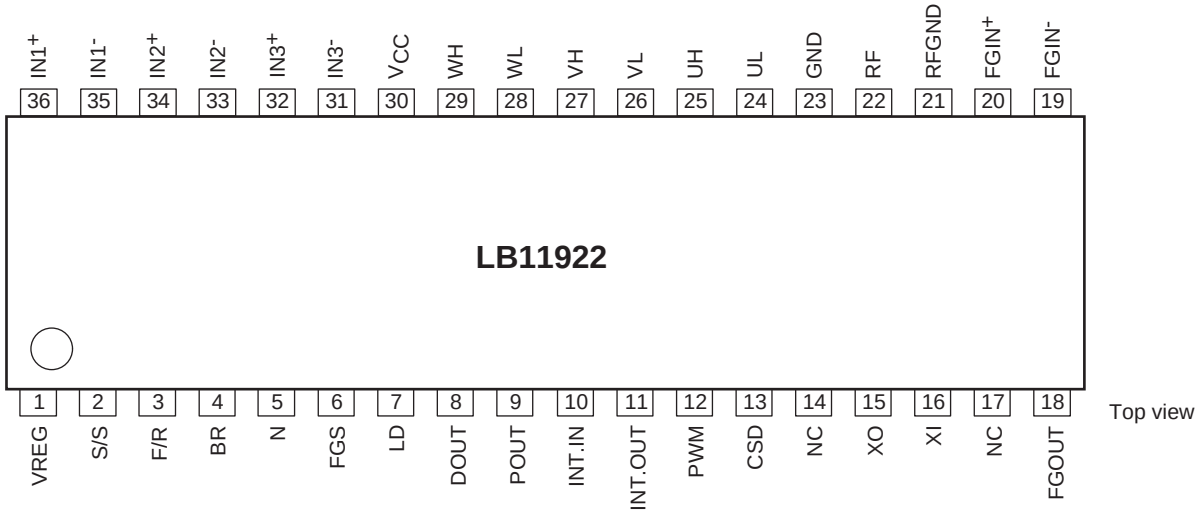
3247A



SANYO : SSOP36(275mil)



Pin Assignment



Top view

Speed Discriminator Counts

N	Number of counts
High or open	512
Low	1024

$f_{FG} = f_{OSC} \div (16 \times$ <number of counts>)

Three-Phase Logic Truth Table (A high (H) input is the state where $IN^+ > IN^-$.)

Item	F/R = L			F/R = H			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	PWM	-
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

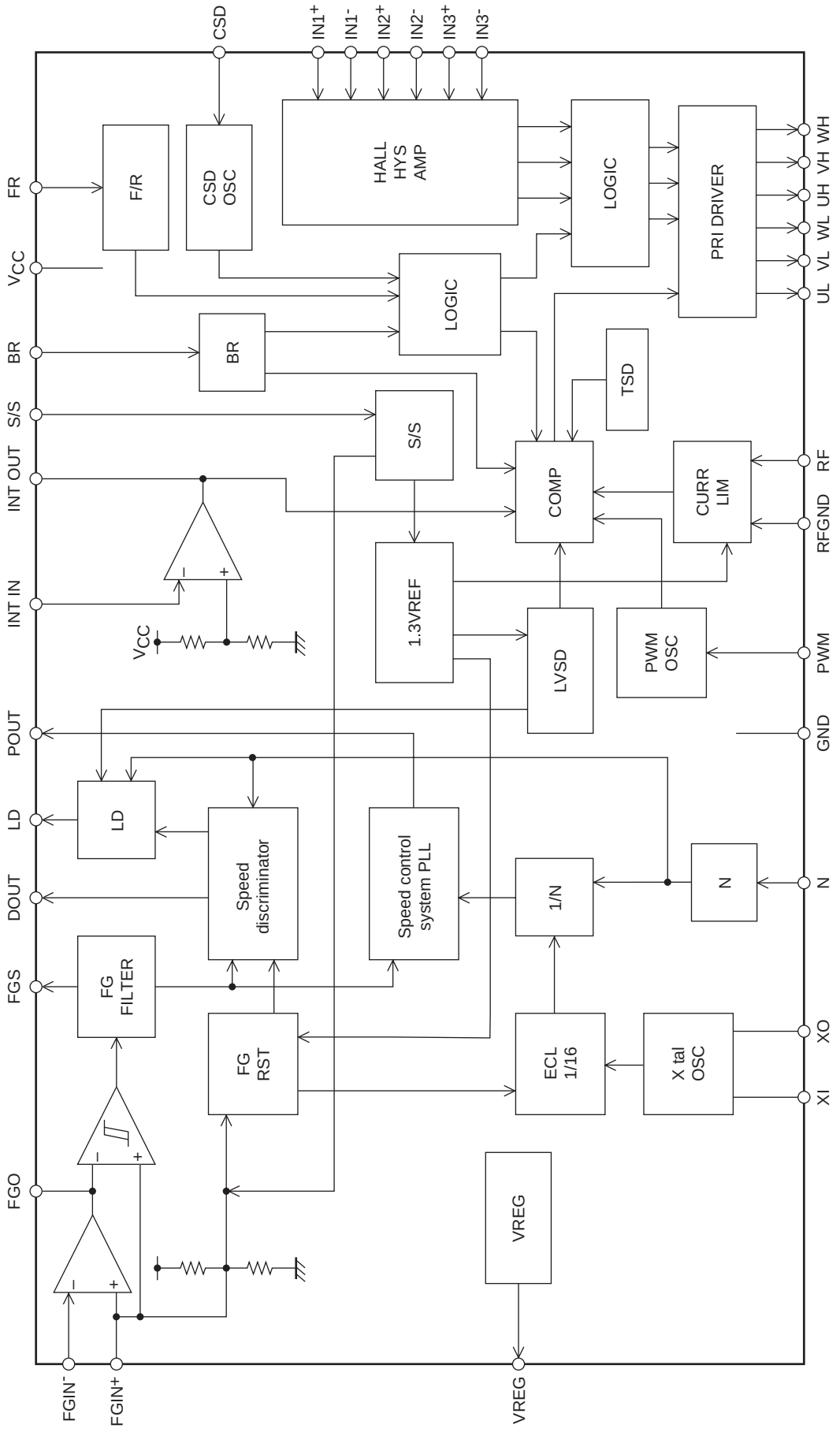
S/S pin

Input condition	Condition
High or open	Stop
Low	Start

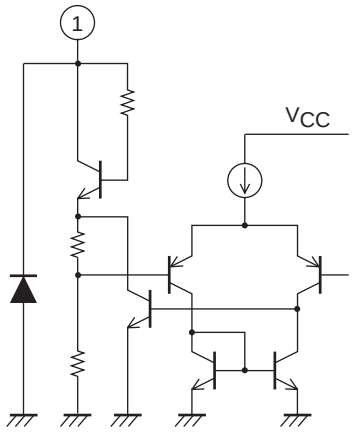
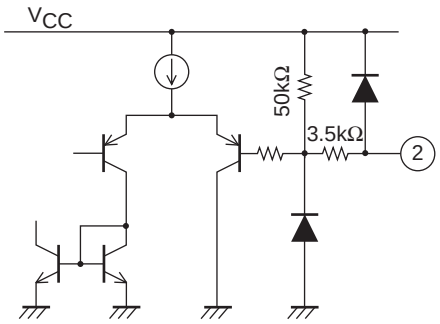
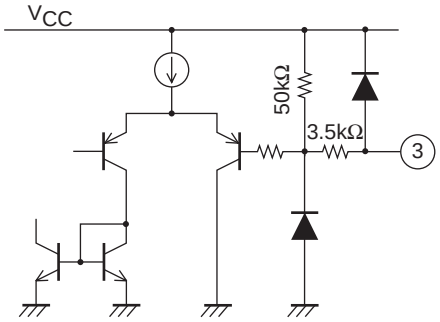
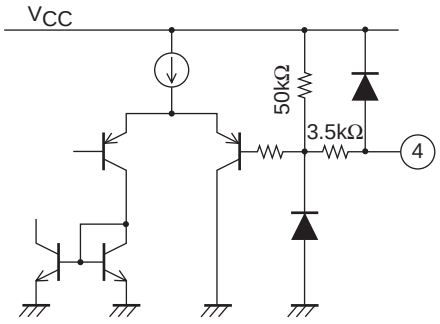
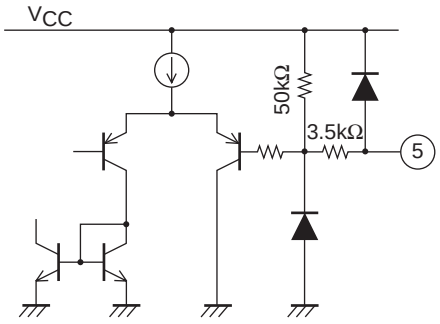
BRK pin

Input condition	Condition
High or open	Brake
Low	Released

Block Diagram



Pin Functions

Pin No.	Pin name	Function	Equivalent circuit
1	VREG	7V shunt regulator output.	
2	S/S	Start/stop control. Low : 0 to 1.0V High : 2.0V to V_{CC} Goes high when left open. Low for start. High or open for stop. The hysteresis is about 0.22V.	
3	F/R	Forward/reverse control. Low : 0 to 1.0V High : 2.0V to V_{CC} Goes high when left open. Low for forward. High or open for reverse. The hysteresis is about 0.22V.	
4	BR	Brake control (short braking operation). Low : 0 to 1.0V High : 2.0V to V_{CC} Goes high when left open. High or open for brake mode operation. The hysteresis is about 0.22V.	
5	N	Speed discriminator count switching. Low : 0 to 1.0V High : 2.0V to V_{CC} Goes high when left open. The hysteresis is about 0.22V.	

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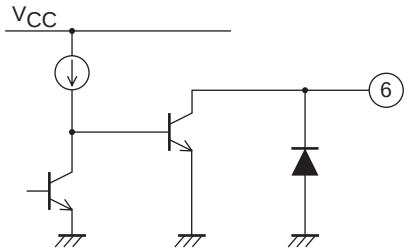
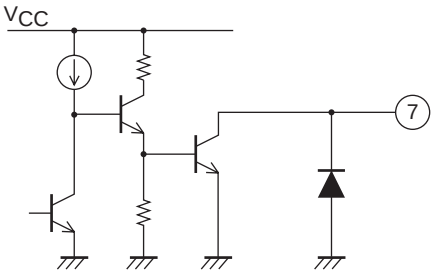
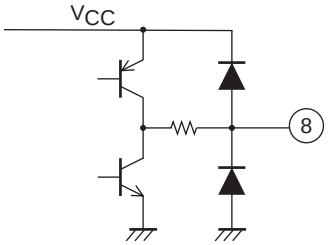
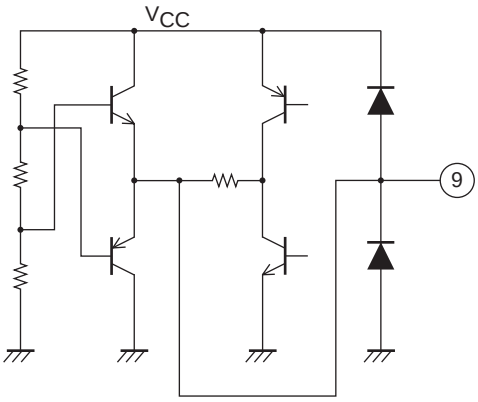
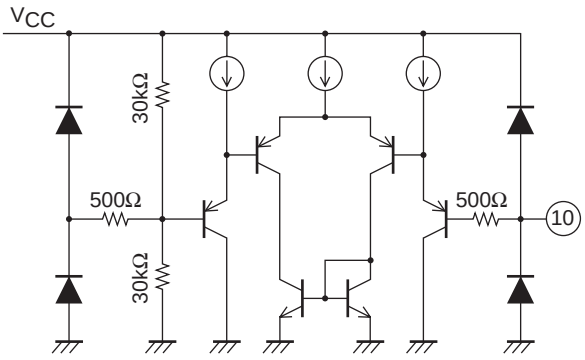
Pin No.	Pin name	Function	Equivalent circuit
6	FGS	FG amplifier output (after the Schmitt circuit). This is an open collector output.	
7	LD	Speed lock detection output. Goes low when the motor speed is within the speed lock range (±6.25%).	
8	DOUT	Speed discriminator output. Acceleration → high, deceleration → low	
9	POUT	Speed control system PLL output. Outputs the phase comparison result for CLK and FG.	
10	INT IN	Integrating amplifier inverting input.	

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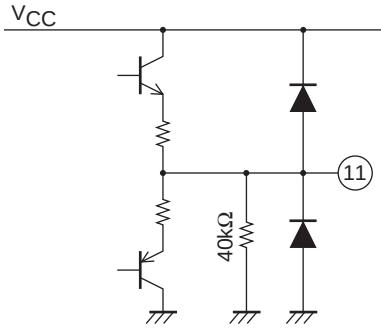
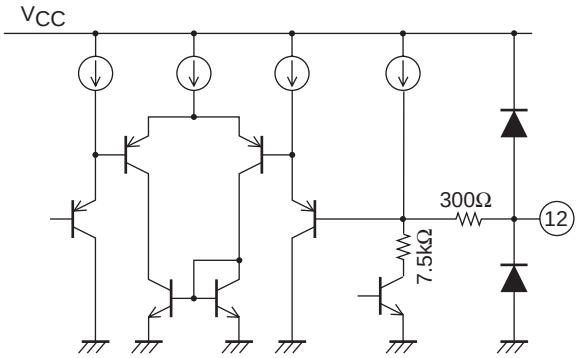
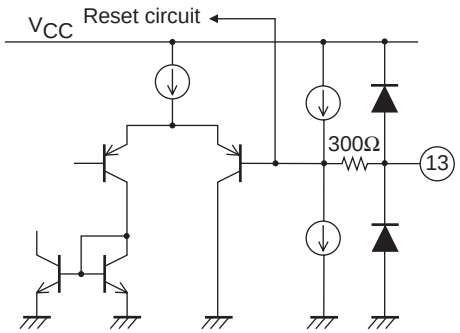
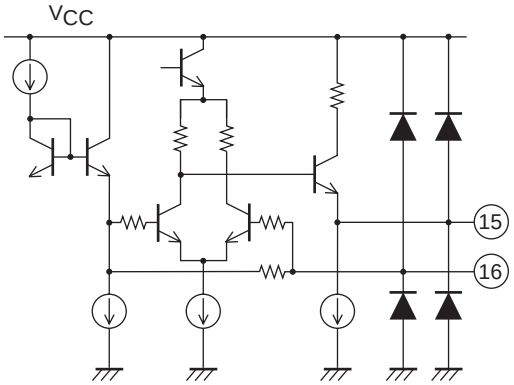
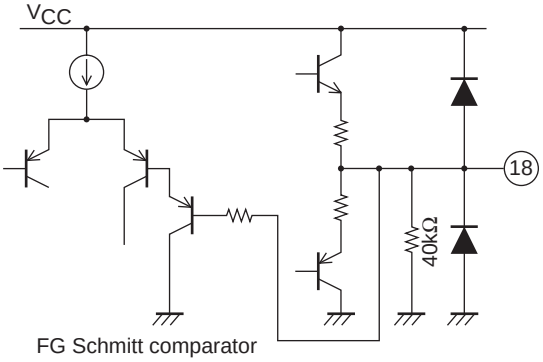
Pin No.	Pin name	Function	Equivalent circuit
11	INT OUT	Integrating amplifier output (speed control).	
12	PWM	PWM oscillator frequency setting. Connect a capacitor between this pin and ground.	
13	CSD	Sets the operating time of the constrained-rotor protection circuit. Reference signal oscillator used when the clock signal is cut off and to prevent malfunctions. The protection function operating time can be set by connecting a capacitor between this pin and ground. This pin also functions as the logic circuit block power-on reset pin.	
15 16	XO XI	Oscillator circuit connections. XO : Output pin XI : Input pin A reference clock can be generated by connecting an oscillator element to these pins. If an external clock with a frequency of a few MHz is used, input that signal through a series resistor of about 5.1kΩ. The XO pin must be left open in this case.	
18	FGOUT	FG amplifier output. This pin is connected to the FG Schmitt comparator circuit internally in the IC.	

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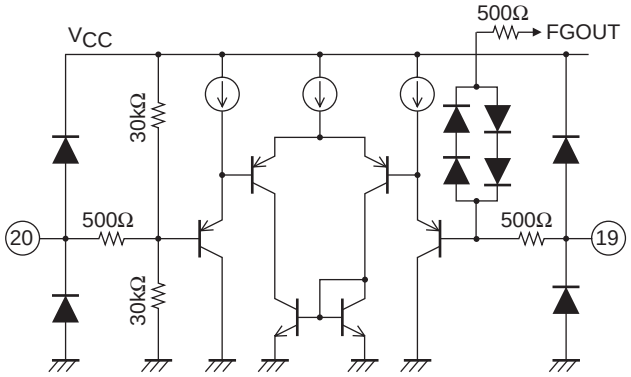
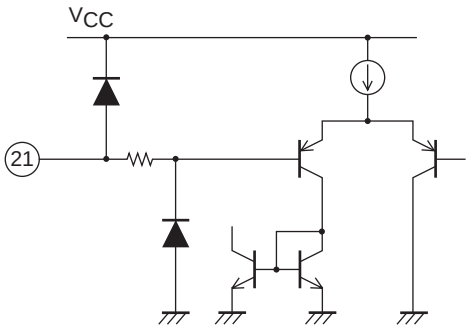
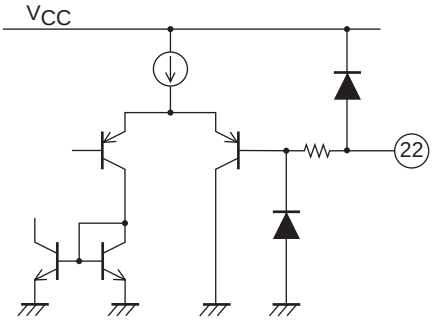
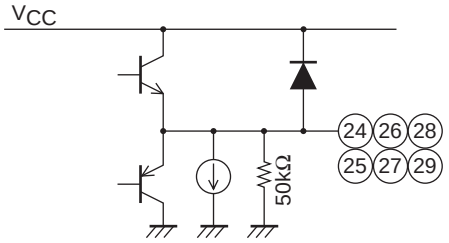
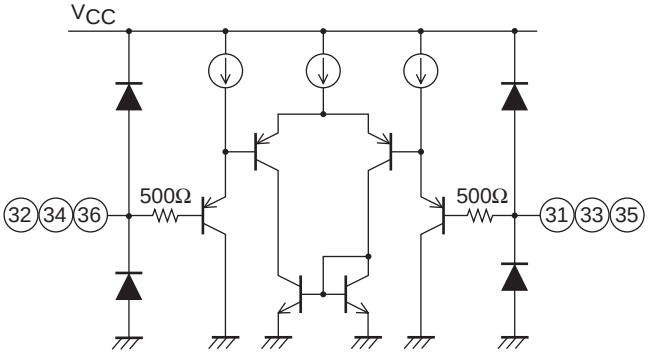
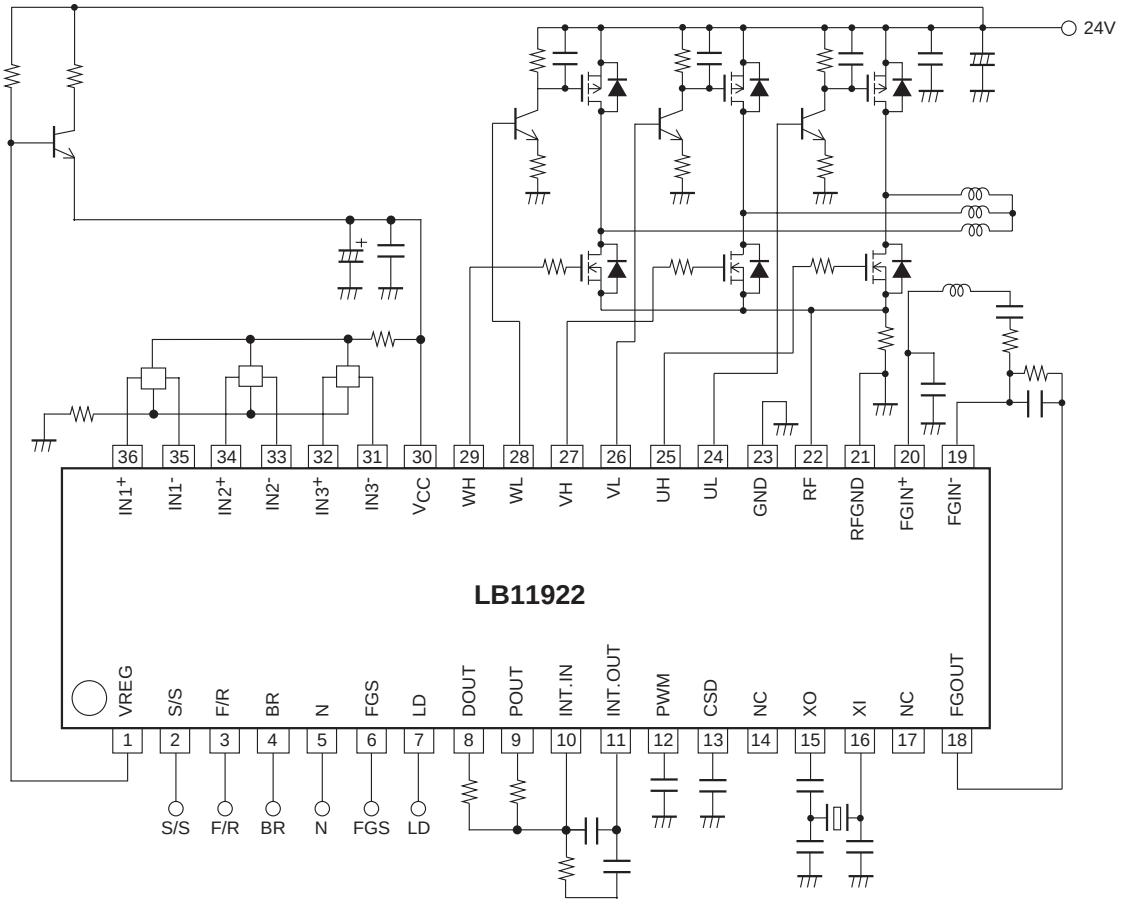
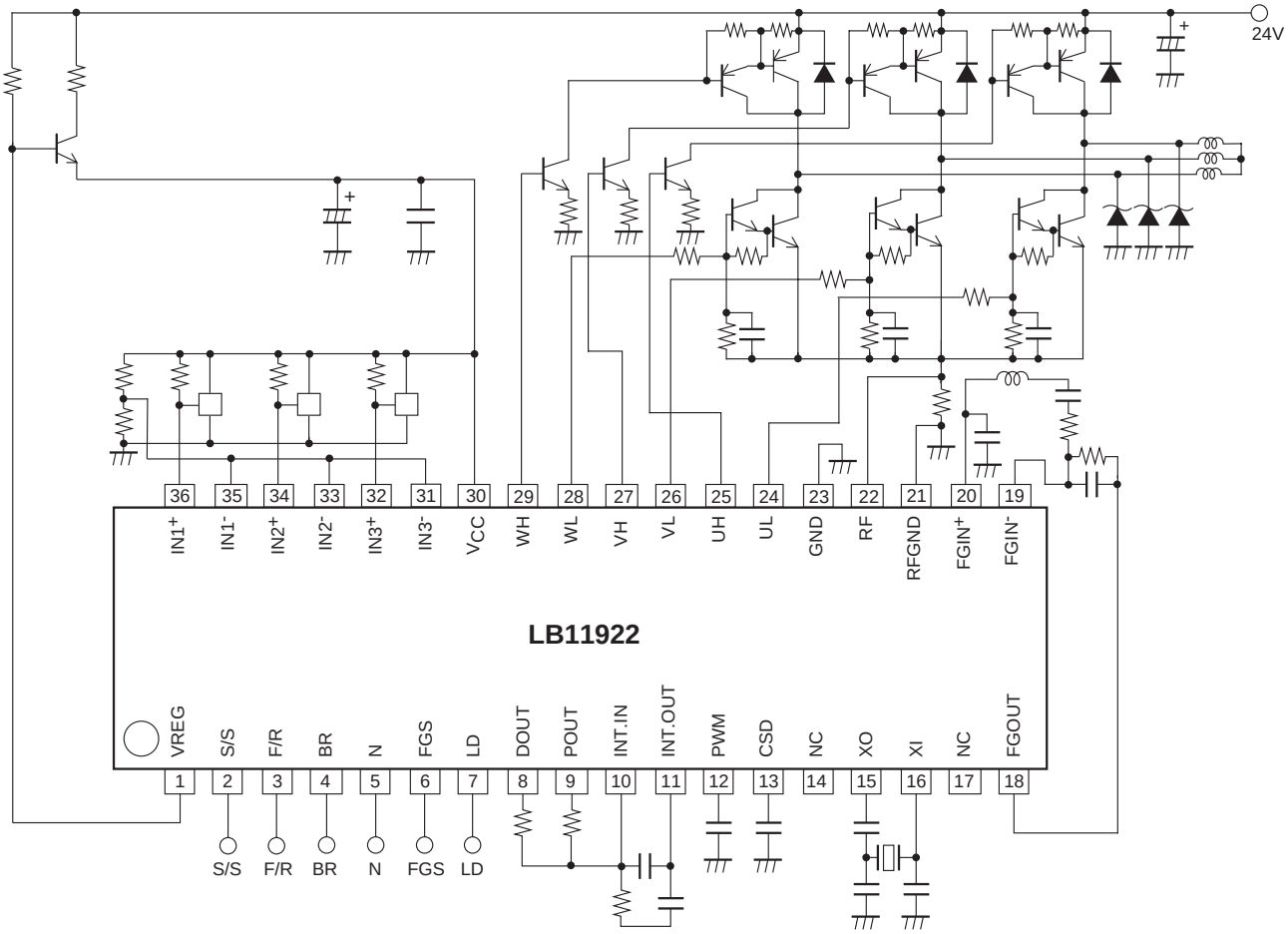
Pin No.	Pin name	Function	Equivalent circuit
19 20	$FGIN^-$ $FGIN^+$	FG amplifier inputs. $FGIN^-$: FG amplifier inverting input $FGIN^+$: FG amplifier noninverting input Insert capacitors between these pins (which have a potential of 1/2 V_{CC}) and ground.	
21	RFGND	Output current detection. Connect a resistor between this pin and ground.	
22	RF	Output current detection. Connect a resistor between this pin and ground. The output limitation maximum current, I_{OUT}, is set to be 0.26/Rf by this resistor.	
23	GND	Ground connection.	
24 25 26 27 28 29	UL UH VL VH WL WH	Outputs (that are used to drive external transistors). These are push-pull outputs. The PWM duty is controlled on the UH, VH, and WH side of these outputs.	
30	V_{CC}	Power-supply voltage. Connect a capacitor between this pin and ground for power supply stabilization.	
31 32 33 34 35 36	$IN3^-$ $IN3^+$ $IN2^-$ $IN2^+$ $IN1^-$ $IN1^+$	Hall-effect device inputs. The input is seen as a high-level input when $IN^+ > IN^-$, and as a low-level input for the opposite state. If noise on the Hall-effect device signals is a problem, insert capacitors between the corresponding IN^+ and IN^- inputs. The logic high state indicates that $V_{IN}^+ > V_{IN}^-$.	
14 17	NC	These are unconnected pins, and can be used for wiring.	

Sample Application Circuit 1 (P-channel + n-channel, Hall-effect sensor application)



Sample Application Circuit 2 (PNP + NPN, Hall-effect sensor application)



LB11922 Description

1. Speed Control Circuit

This IC implements speed control using the combination of a speed discriminator circuit and a PLL circuit. The speed discriminator circuit outputs (This counts a single FG period.) an error signal once every two FG periods. The PLL circuit outputs an error signal once every one FG Period. As compared to the earlier technique in which only a speed discriminator circuit was used, the combination of a speed discriminator and a PLL circuit allows variations in motor speed to be better suppressed when a motor that has large load variations is used. The FG servo frequency (f_{FG}) is controlled to have the following relationship with the crystal oscillator frequency (f_{OSC}).

$f_{FG} = f_{OSC} \div (16 \times$ <number of counts>)

N	Number of counts
High or open	512
Low	1024

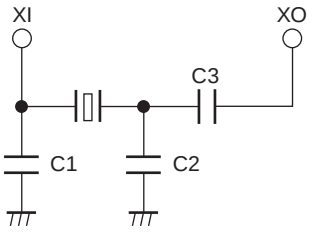
Therefore it is possible to implement half-speed control without switching the clock frequency by using combinations of the N1 = high, N2 = low state and other setting states.

2. Reference Clock

This IC supports the use of either of the following methods for providing the speed control reference clock.

(1) Crystal oscillator

Use a circuit consisting of a crystal and capacitors such as the one shown below to implement a crystal oscillator.



C1 : Used to prevent oscillation at upper harmonic frequencies.
C2 : Used for stabilization and to prevent oscillation at upper harmonic frequencies.
C3 : Used for oscillator coupling.

Oscillator frequency (MHz)	C1 (pF)	C2 (pF)	C3 (pF)
3 to 5	39	10	47
5 to 8	10	10	47
8 to 10	5	10	22

(Values provided for reference purposes)

This circuit and these component values are only provided for reference purposes. When implementing a crystal oscillator in an application, it is necessary to consult the manufacturer of the crystal to verify that problems will not occur due to interactions between stray capacitances due to wiring in the PCB and the crystal.

Notes :

The capacitor C1 is effective at lowering negative resistance values at high frequencies, but care is required to assure that it does not excessively reduce the negative resistance at the fundamental frequency.

Since this crystal oscillator circuit is a high-frequency circuit, it can be easily influenced by stray capacitances on the PCB. To minimize stray capacitances, keep connections between external components as short as possible and use narrower line widths in the PCB patter.

The C1 and C2 ground lines must be as short as possible, and must be connected to the IC's ground pin (pin 23, GND). If the PCB lines are excessively long, the oscillator circuit may be influenced by fluctuations in the ground line voltage when, for example, the motor is overloaded, and the oscillator frequency may change. The C1 and C2 ground lines can be made shorter by using the NC pins next to the XI and XO pins for the C1 and C2 ground, and connecting those pins across the back of the IC to the IC GND pin.

(2) External clock (A frequency equivalent to that of the crystal oscillator circuit : a few MHz)

If a signal from an external signal source with a frequency equivalent to that of the crystal oscillator circuit is used, input that signal to the IC through a series resistor (example value : 5.1kΩ). In this case, the XO pin must be left open.

Input signal levels (signal source)
Low-level voltage : 0 to 0.8V
High-level voltage : 2.5 to 5.0V

3. Output Drive Circuit

To reduce power loss in the output, this IC adopts the direct PWM drive technique. The output transistors (which are external to the IC) are always saturated when on, and the motor drive output is adjusted by changing the duty with which the output is on. The PWM switching is performed on the high side for each phase (UH, VH, and WH). The PWM switching side in the output can be selected to be either the high or low side depending on how the external transistors are connected.

4. Current Limiter Circuit

The current limiter circuit limits the (peak) current at the value $I = V_{RF}/R_f$ (V_{RF} = 0.26V (typical), R_f : current detection resistor). The current limitation operation consists of reducing the output duty to suppress the current. High accuracy detection can be achieved by connecting the RF and RFGND pin lines near the ends of the current detection resistor (R_f).

5. Speed Lock Range

The speed lock range is ±6.25% of the fixed speed. When the motor speed is in the lock range, the LD pin (an open collector output) goes low. If the motor speed goes out of the lock range, the motor on duty is adjusted according to the speed error to control the motor speed to be within the lock range.

6. Notes on the PWM Frequency

The PWM frequency is determined by the capacitor (F) connected to the PWM pin.

When V_{CC} = 6.3V : $f_{PWM} \approx 1/(82000 \times C)$
When V_{CC} = 5.0V : $f_{PWM} \approx 1/(66000 \times C)$

A PWM frequency of between 15 and 25kHz is desirable. If the PWM frequency is too low, the motor may resonate at the PWM frequency during motor control, and if that frequency is in the audible range, that resonation may result in audible noise. If the PWM frequency is too high, the output transistor switching loss will increase. To make the circuit less susceptible to noise, the connected capacitors must be connected to the GND pin (pin 23) with lines that are as short as possible.

7. Hall effect sensor input signals

An input amplitude of over 100mVp-p is desirable in the Hall effect sensor inputs. The closer the input waveform is to a square wave, the lower the required input amplitude. Inversely, a higher input amplitude is required the closer the input waveform is to a triangular wave. Also note that the input DC voltage must be set to be within the commonmode input voltage range.

If noise on the Hall inputs is a problem, that noise must be excluded by inserting capacitors across the inputs. Those capacitors must be located as close as possible to the input pins.

When the Hall inputs for all three phases are in the same state, all the outputs will be in the off state.

If a Hall sensor IC is used to provide the Hall inputs, those signals can be input to one side (either the + or - side) of the Hall effect sensor signal inputs as 0 to V_{CC} level signals if the other side is held fixed at a voltage within the common-mode input voltage range that applies when a Hall effect sensors are used.

8. Forward/Reverse Switching

The motor rotation direction can be switched using the F/R pin. However, the following notes must be observed if the motor direction is switched while the motor is turning.

- This IC is designed to avoid through currents when switching directions. However, increases in the motor supply voltage (due to instantaneous return of motor current to the power supply) during direction switching may cause problems. The values of the capacitors inserted between power and ground must be increased if this increase is excessive.
- If the motor current after direction switching exceeds the current limit value, the PWM drive side outputs will be turned off, but the opposite side output will be in the short-circuit braking state, and a current determined by the motor back EMF voltage and the coil resistance will flow. Applications must be designed so that this current does not exceed the ratings of the output transistors used. (The higher the motor speed at which the direction is switched, the more severe this problem becomes.)

9. Brake Switching

The LB11922 provides short-circuit braking implemented by turning the output transistors for the high side for all phases (UH, VH, and WH) on. (The opposite side transistors are turned off for all phases.) Note that the current limiter does not operate during braking. During braking, the duty is set to 100%, regardless of the motor speed. The current that flows in the output transistors during braking is determined by the motor back EMF voltage and the coil resistance. Applications must be designed so that this current does not exceed the ratings of the output transistors used. (The higher the motor speed at which braking is applied, the more severe this problem becomes.)

The braking function can be applied and released with the IC in the start state. This means that motor startup and stop control can be performed using the brake pin with the S/S pin held at the low level (the start state).

10. Constraint Protection Circuit

The LB1922M includes an on-chip constraint protection circuit to protect the IC and the motor in motor constraint mode. If the LD output remains high (indicating the locked state) for a fixed period in the start state, the upper side (external) transistors are turned off. This time is set by the capacitance of the capacitor attached to the CSD pin.

When V_{CC} = 6.3V : The set time (in seconds) is 74 × C (μF)

When V_{CC} = 5.0V : The set time (in seconds) is 60 × C (μF)

To clear the rotor constrained protection state, the application must either switch to the stop state for a fixed period (about 1ms or longer) or turn off and reapply power.

If the rotor constrained protection circuit is not used, a 220kΩ resistor and a 1500pF capacitor must be connected in parallel between the CSD pin and ground. Since the CSD pin also functions as the power-on reset pin, if the CSD pin were connected directly to ground, the IC would go to the power-on reset state and motor drive operation would remain off. The power-on reset state is cleared when the CSD pin voltage rises above a level of about 0.64V.

11. Low-Voltage Protection Circuit

The LB11922 includes a low-voltage protection circuit to protect against incorrect operation when power is first applied or if the power-supply voltage (V_{CC}) falls. The (external) upper side output transistors are turned off if V_{CC} falls under about 3.75V (tpyical), and this function is cleared at about 4.0V (typical).

12. Power Supply Stabilization

Since this IC is used in applications that draw large output currents, the power-supply line is subject to fluctuations. Therefore, capacitors with capacitances adequate to stabilize the power-supply voltage must be connected between the V_{CC} pin and ground. If diodes are inserted in the power-supply line to prevent IC destruction due to reverse power supply connection, since this makes the power-supply voltage even more subject to fluctuations, even larger capacitors will be required.

13. Ground Lines

The signal system ground and the output system ground must be separated and a single ground point must be taken at the connector. Since the output system ground carries large currents, this ground line must be made as short as possible.

Output system ground ... Ground for Rf and the output diodes

Signal system ground ... Ground for the IC and the IC external components

14. VREG Pin

If a motor drive system is formed from a single power supply, the VREG pin (pin 1) can be used to create the powersupply voltage (about 6.3V) for this IC. The VREG pin is a shunt regulator and generates a voltage of about 7V by passing a current through an external resistor. A stable voltage can be generated by setting the current to value in the range 0.2 to 1.5mA. The external transistors must have current capacities of at least 80mA (to cover the I_{CC} + Hall bias current + output current <source> requirements) and they must have voltage handling capacities in excess of the motor power-supply voltage. Since the heat generated by these transistor may be a problem, heat sinks may be required depending on the packages used. If the IC power-supply voltage (4.4 to 7.0V) is provided from an external circuit, apply that voltage directly to the V_{CC} pin (pin 30). In that case, the VREG pin must either be left open or connected to ground.

15. FG Amplifier

The FG amplifier is normally implemented as a filter amplifier such as that shown in the application circuits to reject noise. Since a clamp circuit has been added at the FG amplifier output, the output amplitude is clamped at about 3Vp-p, even if the gain is increased.

Since a Schmitt comparator is inserted after the FG amplifier, applications must set the gain so that the amplifier output amplitude is at least 250mVp-p. (It is desirable that the gain be set so that the amplitude is over 0.5Vp-p at the lowest controlled speed to be used.)

The capacitor inserted between the $FGIN^+$ pin (pin 20) and ground is required for bias voltage stabilization. To make the connected capacitor as immune from noise as possible, connect this capacitor to the GND pin (pin 23) with a line that is as short as possible.

16. Integrating Amplifier

The integrating amplifier integrates the speed error pulses and the phase error pulses and converts them to a speed command voltage. At the same time it also sets the control loop gain and frequency characteristics using external components.

17. NC pin

Since the NC pins are electrically open with respect to the IC itself, they can be used as intermediate connection points for lines in the PCB pattern.