No. 2156A

LC6554D, 6554H

CMOS LSI

4K-Byte ROM-Contained Single-Chip 4-Bit Microcomputers With FLT, LED Drivers

The LC6554D/H are single-chip 4-bit microcomputers that contain a 4K-byte ROM, 1K-bit RAM, and have 64 pins. The LC6554D/H have 57 pins for ports — 28 pins for 7 input/output common ports, 21 pins for 6 output ports, and 8 pins for 2 input ports. The LC6554D/H have specific ports that are used to provide the interrupt function, 4-bit/8-bit serial input/output function and burst pulse output function. Each of the 28 pins for input/output common ports contains a driver with a withstand voltage of 15V max. and a drive current of 15mA max. and each of the 21 pins for output ports contains a high-voltage output driver of the P-channel open drain type. Since the high-voltage output driver can be used as general-purpose high-current driver as well as fluorescent tube driver, the LC6554D/H can be also widely used in applications where no fluorescent display is provided.
The LC6554D/H are the same as our LC6500 series in the basic architecture of the CPU and the instruction set, but are made more powerful in the stack level and also made easier-to-use in the standby function.

Features

- Instruction set with 80 instructions (Common to the LC6500 series)
- On-chip 4096-byte ROM, 1024-bit RAM
- Instruction cycle time: 2.77 μs (D version, V_{DD} = 4 to 5.5V)
  0.92 μs (H version, V_{DD} = 4.5 to 5.5V)
- Serial input/output interface x 1 (4 bit/8 bit program-selectable)
- I/O ports: 57 pins in all
  - Input ports: 8 pins
  - Input/output common ports: 28 pins: 15V max., 15 mA max., LED drivable, pull-up resistance option available
  - Output ports: 21 pins: V_{DD}—45 V withstand voltage, FLT drivable, common with general-purpose output, pull-down resistance option available
  - Output level during reset: For ports C, D, output (H or L) during reset may be specified portwise by option.
- Interrupt function
  - Timer interrupt: 1
  - $\overline{INT}$ pin or serial I/O interrupt: 1
- Stack level: 8 levels (Common with interrupt)
- Timer: 4-bit prescaler + 8-bit programmable timer
- Burst pulse (64 x cycle time, dury 50%) output function
- Oscillator option
  Circuit mode: Ceramic resonator mode, RC mode, external clock mode (384 kHz to 4.33 MHz)
  Predivider option: 1/1, 1/3, 1/4
- Standby function: Standby function provided by the HALT instruction. Provides the function to absorb the OSC stabilizing time in the ceramic resonator mode.
- Supply Voltage: 4 to 5.5 V (D version)
  4.5 to 5.5 V (H version)
- Package: DIP64 shrink type, FLP64
- Evaluation LSI: LC6595 (Evaluation chip) + EVA-TB6520/22/54/43/46 (Target board), LC65PG54 (Piggyback)

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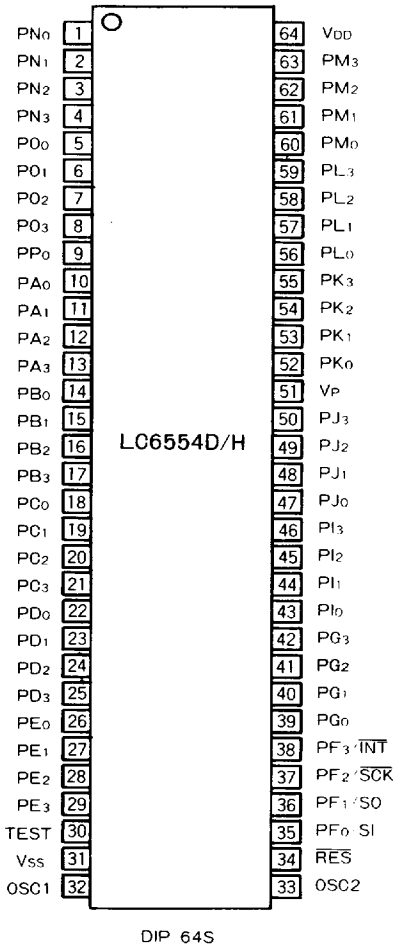
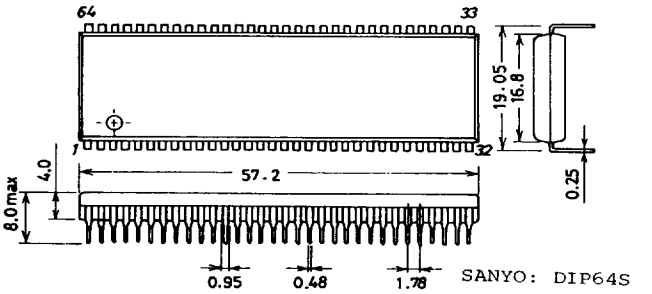
Pin Assignment

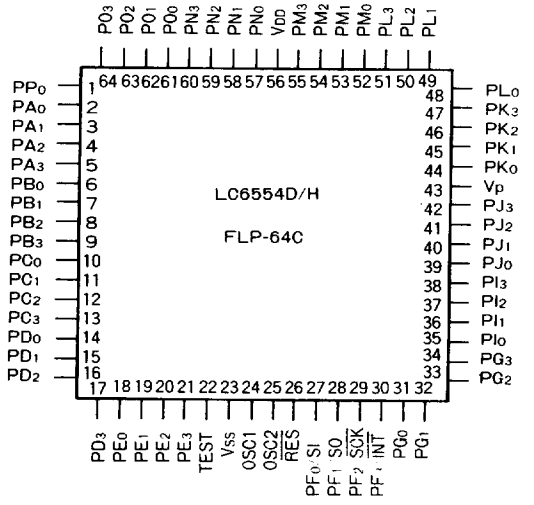


DIP 64S

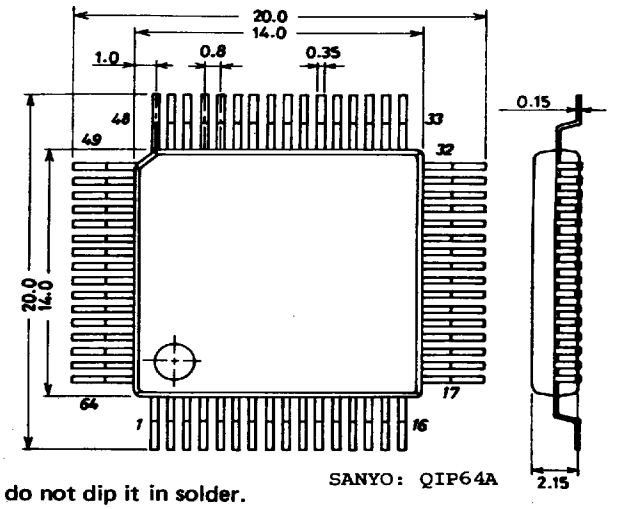
OSC1, OSC2 : C, R, or ceramic resonator oscillator for OSC
PA_{0-3} : Port for input only A_{0-3}
PB_{0-3} : Port for input only B_{0-3}
PC_{0-3} : Input/output common port C_{0-3}
PD_{0-3} : Input/output common port D_{0-3}
PE_{0-3} : Input/output common port E_{0-3}
PF_{0-3} : Input/output common port F_{0-3}
PG_{0-3} : Input/output common port G_{0-3}
PI_{0-3} : Input/output common port I_{0-3}
PJ_{0-3} : Input/output common port J_{0-3}
PK_{0-3} : Port for output only K_{0-3}
PL_{0-3} : Port for output only L_{0-3}
PM_{0-3} : Port for output only M_{0-3}
PN_{0-3} : Port for output only N_{0-3}
PO_{0-3} : Port for output only O_{0-3}
PP_0 : Port for output only P_0
} With high-voltage output driver
SI : 4-bit/8-bit serial input port
SO : 4-bit/8-bit serial output port
$\overline{SCK}$: Input/output for serial clock
$\overline{INT}$: Interrupt request input
Vp : Vp pin
$\overline{RES}$: Reset
TEST : Test

Case Outline 3071-D64IC
(unit: mm)



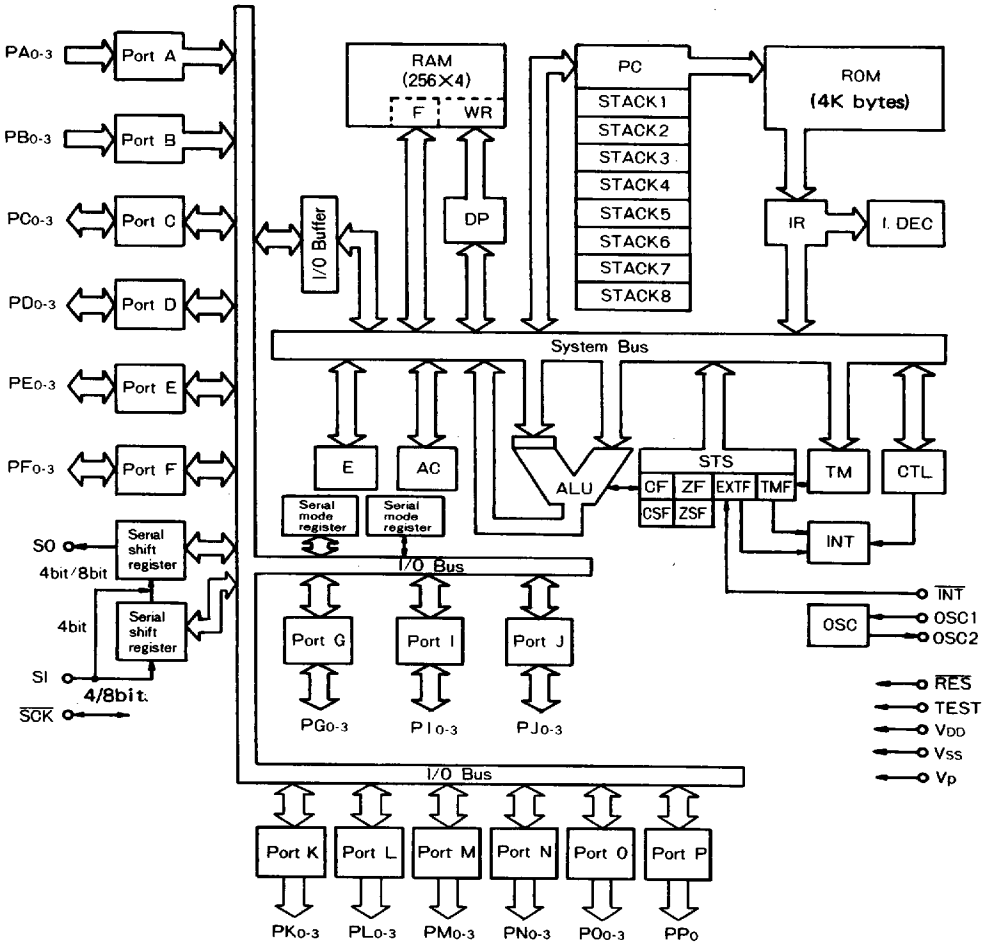


Case Outline 3057-Q64AIC
(unit: mm)



Note: When mounting the FLP version on the board, do not dip it in solder.

System Block Diagram



RAM	:	Data memory	STS	:	Status register
F	:	Flag	ROM	:	Program memory
WR	:	Working register	PC	:	Program counter
AC	:	Accumulator	INT	:	Interrupt control
ALU	:	Arithmetic and logic unit	IR	:	Instruction register
DP	:	Data pointer	I. DEC	:	Instruction decoder
E	:	E register	CF, CSF	:	Carry flag, carry save flag
CTL	:	Control register	ZF, ZSF	:	Zero flag, zero save flag
OSC	:	Oscillator	EXTF	:	External interrupt request
TM	:	Timer	TMF	:	Internal interrupt request

(Note) SI, SO, $\overline{SCK}$, $\overline{INT}$: Common to PF_0 to PF_3

Pin Description

Pin Name	Pins	I/O	Functions	Options	During Reset
V_{DD} V_{SS}	1 1	—	Power supply	—	—
OSC1	1	Input	●Pin for externally connecting R,C or a ceramic resonator for system clock generation ●For the external clock mode, the OSC2 pin is open.	(1) External clock input (2) 2-pin RC OSC (3) 2-pin ceramic resonator OSC (4) Predivider option 1. No predivider 2. 1/3 predivider 3. 1/4 predivider	—
OSC2	1	Output			
PA_0 PA_1 PA_2 PA_3	4	Input	● Input port A_0 to 3 (Low-threshold input) 4-bit input (IP instruction) Single-bit decision (BP, BNP instructions)	—	—
PB_0 PB_1 PB_2 PB_3	4	Input	● Input port B_0 to 3 (Low-threshold input) 4-bit input (IP instruction) Single-bit decision (BP, BNP instructions) ●Standby is controlled by the PB_3. ●The PB_3 pin must be free from chattering during the HALT instruction execution cycle.	—	—
PC_0 PC_1 PC_2 PC_3	4	Input/output	● Input/output common port C_0 to 3. 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit decision (BP, BNP instructions) Single-bit set/reset (SPB, RPB instructions) ●Output ("H" or "L") during reset may be specified by option.	(1) Open drain type output (2) With pull-up resistance (3) Output during reset: "H" (4) Output during reset: "L" ● (1), (2): Specified bit by bit. ● (3), (4): Specified in a group of 4 bits.	●"H" output ●"L" output (Option-selectable)
PD_0 PD_1 PD_2 PD_3	4	Input/output	● Input/output common port D_0 to 3. The functions, options are the same as for the PC_0 to 3.	Same as for the PC_0 to 3.	Same as for the the PC_0 to 3.
PE_0 PE_1 PE_2 PE_3	4	Input/output	● Input/output common port E_0 to 3 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit decision (BP, BNP instructions) Single-bit set/reset (SPB, RPB instructions) ●PE_0: With burst pulse (64Tcyc) output function	(1) Open drain type output (2) With pull-up resistance (1), (2): Specified bit by bit.	●"H" output (Output Nch transistor OFF)

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Pin Name	Pins	I/O	Functions	Options	During Reset
PF_0/SI PF_1/SO PF_2/$\overline{SCK}$ PF_3/$\overline{INT}$	4	Input/output	●Input/output port F_0 to 3 The functions, options are the same as for the PE_0 to 3. However, no burst pulse output function is provided. ●PF_0 to 3: Also used for serial interface, $\overline{INT}$ input. Program-selectable. ●4-bits/8 bits of serial input/output: Program-selectable SI: Serial input port SO: Serial output port $\overline{SCK}$: Serial clock input/output $\overline{INT}$: Interrupt request input	Same as for the PE_0 to 3.	Same as for the PE_0 to 3. Serial port: Disable Interrupt source: $\overline{INT}$
PG_0 PG_1 PG_2 PG_3	4	Input/output	●Input/output common port G_0 to 3. The functions, options are the same as for the PE_0 to 3. However, no burst pulse output function is provided.	Same as for the PE_0 to 3.	Same as for the PE_0 to 3.
PI_0 PI_1 PI_2 PI_3	4	Input/output	●Input/output common port I_0 to 3 The functions, options are the same as for the PG_0 to 3.	Same as for the PG_0 to 3.	Same as for the PG_0 to 3.
PJ_0 PJ_1 PJ_2 PJ_3	4	Input/output	●Input/output common port J_0 to 3 The functions, options are the same as for the PG_0 to 3.	Same as for the PG_0 to 3.	Same as for the PG_0 to 3.
PK_0 PK_1 PK_2 PK_3	4	Output	●Output port K_0 to 3 (Segment driver output) 4-bit output (OP instruction) Single-bit decision (BP, BNP instructions) Single-bit set/reset (SPB, RPB instructions)	(1) Open drain type output (2) With pull-down resistance ● (1), (2): Specified bit by bit.	"L" output (Output Pch transistor OFF)
PL_0 PL_1 PL_2 PL_3	4	Output	●Output port L_0 to 3 (Segment driver output) The functions, options are the same as for the PK_0 to 3.	Same as for the PK_0 to 3.	Same as for the PK_0 to 3.
PM_0 PM_1 PM_2 PM_3	4	Output	●Output port M_0 to 3 (Digit driver output) The functions, options are the same as for the PK_0 to 3.	Same as for the PK_0 to 3.	Same as for the PK_0 to 3.
PN_0 PN_1 PN_2 PN_3	4	Output	●Output port N_0 to 3 (Digit driver output) The functions, options are the same as for the PK_0 to 3.	Same as for the PK_0 to 3.	Same as for the PK_0 to 3.

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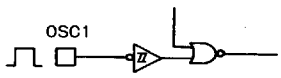
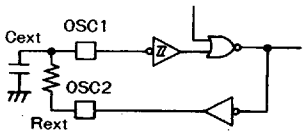
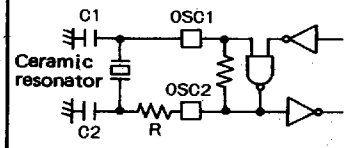
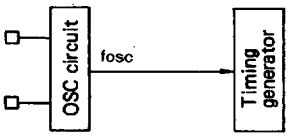
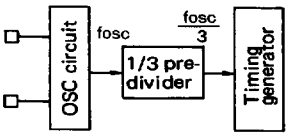
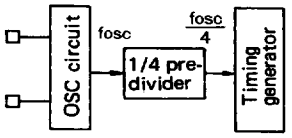
Pin Name	Pins	I/O	Functions	Options	During Reset
PO_0 PO_1 PO_2 PO_3	4	Output	●Output port O_0 to 3 (Digit driver output) The functions, options are the same as for the PK_0 to 3.	Same as for the PK_0 to 3.	Same as for the PK_0 to 3.
PP_0	1	Output	●Output port P_0 (Digit driver output) The functions, options are the same as for the PK_0 to 3. This port consists of a single bit.	Same as for the PK_0 to 3.	Same as for the PK_0 to 3.
$\overline{RES}$	1	Input	●System reset input ●For power-up reset, C is connected externally. ●For reset restart, "L" level is applied for 4 clock cycles or more.	—	—
TEST	1	Input	●LSI test pin Normally connected to V_{SS}	—	—
Vp	1	—	●Power supply pin for pull-down resistance	—	—

Oscillator Circuit Option

Option Name	Circuit	Conditions, etc.
1. External Clock		● Input: Schmitt type.
2. 2-pin RC OSC		● Input: Schmitt type.
3. Ceramic Resonator OSC		

Predivider Option

Option Name	Circuit	Conditions, etc.
1. No predivider		• Applicable to all of 3 OSC options. • The OSC frequency, external clock do not exceed 1444 kHz. (LC6554D) • The OSC frequency, external clock do not exceed 4330 kHz. (LC6554H) • Refer to Table of OSC, Predivider Option (Table 2).
2. 1/3 predivider		• Applicable to only 2 options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330 kHz. • Refer to Table of OSC, Predivider Option (Table 2).
3. 1/4 predivider		• Applicable to only 2 options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330 kHz. • Refer to Table of OSC, Predivider Option (Table 2).

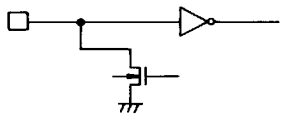
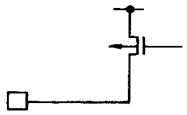
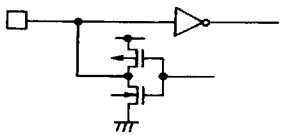
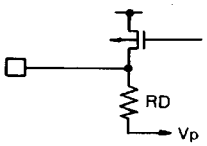
Options of Ports C, D Output Level during Reset

For input/output common ports C, D, either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions, etc.
1. Output during reset: "H" level	All of 4 bits of ports C, D
2. Output during reset: "L" level	All of 4 bits of ports C, D

Options of Port Output Configuration

For each input/output common port, either of the following two output configurations may be selected by option (bitwise).

Option Name	Circuit	Applicable Ports
1. Open drain type output		Ports C, D, E, F, G, I, J
		Ports K, L, M, N, O, P
2. Output with pull-up resistance		Ports C, D, E, F, G, I, J
3. Output with pull-down resistance		Ports K, L, M, N, O, P

LC6554D

1. Absolute Maximum Ratings/Ta=25°C, V_{SS}=0V

					unit
Maximum Supply Voltage	V_{DD} max		V_{DD}	−0.3 to +7.0	V
Output Voltage	$V_{O(1)}$		OSC2	Allowable up to voltage generated	V
	$V_{O(2)}$		Port K to P	V_{DD}−45 to V_{DD}+0.3	V
Input Voltage	$V_{I(1)}$		OSC1 (Note 1)	−0.3 to V_{DD}+0.3	V
	$V_{I(2)}$		TEST, $\overline{RES}$	−0.3 to V_{DD}+0.3	V
	$V_{I(3)}$		Port A, B	−0.3 to +15	V
	$V_{I(4)}$		Vp	V_{DD}−45 to V_{DD}+0.3	V
Input/Output Voltage	$V_{IO(1)}$		Port of OD type (Port C to J)	−0.3 to +15	V
	$V_{IO(2)}$		Port of PU type (Port C to J)	−0.3 to V_{DD}+0.3	V
Peak Output Current	$I_{OP(1)}$		Port C to J	−2 to +15	mA
	$I_{OP(2)}$		Port K, L	−10 to 0	mA
	$I_{OP(3)}$		Port M to P	−15 to 0	mA
Average Output Current	$I_{OA(1)}$	Per pin over the period of 100 msec.	Port C to J	−2 to +15	mA
	$I_{OA(2)}$	Per pin over the period of 100 msec.	Port K, L	−10 to 0	mA
	$I_{OA(3)}$	Per pin over the period of 100 msec.	Port M to P	−15 to 0	mA
	$\Sigma I_{OA(1)}$	Total current of all pins (Note 2)	Port C, D, E	−30 to +50	mA
	$\Sigma I_{OA(2)}$	Total current of all pins (Note 2)	Port F to J	−30 to +50	mA
	$\Sigma I_{OA(3)}$	Total current of all pins (Note 2)	Port K, L, M	−50 to 0	mA
	$\Sigma I_{OA(4)}$	Total current of all pins (Note 2)	Port N, O, P	−50 to 0	mA
Allowable Power Dissipation	Pd max(1)	Ta=−30 to +70°C(FLP)		430	mW
	Pd max(2)	Ta=−30 to +70°C(DIP)		600	mW
Operating Temperature	Topg			−30 to +70	°C
Storage Temperature	Tstg			−55 to +125	°C

2. Allowable Operating Conditions/Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=4.0 to 5.5V

				min	typ	max	unit
Operating Supply Voltage	V_{DD}		V_{DD}	4.0		5.5	V
Standby Supply Voltage	Vst	RAM, register hold(Note 3)	V_{DD}	1.8		5.5	V
"H"-Level Input Voltage	$V_{IH(1)}$		Port A, B_0 to 2	1.9		+13.5	V
	$V_{IH(2)}$	Output Nch Tr OFF	Port of OD type (Port C to J)	0.7V_{DD}		+13.5	V
	$V_{IH(3)}$	Output Nch Tr OFF	Port of PU type (Port C to J)	0.7V_{DD}		V_{DD}	V
	$V_{IH(4)}$	Output Nch Tr OFF	$\overline{INT}$, $\overline{SCK}$, SI of OD type	0.8V_{DD}		+13.5	V
	$V_{IH(5)}$	Output Nch Tr OFF	$\overline{INT}$, $\overline{SCK}$, SI of PU type	0.8V_{DD}		V_{DD}	V
	$V_{IH(6)}$		$\overline{RES}$	0.8V_{DD}		V_{DD}	V
	$V_{IH(7)}$	External clock mode	OSC1	0.8V_{DD}		V_{DD}	V
	$V_{IH(8)}$	Fig. 8	High Vt input circuit of Port B_3	V_{DD}−0.5		+13.5	V
	$V_{IH(9)}$	Fig. 8	Low Vt input circuit of Port B_3	0.5V_{DD}		+13.5	V

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LC6554D

				min	typ	max	unit
"L"-Level Input Voltage	$V_{IL(1)}$		Port A, B_0 to 2	V_{SS}		+0.5	V
	$V_{IL(2)}$		Port C to J	V_{SS}		$0.3V_{DD}$	V
	$V_{IL(3)}$		$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		$0.25V_{DD}$	V
	$V_{IL(4)}$		TEST	V_{SS}		$0.3V_{DD}$	V
	$V_{IL(5)}$		$\overline{RES}$	V_{SS}		$0.25V_{DD}$	V
	$V_{IL(6)}$	External clock mode	OSC1	V_{SS}		$0.25V_{DD}$	V
	$V_{IL(7)}$	Fig. 8	Low Vt input circuit of Port B_3	V_{SS}		+0.9	V
				See Table 2.			
Operating Frequency (Cycle Time)	fop			384		1444	kHz
	(T_{CYC})			(10.4)		(2.77)	(μs)

External Clock Conditions (When the external clock or 2-pin RC OSC option is selected)

Frequency	fext	Fig. 1	OSC1	See Table 2.			
Pulse Width	textH, textL	Fig. 1	OSC1	90			ns
Rise/Fall Time	textR, textF	Fig. 1	OSC1			30	ns
Oscillation Guaranteed Constants							
2-Pin RC Oscillation	Cext	Fig. 2	OSC1, OSC2	220±5%			pF
	Rext	Fig. 2	OSC1, OSC2	6.8±1%			kΩ
Ceramic Resonator Oscillation		Fig. 3		See Table 1.			

3. Electrical Characteristics/Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=4.0 to 5.5V

				min	typ	max	unit
"H"-Level Input Current	$I_{IH(1)}$	Output Nch Tr OFF (Including OFF leakage current of Nch Tr) V_{IN}=+13.5V	Port of OD type (Port C to J) Port A, B			+5.0	μA
	$I_{IH(2)}$	External clock mode, $V_{IN}=V_{DD}$	OSC1			+1.0	μA
"L"-Level Input Current	$I_{IL(1)}$	Output Nch Tr OFF $V_{IN}=V_{SS}$	Port of OD type (Port C to J) Port A, B	−1.0			μA
	$I_{IL(2)}$	Output Nch Tr OFF $V_{IN}=V_{SS}$	Port of PU type (Port C to J)	−1.3	−0.35		mA
	$I_{IL(3)}$	$V_{IN}=V_{SS}$	$\overline{RES}$	−45	−10		μA
	$I_{IL(4)}$	External clock mode, $V_{IN}=V_{SS}$	OSC1	−1.0			μA
"H"-Level Output Voltage	$V_{OH(1)}$	I_{OH}=−50μA	Port of PU type (Port C to J)	V_{DD}−1.2			V
	$V_{OH(2)}$	I_{OH}=−3mA	Port K, L	V_{DD}−1.8			V
	$V_{OH(3)}$	I_{OH}=−10mA	Port M to P	V_{DD}−1.8			V
"L"-Level Output Voltage	$V_{OL(1)}$	I_{OL}=10mA	Port C to J			1.5	V
	$V_{OL(2)}$	I_{OL}=2mA, When I_{OL} of each port is 2mA or less	Port C to J			0.5	V
	$V_{OL(3)}$	Output Pch Tr OFF Vp=−35V Output open	Port of PD type (Port K to P)			−33	V
Output OFF Leakage Current	$I_{OFF(1)}$	Output Pch Tr OFF $V_{OUT}=V_{DD}$	Port of OD type (Port K to P)			+30	μA
	$I_{OFF(2)}$	Output Pch Tr OFF $V_{OUT}=V_{DD}$−40V	Port of OD type (Port K to P)	−30			μA
Hysteresis Voltage	V_{HYS}		$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, SI, OSC1 of Schmitt type (Note 5)	$0.1V_{DD}$			V

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LC6554D

					min	typ	max	unt
Current Dissipation	Operation mode, Output Nch Tr, Pch Tr OFF, Port=V_{DD}							
2-Pin RC Oscillation Mode	$I_{DDOP(1)}$	Fig. 2	f_{OSC}=700kHZ(TYP)	V_{DD}		1.5	5	mA
Ceramic Resonator	$I_{DDOP(2)}$	Fig. 3	4MHz, 1/3 predivider	V_{DD}		5	10	mA
Oscillation Mode	$I_{DDOP(3)}$	Fig. 3	4MHz, 1/4 predivider	V_{DD}		5	10	mA
	$I_{DDOP(4)}$	Fig. 3	3MHz, 1/3 predivider	V_{DD}		4	9	mA
	$I_{DDOP(5)}$	Fig. 3	3MHz, 1/4 predivider	V_{DD}		4	9	mA
	$I_{DDOP(6)}$	Fig. 3	400KHz	V_{DD}		0.6	3	mA
	$I_{DDOP(7)}$	Fig. 3	800KHz	V_{DD}		1.2	4	mA
External Clock Mode	$I_{DDOP(8)}$		384kHz to 1444kHz, 1/1 predivider	V_{DD}		2	6	mA
			1152kHz to 4330kHz, 1/3 predivider 1536kHz to 4330kHz, 1/4 predivider	V_{DD}		5	10	mA
Standby Mode	I_{DDSt}		V_{DD}=5.5V Output Nch Tr OFF Output Pch Tr OFF Port=V_{DD}	V_{DD}		0.05	10	μA
Oscillation Characteristics								
Ceramic Resonator Oscillation								
Oscillation Frequency	f_{CFOSC} (Note 4)	Fig. 3	fo=400kHz	OSC1, OSC2	392	400	408	kHz
		Fig. 3	fo=800kHz	OSC1, OSC2	784	800	816	kHz
		Fig. 3	fo=3MHz, 1/3 predivider 1/4 predivider	OSC1, OSC2	2940	3000	3060	kHz
		Fig. 3	fo=4MHz, 1/3 predivider 1/4 predivider	OSC1, OSC2	3920	4000	4080	kHz
Oscillation Stabilizing Period	t_{CFS}	Fig. 4	fo=400kHz, 800kHz, 3MHz, 4MHz				10	ms
2-Pin RC Oscillation								
Oscillation Frequency	f_{MOSC}	Fig. 2	Cext=220pF ±5% Rext=6.8kΩ ±1%	OSC1, OSC2	486	700	1056	kHz
Pull-up Resistance								
I/O Port Pull-up Resistance	Rpp		V_{DD}=5V	Port of PU type (Port C to J)		14		kΩ
Pull-down Resistance								
Output Port Pull-down Resistance	Rpd		V_{DD}=5V	Port of PD type (Port K to P)	50		200	kΩ
External Reset Characteristics								
Reset Time	T_{RST}					See Fig. 5.		

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LC6554D

				min	typ	max	unit
Pin Capacitance	CP	f=1MHz Other than pins to be tested, $V_{IN}=V_{SS}$			10		pF
Serial Clock							
Input Clock Cycle Time	$t_{CKCY(1)}$	Fig. 6	$\overline{SCK}$	3.0			μs
Output Clock Cycle Time	$t_{CKCY(2)}$	Fig. 6	$\overline{SCK}$		64 x T_{CYC} (T_{CYC}=4 x System clock period)		μs
Input Clock "L"-Level Pulse Width	$t_{CKL(1)}$	Fig. 6	$\overline{SCK}$	1.0			μs
Output Clock "L"-Level Pulse Width	$t_{CKL(2)}$	Fig. 6	$\overline{SCK}$		32 x T_{CYC}		μs
Input Clock "H"-Level Pulse Width	$t_{CKH(1)}$	Fig. 6	$\overline{SCK}$	1.0			μs
Output Clock "H"-Level Pulse Width	$t_{CKH(2)}$	Fig. 6	$\overline{SCK}$		32 x T_{CYC}		μs
Serial Input							
Data Setup Time	t_{ICK}	Specified for ↑ of $\overline{SCK}$, Fig. 6	SI	0.5			μs
Data Hold Time	t_{CKI}		SI	0.5			μs
Serial Output							
Output Delay Time	t_{CKO}	Specified for ↓ of $\overline{SCK}$, Nch OD only: External 1kohm, external 50pF Fig. 6	SO			0.5	μs
Pulse Output							
Period	t_{PCY}	Fig. 7	PE_0		64xT_{CYC}		μs
"H"-Level Pulse Width	t_{PH}	T_{CYC}=4 x System clock	PE_0		32xT_{CYC} ±10%		μs
"L"-Level Pulse Width	t_{PL}	period, Nch OD only: External 1kohm, external 50pF	PE_0		32xT_{CYC} ±10%		μs

Note 1: When oscillated internally under the oscillating conditions in Fig. 3, up to the oscillation amplitude generated is allowable.

Note 2: Average over the period of 10 msec.

Note 3: Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction.
The PB_3 pin must be free from chattering during the HALT instruction execution cycle.

Note 4: f_{CFOSC} represents an oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

Note 5: The OSC1 becomes the Schmitt type when the OSC option is the 2-pin RC OSC or external clock OSC.

Note 6: When mounting the FLP version on the board, do not dip it in solder.

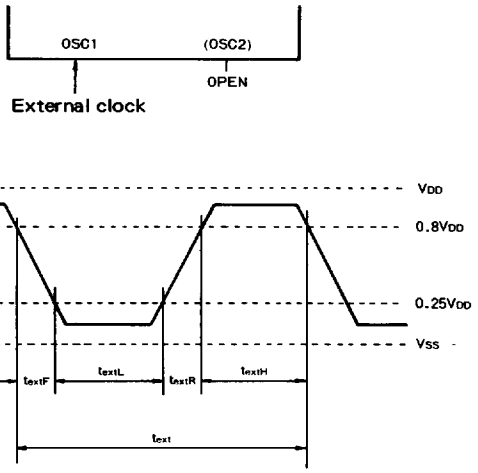


Fig. 1 External Clock Input Waveform

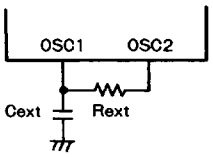


Fig. 2 2-Pin RC Oscillation Circuit

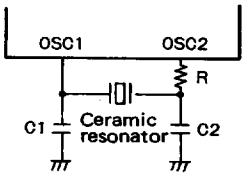


Fig. 3 Ceramic Resonator Oscillation Circuit

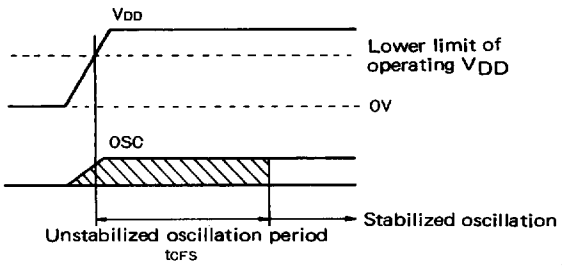


Fig. 4 Oscillation Stabilizing Period

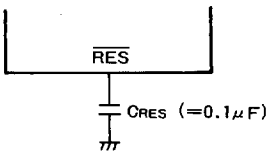


Fig. 5 Reset Circuit

Note 7: When the rise time of the power supply is 0, the reset time becomes 10 ms to 100 ms at C_{RES}=0.1 μF. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10 ms or greater.

4MHz CSA4.00MG (Murata)	C 1	33pF±10%
	C 2	33pF±10%
	R	0 Ω
4MHz KBR4.0MS (Kyocera)	C 1	33pF±10%
	C 2	33pF±10%
	R	0 Ω
3MHz CSA3.00MG (Murata)	C 1	33pF±10%
	C 2	33pF±10%
	R	0 Ω
3MHz KBR3.0MS (Kyocera)	C 1	47pF±10%
	C 2	47pF±10%
	R	0 Ω

800KHz CSB800D CSB800K (Murata)	C 1	220pF±10%
	C 2	220pF±10%
	R	0 Ω
800KHz KBR800H (Kyocera)	C 1	220pF±10%
	C 2	220pF±10%
	R	0 Ω
400KHz CSB400P (Murata)	C 1	330pF±10%
	C 2	330pF±10%
	R	0 Ω
400KHz KBR400B (Kyocera)	C 1	330pF±10%
	C 2	330pF±10%
	R	0 Ω

Table 1 Constants Guaranteed for Ceramic Resonator Oscillation

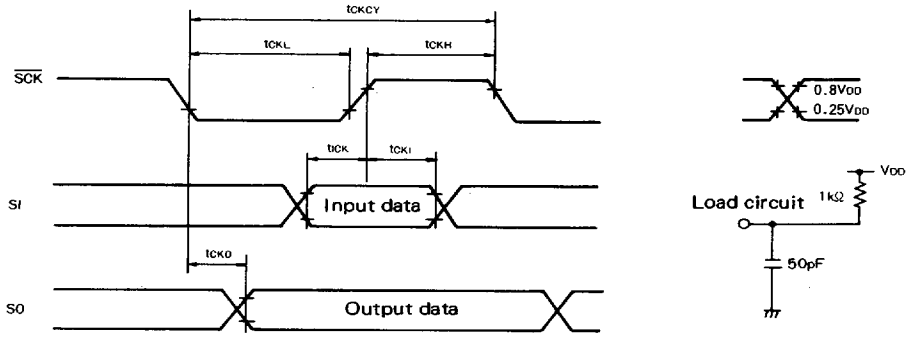
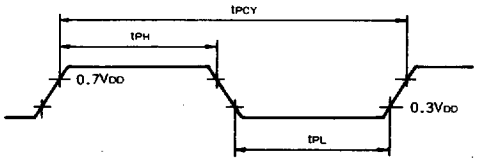


Fig. 6 Serial Input/Output Timing



The load conditions are the same as in Fig. 6.

Fig. 7 Pulse Output Timing at Port PE_0

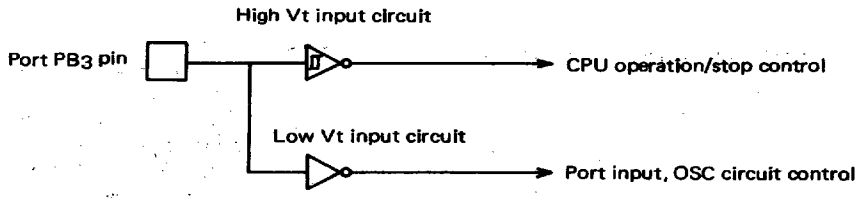


Fig. 8 Port PB_3 High Vt/Low Vt Input Circuit

Table 2 LC6554D

Table of Oscillation, Predivider Option (All selectable combinations are shown. Do not use any other combinations than shown below.) V_{DD}=4 to 5.5V

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	Remarks
Ceramic Resonator Option	400 kHz	1/1 (10 μs)	Unusable with 1/3, 1/4 predivider
	800 kHz	1/1 (5 μs)	Unusable with 1/3, 1/4 predivider
	3 MHz	1/3 (4 μs) 1/4 (5.33 μs)	Unusable with 1/1 predivider
	4 MHz	1/3 (3 μs) 1/4 (4 μs)	Unusable with 1/1 predivider
External Clock Option or External Clock Drive by RC OSC Option	384 to 1444 kHz 1152 to 4330 kHz 1536 to 4330 kHz	1/1 (10.4 to 2.77 μs) 1/3 (10.4 to 2.77 μs) 1/4 (10.4 to 3.70 μs)	
External Clock Drive by Ceramic Resonator OSC Option	The external clock drive is impossible. When using the external clock drive, specify the external clock option or RC OSC option.		
RC OSC Option	Used with 1/1 predivider, recommended constants. If used with other than recommended constants, the predivider option, frequency, V_{DD} range must be the same as for the external clock option.		

RC Oscillation Characteristic of the LC6554D

Fig. 8 shows the RC oscillation characteristic of the LC6554D. For the variation range of RC OSC frequency of the LC6554D, the following are guaranteed at the external constants only shown below.

External constants Cext=220 pF, Rext=6.8 kohms

486 kHz ≦ f_{MOSC} ≦ 1056 kHz (Ta=−30°C to +70°C, V_{DD}=4.0 to 5.5 V)

If any other constants than specified above are used, the range of Rext = 4 kohms to 20 kohms, Cext = 150 pF to 390 pF must be observed. (See Fig. 8.)

Note 8: The oscillation frequency at V_{DD}=5.0 V, Ta=25°C must not exceed 700 kHz.

Note 9: The oscillation frequency at V_{DD}=4 to 5.5 V, Ta=−30 to +70°C must be within the operation clock frequency range (384 kHz to 1444 kHz).

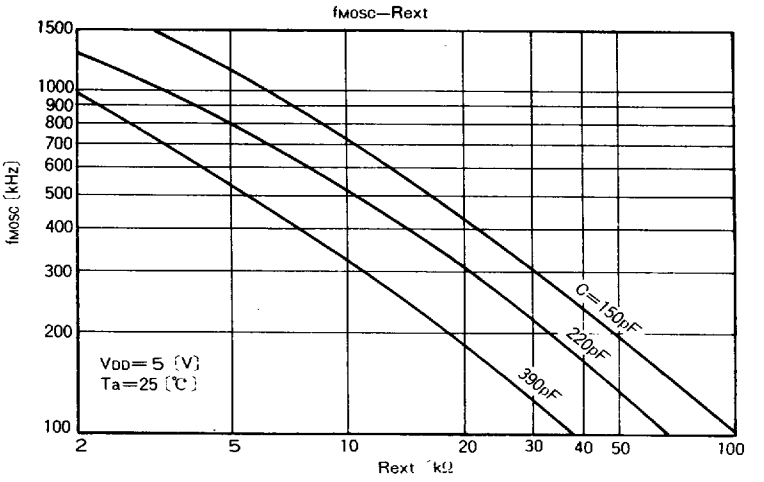


Fig. 8 RC Oscillation Frequency Data (Typ.)

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1. Absolute Maximum Ratings/Ta=25°C, V_{SS}=0V

					unit
Maximum Supply Voltage	V_{DD} max		V_{DD}	−0.3 to +7.0	V
Output Voltage	$V_{O(1)}$		OSC2	Allowable up to voltage generated	V
	$V_{O(2)}$		Port K to P	V_{DD}−45 to V_{DD}+0.3	V
Input Voltage	$V_{I(1)}$		OSC1 (Note 1)	−0.3 to V_{DD}+0.3	V
	$V_{I(2)}$		TEST, $\overline{RES}$	−0.3 to V_{DD}+0.3	V
	$V_{I(3)}$		Port A, B	−0.3 to +15	V
	$V_{I(4)}$		Vp	V_{DD}−45 to V_{DD}+0.3	V
Input/Output Voltage	$V_{IO(1)}$		Port of OD type (Port C to J)	−0.3 to +15	V
	$V_{IO(2)}$		Port of PU type (Port C to J)	−0.3 to V_{DD}+0.3	V
Peak Output Current	$I_{OP(1)}$		Port C to J	−2 to +15	mA
	$I_{OP(2)}$		Port K, L	−10 to 0	mA
	$I_{OP(3)}$		Port M to P	−15 to 0	mA
Average Output Current	$I_{OA(1)}$	Per pin over the period of 100 msec.	Port C to J	−2 to +15	mA
	$I_{OA(2)}$	Per pin over the period of 100 msec.	Port K, L	−10 to 0	mA
	$I_{OA(3)}$	Per pin over the period of 100 msec.	Port M to P	−15 to 0	mA
	$\Sigma I_{OA(1)}$	Total current of all pins (Note 2)	Port C, D, E	−30 to +50	mA
	$\Sigma I_{OA(2)}$	Total current of all pins (Note 2)	Port F to J	−30 to +50	mA
	$\Sigma I_{OA(3)}$	Total current of all pins (Note 2)	Port K, L, M	−50 to 0	mA
	$\Sigma I_{OA(4)}$	Total current of all pins (Note 2)	Port N, O, P	−50 to 0	mA
Allowable Power Dissipation	Pd max(1)	Ta=−30 to +70°C(FLP)		430	mW
	Pd max(2)	Ta=−30 to +70°C(DIP)		600	mW
Operating Temperature	Topg			−30 to +70	°C
Storage Temperature	Tstg			−55 to +125	°C

2. Allowable Operating Conditions/Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=4.5 to 5.5V

				min	typ	max	unit
Operating Supply Voltage	V_{DD}		V_{DD}	4.5		5.5	V
Standby Supply Voltage	Vst	RAM, register hold(Note 3)	V_{DD}	1.8		5.5	V
"H"-Level Input Voltage	$V_{IH(1)}$		Port A, B_0 to 2	1.9		+13.5	V
	$V_{IH(2)}$	Output Nch Tr OFF	Port of OD type (Port C to J)	0.7V_{DD}		+13.5	V
	$V_{IH(3)}$	Output Nch Tr OFF	Port of PU type (Port C to J)	0.7V_{DD}		V_{DD}	V
	$V_{IH(4)}$	Output Nch Tr OFF	$\overline{INT}$, $\overline{SCK}$, SI of OD type	0.8V_{DD}		+13.5	V
	$V_{IH(5)}$	Output Nch Tr OFF	$\overline{INT}$, $\overline{SCK}$, SI of PU type	0.8V_{DD}		V_{DD}	V
	$V_{IH(6)}$		$\overline{RES}$	0.8V_{DD}		V_{DD}	V
	$V_{IH(7)}$	External clock mode	OSC1	0.8V_{DD}		V_{DD}	V
	$V_{IH(8)}$	Fig. 7	High Vt input circuit of Port B_3	V_{DD}−0.5		+13.5	V
	$V_{IH(9)}$	Fig. 7	Low Vt input circuit of Port B_3	0.5V_{DD}		+13.5	V

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				min	typ	max	unit
"L"-Level Input Voltage	$V_{IL(1)}$		Port A, B_0 to 2	V_{SS}		+0.5	V
	$V_{IL(2)}$		Port C to J	V_{SS}		$0.3V_{DD}$	V
	$V_{IL(3)}$		$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		$0.25V_{DD}$	V
	$V_{IL(4)}$		TEST	V_{SS}		$0.3V_{DD}$	V
	$V_{IL(5)}$		$\overline{RES}$	V_{SS}		$0.25V_{DD}$	V
	$V_{IL(6)}$	External clock mode	OSC1	V_{SS}		$0.25V_{DD}$	V
	$V_{IL(7)}$	Fig. 7	Low Vt input circuit of Port B_3	V_{SS}		+0.9	V
				See Table 2.			
Operating Frequency (Cycle Time)	fop (T_{CYC})			384 (10.4)		4330 (0.92)	kHz (μs)
External Clock Conditions (When the external clock option is selected)							
Frequency	fext	Fig. 1	OSC1	See Table 2.			
Pulse Width	textH, textL	Fig. 1	OSC1	90			ns
Rise/Fall Time	textR, textF	Fig. 1	OSC1			30	ns
Oscillation Guaranteed Constants							
Ceramic Resonator Oscillation		Fig. 2		See Table 1.			

3. Electrical Characteristics/Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=4.5 to 5.5V				min	typ	max	unit
"H"-Level Input Current	$I_{IH(1)}$	Output Nch Tr OFF (Including OFF leakage current of Nch Tr) V_{IN}=+13.5V	Port of OD type (Port C to J) Port A, B			+5.0	μA
	$I_{IH(2)}$	External clock mode, $V_{IN}=V_{DD}$	OSC1			+1.0	μA
"L"-Level Input Current	$I_{IL(1)}$	Output Nch Tr OFF $V_{IN}=V_{SS}$	Port of OD type (Port C to J) Port A, B	−1.0			μA
	$I_{IL(2)}$	Output Nch Tr OFF $V_{IN}=V_{SS}$	Port of PU type (Port C to J)	−1.3	−0.35		mA
	$I_{IL(3)}$	$V_{IN}=V_{SS}$	$\overline{RES}$	−45	−10		μA
	$I_{IL(4)}$	External clock mode, $V_{IN}=V_{SS}$	OSC1	−1.0			μA
"H"-Level Output Voltage	$V_{OH(1)}$	I_{OH}=−50μA	Port of PU type (Port C to J)	V_{DD}−1.2			V
	$V_{OH(2)}$	I_{OH}=−3mA	Port K, L	V_{DD}−1.8			V
	$V_{OH(3)}$	I_{OH}=−10mA	Port M to P	V_{DD}−1.8			V
"L"-Level Output Voltage	$V_{OL(1)}$	I_{OL}=10mA	Port C to J			1.5	V
	$V_{OL(2)}$	I_{OL}=2mA, When I_{OL} of each port is 2mA or less	Port C to J			0.5	V
	$V_{OL(3)}$	Output Pch Tr OFF Vp=−35V Output open	Port of PD type (Port K to P)			−33	V
Output OFF Leakage Current	$I_{OFF(1)}$	Output Pch Tr OFF $V_{OUT}=V_{DD}$	Port of OD type (Port K to P)			+30	μA
	$I_{OFF(2)}$	Output Pch Tr OFF $V_{OUT}=V_{DD}$−40V	Port of OD type (Port K to P)	−30			μA
Hysteresis Voltage	V_{HYS}		$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, SI, OSC1 of Schmitt type (Note 5)		$0.1V_{DD}$		V

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				min	typ	max	unit
Current Dissipation							
Ceramic Resonator Oscillaton Mode	$I_{DDOP(1)}$	Fig. 2 4MHz	V_{DD} Operating mode, Output Nch Tr, Pch Tr OFF, Port = V_{DD}		5	10	mA
External Clock Mode	$I_{DDOP(2)}$	384 kHz to 4330 kHz	V_{DD}		5	10	mA
Standby Mode	I_{DDST}	Output Nch Tr OFF Output Pch Tr OFF Port V_{DD}, V_{DD}=5.5 V	V_{DD}		0.05	10	μA
Oscillation Characteristics							
Ceramic Resonator Oscillation							
Oscillation Frequency	f_{CFOSC} (Note 4)	Fig. 2 f_O=4 MHz	OSC1, OSC2	3920	4000	4080	kHz
Oscillation Stabilizing Period	t_{CFS}	Fig. 3 f_O=4MHz				10	ms
Pull-up Resistance							
I/O Port Pull-up Resistance	Rpp	V_{DD}=5V	Port of PU type (Port C to J)		14		kΩ
Pull-down Resistance							
Output Port Pull-down Resistance	Rpd	V_{DD}=5V	Port of PD type (Port K to P)	50		200	kΩ
External Reset Characteristics							
Reset Time	T_{RST}				See Fig. 4.		

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LC6554H

				min	typ	max	unit
Pin Capacitance	CP	f=1MHz Other than pins to be tested, $V_{IN}=V_{SS}$			10		pF
Serial Clock							
Input Clock Cycle Time	$t_{CKCY(1)}$	Fig. 5	$\overline{SCK}$	3.0			μs
Output Clock Cycle Time	$t_{CKCY(2)}$	Fig. 5	$\overline{SCK}$		64 x T_{CYC} (T_{CYC}=4 x System clock period)		μs
Input Clock "L"-Level Pulse Width	$t_{CKL(1)}$	Fig. 5	$\overline{SCK}$	1.0			μs
Output Clock "L"-Level Pulse Width	$t_{CKL(2)}$	Fig. 5	$\overline{SCK}$		32 x T_{CYC}		μs
Input Clock "H"-Level Pulse Width	$t_{CKH(1)}$	Fig. 5	$\overline{SCK}$	1.0			μs
Output Clock "H"-Level Pulse Width	$t_{CKH(2)}$	Fig. 5	$\overline{SCK}$		32 x T_{CYC}		μs
Serial Input							
Data Setup Time	t_{ICK}	Specified for ↑ of $\overline{SCK}$, Fig. 5	SI	0.5			μs
Data Hold Time	t_{CKI}		SI	0.5			μs
Serial Output							
Output Delay Time	t_{CKO}	Specified for ↓ of $\overline{SCK}$, Nch OD only: External 1kohm, external 50pF Fig. 5	SO			0.5	μs
Pulse Output							
Period	t_{PCY}	Fig. 6	PE_0		64xT_{CYC}		μs
"H"-Level Pulse Width	t_{PH}	T_{CYC}=4 x System clock	PE_0		32xT_{CYC} ±10%		μs
"L"-Level Pulse Width	t_{PL}	period, Nch OD only: External 1kohm, external 50pF	PE_0		32xT_{CYC} ±10%		μs

Note 1: When oscillated internally under the oscillating conditions in Fig. 2, up to the oscillation amplitude generated is allowable.

Note 2: Average over the period of 10 msec.

Note 3: Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction.
The PB_3 pin must be free from chattering during the HALT instruction execution cycle.

Note 4: f_{CFOSC} represents an oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

Note 5: The OSC1 becomes the Schmitt type when the OSC option is the external clock OSC.

Note 6: When mounting the FLP version on the board, do not dip it in solder.

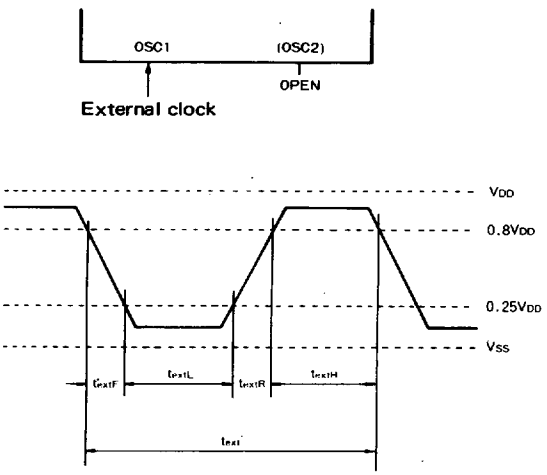


Fig. 1 External Clock Input Waveform

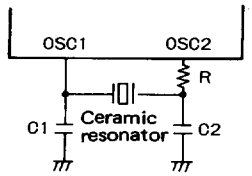


Fig. 2 Ceramic Resonator Oscillation Circuit

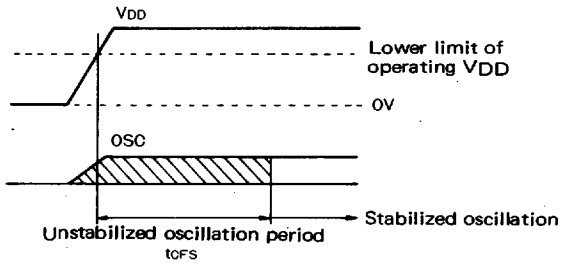


Fig. 3 Oscillation Stabilizing Period

4MHz CSA4.00MG (Murata)	C 1	33pF±10%
	C 2	33pF±10%
	R	0Ω
4MHz KBR4.0MS (Kyosera)	C 1	33pF±10%
	C 2	33pF±10%
	R	0Ω

Table 1 Constants Guaranteed for Ceramic Resonator Oscillation

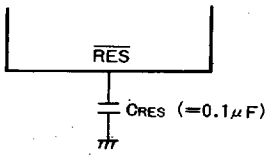


Fig. 4 Reset Circuit

Note 7: When the rise time of the power supply is 0, the reset time becomes 10 ms to 100ms at C_{RES}=0.1μF. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or greater.

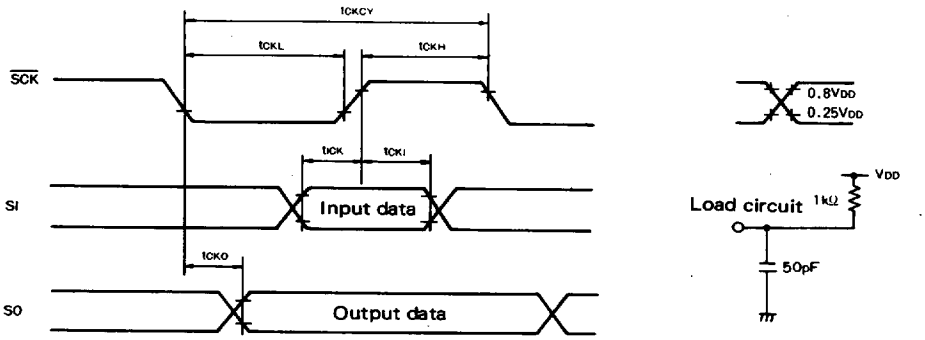
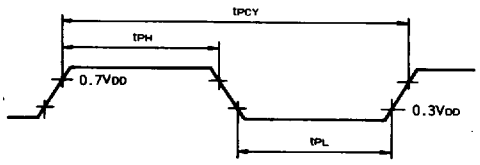


Fig. 5 Serial Input/Output Timing



The load conditions are the same as in Fig. 5.

Fig. 6 Pulse Output Timing at Port PE_0

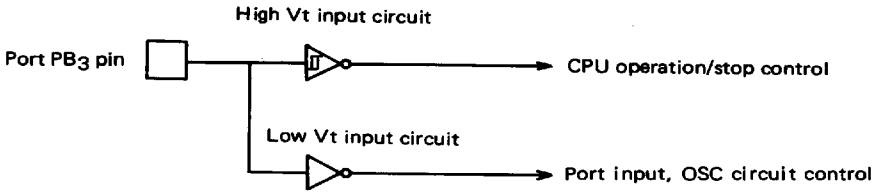


Fig. 7 Port PB_3 High Vt/Low Vt Input Circuit

Table 2 LC6554H

Table of Oscillation, Predivider Option (All selectable combinations are shown. Do not use any other combinations than shown below.) V_{DD}=4.5 to 5.5V

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	Remarks
Ceramic Resonator OSC Option	4 MHz	1/1 (1 μs)	
External Clock Option	384 to 4330 kHz	1/1 (10.4 to 0.92 μs)	
External Clock Drive by Ceramic Resonator OSC Option	The external clock drive is impossible. When using the external clock drive, specify the external clock option.		

LC6554D/H INSTRUCTION SET

Symbol	Description				
AC	: Accumulator	M(DP)	: Memory addressed by DP	( ), [ ]	: Contents
ACt	: Accumulator bit t	$P(DP_L)$	: Input/output port addressed by DP_L	←	: Transfer and direction
CF	: Carry flag	PC	: Program counter	+	: Addition
CTL	: Control register	STACK	: Stack register	−	: Subtraction
DP	: Data pointer	TM	: Timer	∧	: AND
E	: E register	TMF	: Timer (internal) interrupt request flag	∨	: OR
EXTF	: External interrupt request flag	At, Ha, La	: Working register	∀	: Exclusive OR
Fn	: Flag bit n	ZF	: Zero flag		
M	: Memory				

Instruction group	Mnemonic		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	The AC contents are cleared.	ZF	* 1
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	The CF contents are cleared.	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	The CF is set.	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← $\overline{(AC)}$	The AC contents are complemented.	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	The AC contents are incremented +1.	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) − 1	The AC contents are decremented −1.	ZF CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC_0 ← (CF), AC_{n+1} ← (AC_n), CF ← (AC_3)	The AC contents are shifted left through the CF.	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)	The AC contents are transferred to the E.		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ⇆ (E)	The AC contents and the E conents are exchanged.		
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← [M(DP)] + 1	The M(DP) contents are incremented +1.	ZF CF	
	DEM	Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← [M(DP)] − 1	The M(DP) contents are decremented −1.	ZF CF	
	SMB bit	Set M data bit	0 0 0 0	1 0 B_1B_0	1	1	M(DP. B_1B_0) ← 1	A single bit of the M(DP) specified with B_1B_0 is set.		
	RMB bit	Reset M data bit	0 0 1 0	1 0 B_1B_0	1	1	M(DP. B_1B_0) ← 0	A single bit of the M(DP) specified with B_1B_0 is reset.	ZF	
Arithmetic operation/comparion instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + [M(DP)]	Binary addition of the AC contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF	
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + [M(DP)] + (CF)	Binary addition of the AC, CF contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	6 is added to the AC contents.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	10 is added to the AC contents.	ZF	
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) ∀ [M(DP)]	The AC contents and the M(DP) contents are exclusive-ORed and the result is stored in the AC.	ZF	
	AND	And M to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ∧ [M(DP)]	The AC contents and the M(DP) contents are ANDed and the result is stored in the AC.	ZF	
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ [M(DP)]	The AC contents and the M(DP) contents are ORed and the result is stored in the AC.	ZF	
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	$\overline{[M(DP)]}$ + (AC) + 1	The AC contents and the M(DP) contents are compared and the CF and ZF are set/reset. (Comparison result: [M(DP)] > (AC): CF 0, ZF 0; [M(DP)] = (AC): CF 1, ZF 1; [M(DP)] < (AC): CF 1, ZF 0)	ZF CF	
	CI data	Compare AC with immediate data	0 0 1 0 / 0 1 0 0	1 1 0 0 / $I_3I_2I_1I_0$	2	2	$\overline{I_3I_2I_1I_0}$ + (AC) + 1	The AC contents and the immediate data $I_3I_2I_1I_0$ are compared and the ZF and CF are set/reset. (Comparison result: $I_3I_2I_1I_0$ > (AC): CF 0, ZF 0; $I_3I_2I_1I_0$ = (AC): CF 1, ZF 1; $I_3I_2I_1I_0$ < (AC): CF 1, ZF 0)	ZF CF	
	CLI data	Compare DP_L with immediate data	0 0 1 0 / 0 1 0 1	1 1 0 0 / $I_3I_2I_1I_0$	2	2	(DP_L) ∀ $I_3I_2I_1I_0$	The DP_L contents and the immediate data $I_3I_2I_1I_0$ are compared.	ZF	
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	$I_3I_2I_1I_0$	1	1	AC ← $I_3I_2I_1I_0$	The immediate data $I_3I_2I_1I_0$ is loaded in the AC.	ZF	* 1
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)	The AC contents are stored in the M(DP).		
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← [M(DP)]	The M(DP) contents are loaded in the AC.	ZF	
	XM data	Exchange AC with M, then modify DP_H with immediate data	1 0 1 0	0 $M_2M_1M_0$	1	2	(AC) ⇆ [M(DP)], DP_H ← (DP_H) ∀ 0 $M_2M_1M_0$	The AC contents and the M(DP) contents are exchanged and then the DP_H contents are modified with the contents of (DP_H) ∀ 0 $M_2M_1M_0$.	ZF	The ZF is set/reset according to the result of (DP_H) ∀ 0 $M_2M_1M_0$.
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	(AC) ⇆ [M(DP)]	The AC contents and the M(DP) contents are exchanged.	ZF	The ZF is set/reset according to the DP_H contents at the time of instruction execution.
	XI	Exchange AC with M, then increment DP_L	1 1 1 1	1 1 1 0	1	2	(AC) ⇆ [M(DP)], DP_L ← (DP_L) + 1	The AC contents and the M(DP) contents are exchanged and then the DP_L contents are incremented +1.	ZF	The ZF is set/reset according to the result of (DP_L +1).
	XD	Exchange AC with M, then decrement DP_L	1 1 1 1	1 1 1 1	1	2	(AC) ⇆ [M(DP)], DP_L ← (DP_L) − 1	The AC contents and the M(DP) contents are exchanged and then the DP_L contents are decremented −1.	ZF	The ZF is set/reset according to the result of (DP_L −1).
	RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC, E ← ROM (PCh, E, AC)	The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E.		

Instruction group	Mnemonic		Instruction code $D_7 D_6 D_5 D_4$	Instruction code $D_3 D_2 D_1 D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Data pointer manipulation instructions	LDZ data	Load DP_H with Zero and DP_L with immediate data respectively	1 0 0 0	$I_3 I_2 I_1 I_0$	1	1	$DP_H \leftarrow 0$ $DP_L \leftarrow I_3 I_2 I_1 I_0$	The DP_H and DP_L are loaded with 0 and the immediate data $I_3 I_2 I_1 I_0$ respectively.		
	LHI data	Load DP_H with immediate data	0 1 0 0	$I_3 I_2 I_1 I_0$	1	1	$DP_H \leftarrow I_3 I_2 I_1 I_0$	The DP_H is loaded with the immediate data $I_3 I_2 I_1 I_0$.		
	IND	Increment DP_L	1 1 1 0	1 1 1 0	1	1	$DP_L \leftarrow (DP_L)+1$	The DP_L contents are incremented +1.	ZF	
	DED	Decrement DP_L	1 1 1 0	1 1 1 1	1	1	$DP_L \leftarrow (DP_L)-1$	The DP_L contents are decremented −1.	ZF	
	TAL	Transfer AC to DP_L	1 1 1 1	0 1 1 1	1	1	$DP_L \leftarrow (AC)$	The AC contents are transferred to the DP_L.		
	TLA	Transfer DP_L to AC	1 1 1 0	1 0 0 1	1	1	$AC \leftarrow (DP_L)$	The DP_L contents are transferred to the AC.	ZF	
	XAH	Exchange AC with DP_H	0 0 1 0	0 0 1 1	1	1	$(AC) \rightleftarrows (DP_H)$	The AC contents and the DP_H contents are exchanged.		
Working register manipulation instructions	XAt	Exchange AC with working register At		$t_1 t_0$				The AC contents and the contents of working register At are exchanged. At is assigned one of A_0, A_1, A_2, A_3 according to $t_1 t_0$.		
	XA0		1 1 1 0	0 0 0 0	1	1	$(AC) \rightleftarrows (A0)$			
	XA1		1 1 1 0	0 1 0 0	1	1	$(AC) \rightleftarrows (A1)$			
	XA2		1 1 1 0	1 0 0 0	1	1	$(AC) \rightleftarrows (A2)$			
	XA3		1 1 1 0	1 1 0 0	1	1	$(AC) \rightleftarrows (A3)$			
	XHa	Exchange DP_H with working register Ha		a				The DP_H contents and the contents of working register Ha are exchanged. Ha is assigned either of H0 or H1 according to a.		
	XH0		1 1 1 1	1 0 0 0	1	1	$(DP_H) \rightleftarrows (H0)$			
	XH1		1 1 1 1	1 1 0 0	1	1	$(DP_H) \rightleftarrows (H1)$			
	XLa	Exchange DP_L with working register La		a				The DP_L contents and the contents of working register La are exchanged. La is assigned either of L0 or L1 according to a.		
	XL0		1 1 1 1	0 0 0 0	1	1	$(DP_L) \rightleftarrows (L0)$			
	XL1		1 1 1 1	0 1 0 0	1	1	$(DP_L) \rightleftarrows (L1)$			
Flag manipulation instructions	SFB flag	Set flag bit	0 1 0 1	$B_3 B_2 B_1 B_0$	1	1	$Fn \leftarrow 1$	The flag specified with $B_3 B_2 B_1 B_0$ is set.		
	RFB flag	Reset flag bit	0 0 0 1	$B_3 B_2 B_1 B_0$	1	1	$Fn \leftarrow 0$	The flag specified with $B_3 B_2 B_1 B_0$ is reset.	ZF	The flags are divided into 4 groups of F_0 to F_3, F_4 to F_7, F_8 to F_{11}, F_{12} to F_{15}. The ZF is set/reset according to the 4 bits including a single bit specified with the immediate data $B_3 B_2 B_1 B_0$.
Jump/subroutine instructions	JMP addr	Jump in the current bank	0 1 1 0 $P_7 P_6 P_5 P_4$	1 $P_{10} P_9 P_8$ $P_3 P_2 P_1 P_0$	2	2	$PC \leftarrow PC_{11}$ (又は $\overline{PC_{11}}$) $P_{10} P_9 P_8 P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$	A jump to the address specified with the PC_{11} (or $\overline{PC_{11}}$) and immediate data $P_{10} P_9 P_8 P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ occurs.		If the BANK and JMP instructions are executed consecutively, $\overline{PC_{11}} \longrightarrow PC_{11}$.
	JPEA	Jump in the current page modified by E and AC	1 1 1 1	1 0 1 0	1	1	$PC_{7 \sim 0} \leftarrow (E.AC)$	A jump to the address specified with the contents of the PC whose low-order 8 bits are replaced by the E and AC contents occurs.		
	CZP addr	Call subroutine in the zero page	1 0 1 1	$P_3 P_2 P_1 P_0$	1	1	$STACK \leftarrow (PC)+1$ $PC_{11 \sim 6}, PC_{1 \sim 0} \leftarrow 0$ $PC_{5 \sim 2} \leftarrow P_3 P_2 P_1 P_0$	A subroutine in page 0 of bank 0 is called.		
	CAL addr	Call subroutine in the zero bank	1 0 1 0 $P_7 P_6 P_5 P_4$	1 $P_{10} P_9 P_8$ $P_3 P_2 P_1 P_0$	2	2	$STACK \leftarrow (PC)+2$ $PC_{11 \sim 0} \leftarrow 0 P_{10} P_9 P_8 P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$	A subroutine in bank 0 is called.		
	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	1	$PC \leftarrow (STACK)$	A return from a subroutine occurs.		
	RTI	Return from interrupt routine	0 0 1 0	0 0 1 0	1	1	$PC \leftarrow (STACK)$ $CF\ ZF \leftarrow CSF.ZSF$	A return from an interrupt service routine occurs.	ZF CF	
	BANK	Change bank	1 1 1 1	1 1 0 1	1	1	$PC_{11} \leftarrow (\overline{PC_{11}})$	The bank is changed.		Effective only when used immediately before the JMP instruction.
Branch instructions	BAt addr	Branch on AC bit	0 1 1 1 $P_7 P_6 P_5 P_4$	0 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7 \sim 0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if ACt = 1	If a single bit of the AC specified with the immediate data $t_1 t_0$ is 1, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BA0 to BA3 according to the value of t.
	BNAt addr	Branch on no AC bit	0 0 1 1 $P_7 P_6 P_5 P_4$	0 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7 \sim 0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if ACt = 0	If a single bit of the AC specified with the immediate data $t_1 t_0$ is 0, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BNA0 to BNA3 according to the value of t.
	BMt addr	Branch on M bit	0 1 1 1 $P_7 P_6 P_5 P_4$	0 1 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7 \sim 0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if (M(DP.$t_1 t_0$)) = 1	If a single bit of the M(DP) specified with the immediate data $t_1 t_0$ is 1, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BM0 to BM3 according to the value of t.
	BNMt addr	Branch on no M bit	0 0 1 1 $P_7 P_6 P_5 P_4$	0 1 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7 \sim 0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if (M(DP.$t_1 t_0$)) = 0	If a single bit of the M(DP) specified with the immediate data $t_1 t_0$ is 0, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BNM0 to BNM3 according to the value of t.
	BPt addr	Branch on Port bit	0 1 1 1 $P_7 P_6 P_5 P_4$	1 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7 \sim 0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if (P(DP_L $t_1 t_0$)) = 1	If a single bit of port P(DP_L) specified with the immediate data $t_1 t_0$ is 1, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BP0 to BP3 according to the value of t.
	BNPt addr	Branch on no Port bit	0 0 1 1 $P_7 P_6 P_5 P_4$	1 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7 \sim 0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if (P(DP_L $t_1 t_0$)) = 0	If a single bit of port P(DP_L) specified with the immediate data $t_1 t_0$ is 0, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BNP0 to BNP3 according to the value of t.
	BTM addr	Branch on timer	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 0 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7 \sim 0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if TMF = 1 then TMF ← 0	If the TMF is 1, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs. The TMF is reset.	TMF	

Instruction group	Mnemonic		Instruction code $D_7 D_6 D_5 D_4$	Instruction code $D_3 D_2 D_1 D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Branch instructions	BNTM addr	Branch on no timer	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 0 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if TMF = 0 then TMF ← 0	If the TMF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The TMF is reset.	TMF	
	BI addr	Branch on interrupt	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 0 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if EXTF = 1 then EXTF ← 0	If the EXTF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The EXTF is reset.	EXTF	
	BNI addr	Branch on no interrupt	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 0 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if EXTF = 0 then EXTF ← 0	If the EXTF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The EXTF is reset.	EXTF	
	BC addr	Branch on CF	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 1 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if CF = 1	If the CF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BNC addr	Branch on no CF	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 1 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if CF = 0	If the CF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BZ addr	Branch on ZF	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 1 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \sim P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if ZF = 1	If the ZF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BNZ addr	Branch on no ZF	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 1 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if ZF = 0	If the ZF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BFn addr	Branch on flag bit	1 1 0 1 $P_7 P_6 P_5 P_4$	$n_3 n_2 n_1 n_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if Fn = 1	If the flag bit of the 16 flags specified with the immediate data $n_3n_2n_1n_0$ is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BF0 to BF15 according to the value of n.
	BNFn addr	Branch on no flag bit	1 0 0 1 $P_7 P_6 P_5 P_4$	$n_3 n_2 n_1 n_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if Fn = 0	If the flag bit of the 16 flags specified with the immediate data $n_3n_2n_1n_0$ is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNF0 to BNF15 according to the value of n.
Input/Output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← (P(DPL))	Port P(DP_L) contents are loaded in the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(DPL) ← (AC)	The AC contents are outputted to port P(DP_L).		
	SPB bit	Set port bit	0 0 0 0	0 1 B_1 B_0	1	2	P(DP_L, B_1B_0) ← 1	A single bit in port P(DP_L) specified with the immediate data B_1B_0 is set.		When this instruction is executed, the E contents are destroyed.
	RPB bit	Reset port bit	0 0 1 0	0 1 B_1 B_0	1	2	P(DP_L, B_1B_0) ← 0	A single bit in port P(DP_L) specified with the immediate data B_1B_0 is reset.	ZF	When this instruction is executed, the E contents are destroyed.
Other instructions	SCTL bit	Set control register bit(S)	0 0 1 0 1 0 0 0	1 1 0 0 B_3 B_2 B_1 B_0	2	2	CTL ← (CTL) V $B_3B_2B_1B_0$	The bits of the control register specified with the immediate data $B_3B_2B_1B_0$ are set.		
	RCTL bit	Reset control register bit(S)	0 0 1 0 1 0 0 1	1 1 0 0 B_3 B_2 B_1 B_0	2	2	CTL ← (CTL) Λ $\overline{B_3B_2B_1B_0}$	The bits of the control register specified with the immediate data $B_3B_2B_1B_0$ are reset.	ZF	
	WTTM	Write timer	1 1 1 1	1 0 0 1	1	1	TM ← (E), (AC) TMF ← 0	The E and AC contents are loaded in the timer. The TMF is reset.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	All operations stop.		Only when all pins of port PA are set at L, stop.
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

*1 If the CLA instruction is used consecutively in such a manner as CLA, CLA, ———, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.