

**MSM65524A/65P524****8-Bit Microcontroller with A/D Converter****GENERAL DESCRIPTION**

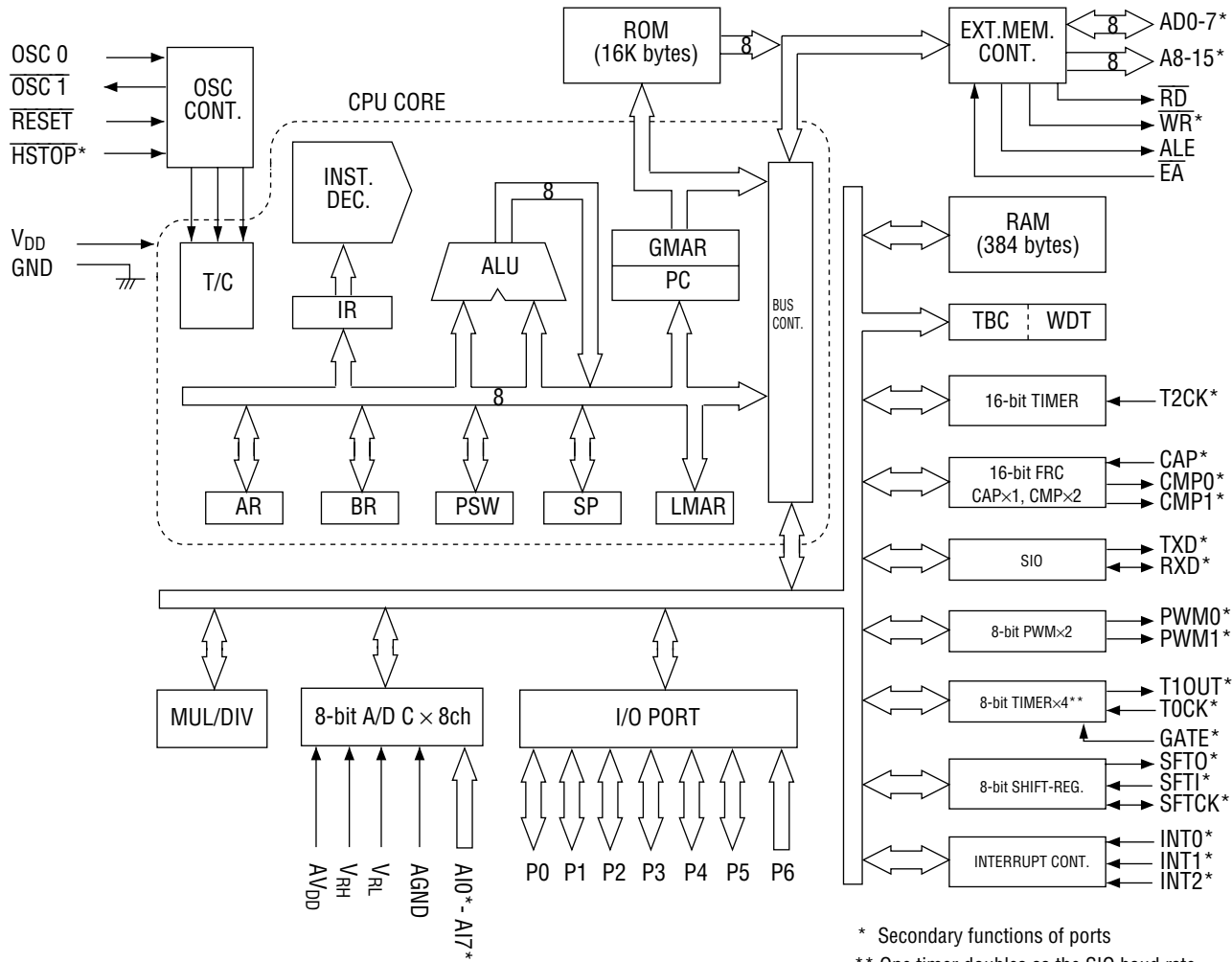
The MSM65524A is a high-performance 8-bit microcontroller that employs OKI original nX-8/50 CPU core. With a minimum instruction execution time of 400 ns (10MHz clock), the MSM65524A is capable of high-speed processing, and includes 16K bytes of program memory, 384 bytes of data memory, timers, serial ports, an A/D converter and PWMs on chip. Also available are the MSM65P524, which replaces the on-chip program memory with one-time PROM, and the MSM65X524A, which uses the external program memory.

**FEATURES**

- Operating range
  - Operating frequency : 0 to 10MHz ( $V_{DD}=4.5$  to 5.5V)  
0 to 5MHz ( $V_{DD}=2.7$  to 5.5V)
  - Operating voltage : 2.7 to 5.5V
  - Operating temperature :  $-40$  to  $+85^{\circ}\text{C}$
- Memory space : 64K bytes
  - Internal program memory : 16K bytes
  - Internal data memory : 384 bytes
- Minimum instruction execution time : 400ns @ 10 MHz
- Powerful instruction set : 83 basic instructions  
8/16-bit operation instructions  
Bit manipulation instructions  
Compound function instructions
- Abundant addressing modes
- Multiplication/division operation functions :  $8 \times 8 \rightarrow 16$   
 $16 \div 8 \rightarrow 16 \dots 8$
- I/O port
  - Input-output port : 5 ports  $\times$  8 bits  
1 port  $\times$  4 bits
  - Input port : 1 port  $\times$  8 bits
- Timers : 8-bit auto-reload timer  $\times$  2  
16-bit auto-reload timer  $\times$  1  
Watchdog timer  $\times$  1
- Counters : Time base counter  $\times$  1  
16-bit free-running counter  $\times$  1
- Capture input : 1 channel
- Compare output : 2 channels
- Serial ports : Shift register  $\times$  1  
Serial port with baud rate generator (UART/Synchronous)  $\times$  1
- A/D converter : 8 bits  $\times$  8 channels
- PWM : 8 bits  $\times$  2 channels  
PWM with auto-reload timer for period setting

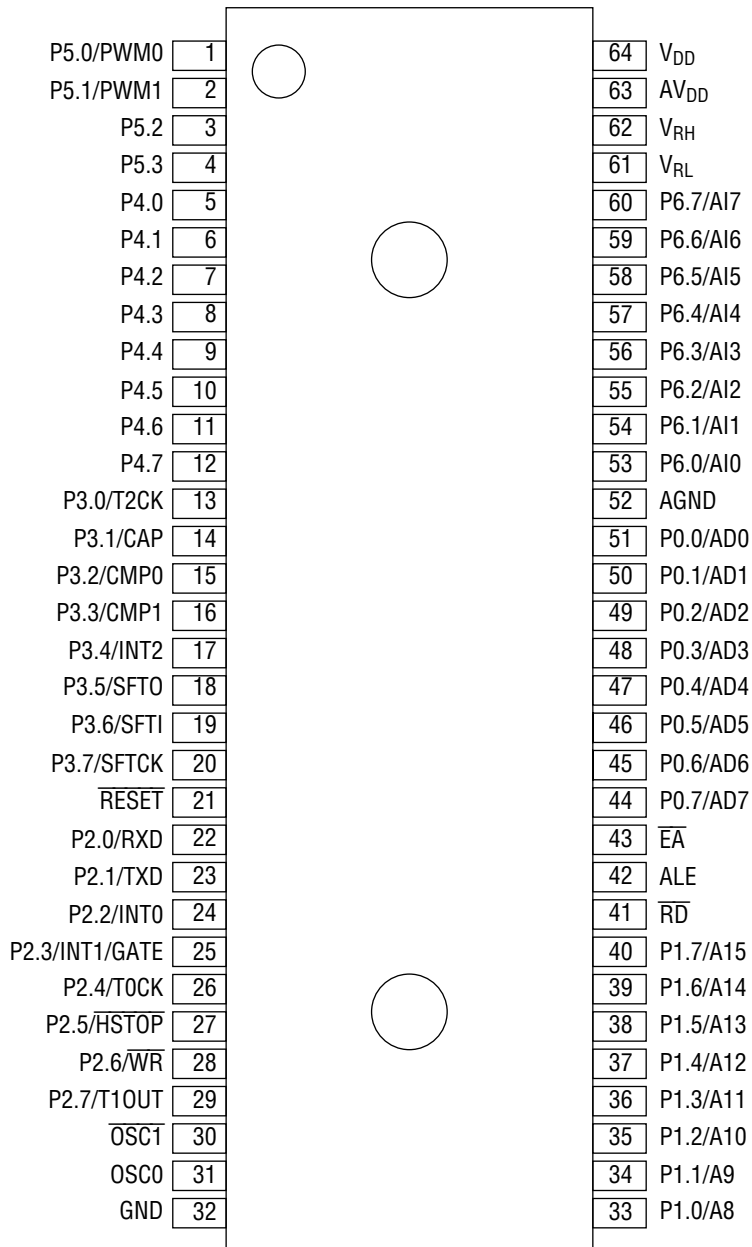
- External interrupts : 3
  - Interrupt sources : 19
  - Package options
    - 64-pin plastic shrink DIP (SDIP64-P-750-1.78) : (Product name: MSM65524A-xxxSS, MSM65P524-xxxSS)
    - 64-pin plastic QFP (QFP64-P-1414-0.80-BK) : (Product name: MSM65524A-xxxGS-BK, MSM65P524-xxxGS-BK)
    - 68-pin plastic QFJ (PLCC) (QFJ68-P-S950-1.27): (Product name: MSM65524A-xxxJS, MSM65P524-xxxJS)
- xxx indicates the code number.

**BLOCK DIAGRAM**



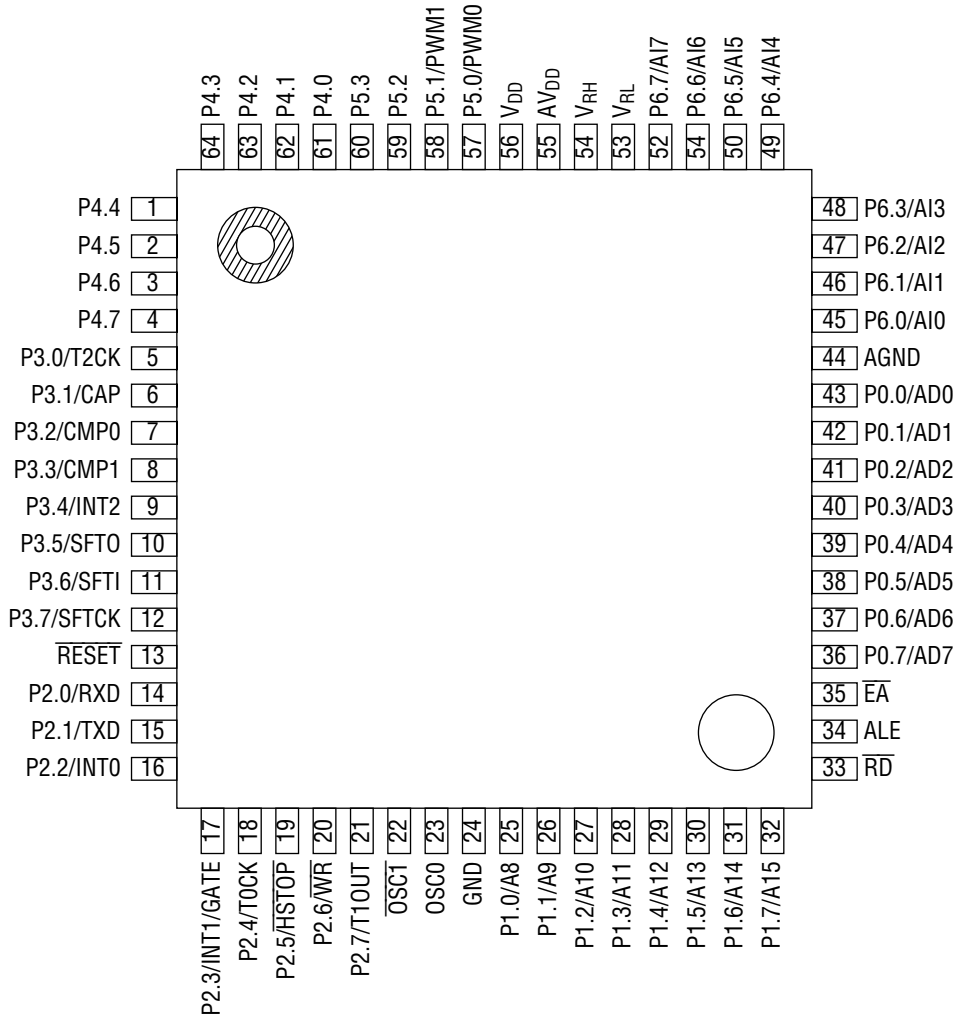
\* Secondary functions of ports  
 \*\* One timer doubles as the SIO baud rate generator, another doubles as a PWM clock source.

**PIN CONFIGURATION (TOP VIEW)**



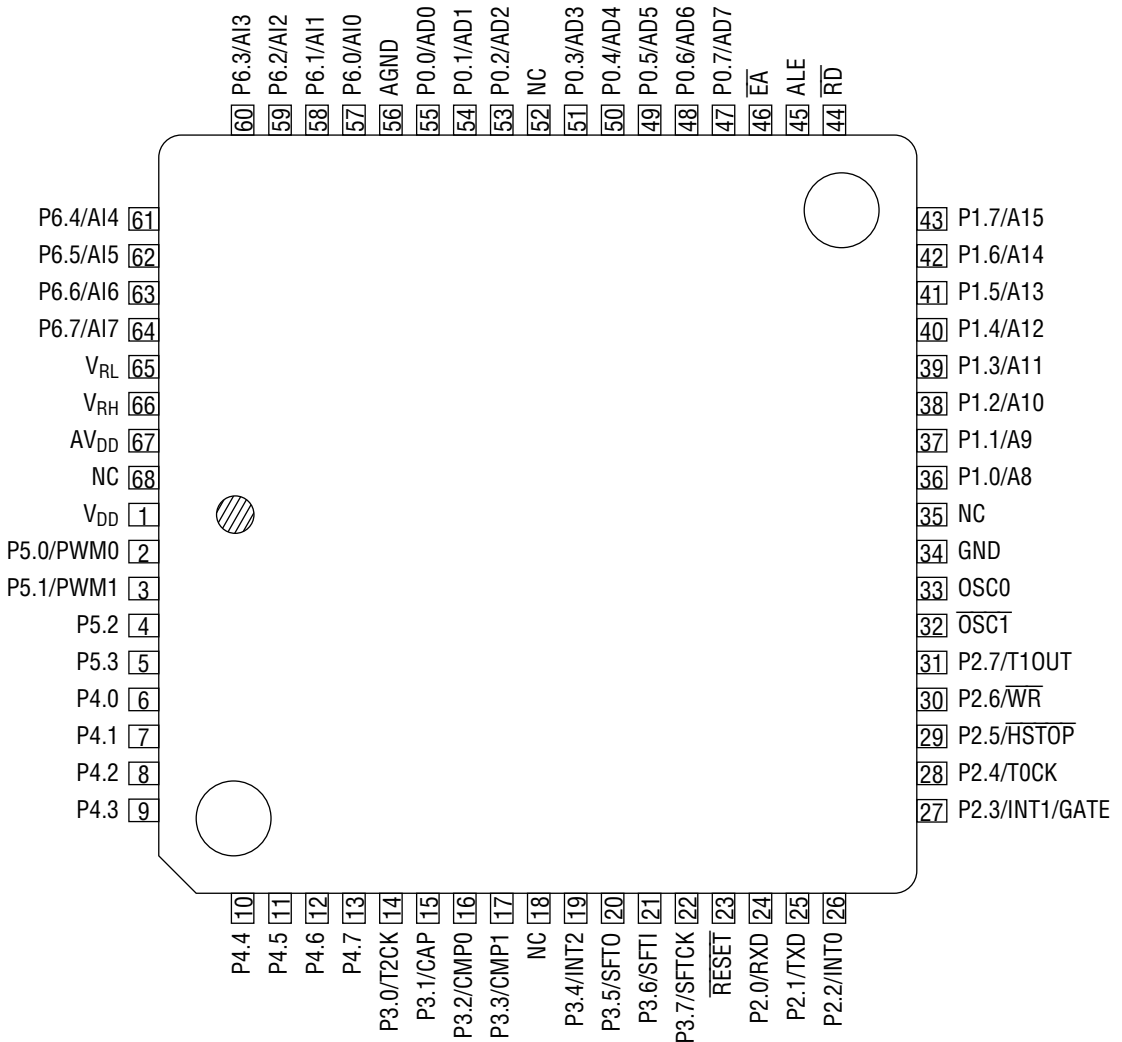
**64-Pin Plastic Shrink DIP**

**PIN CONFIGURATION (TOP VIEW) (Continued)**



**64-Pin Plastic QFP**

**PIN CONFIGURATION (TOP VIEW) (Continued)**



NC: No-connection pin

**68-Pin Plastic QFJ (PLCC)**

## PIN DESCRIPTION

### Basic Functions

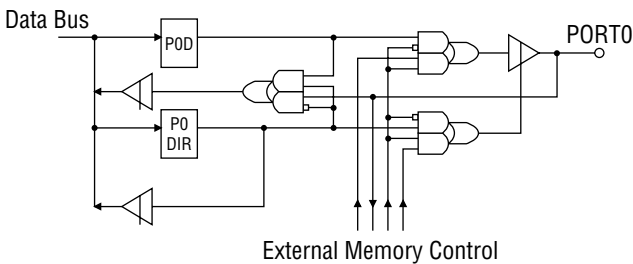
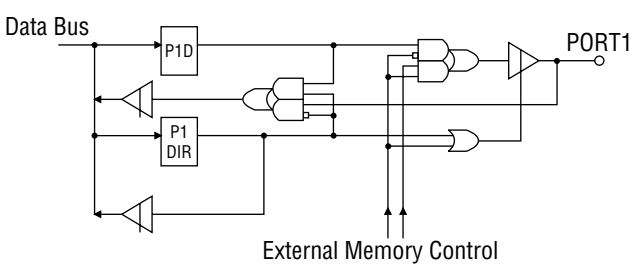
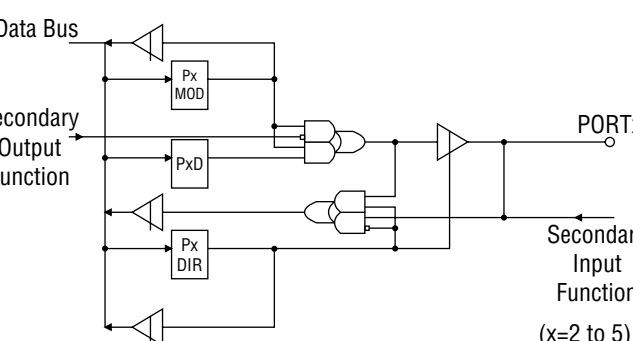
Function	Symbol	Type	Description
Power Supply	V <sub>DD</sub>	—	+5V digital power supply
	GND	—	0V digital ground
	AV <sub>DD</sub>	—	+5V analog power supply
	AGND	—	0V analog ground
	V <sub>RH</sub>	—	+5V analog reference voltage
	V <sub>RL</sub>	—	0V analog reference voltage
Oscillation	OSC0	I	System clock input pin. Quartz oscillator or ceramic oscillator is connected between OSC0 and $\overline{\text{OSC1}}$ . For external clock, input at OSC0, leaving $\overline{\text{OSC1}}$ open.
	$\overline{\text{OSC1}}$	O	System clock output pin
Control	$\overline{\text{RESET}}$	I	System reset input (program starts from address 0040H); internal pull-up resistance
	$\overline{\text{EA}}$	I	Program memory select input pin. "L" level input for external program memory; "H" level input for internal program memory.
	$\overline{\text{RD}}$	O	Read strobe signal during external memory access
	ALE	O	Address latch signal during external memory access
Port	PORT 0	I/O	8-bit Input-output port During external memory access, becomes address/data bus for address output, instruction fetch or data read/write along with ALE, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pins.
	PORT 1	I/O	8-bit Input-output port Address bus during external memory access
	PORT 2 PORT 3 PORT 4	I/O	8-bit Input-output port × 3. Secondary functions shown in following table are added for ports 2 and 3.
	PORT 5	I/O	4-bit Input-output port Secondary functions shown in following table are added for port 5.
	PORT 6	I	8-bit Input port Functions as analog input channel during A/D conversion.

## Secondary Functions

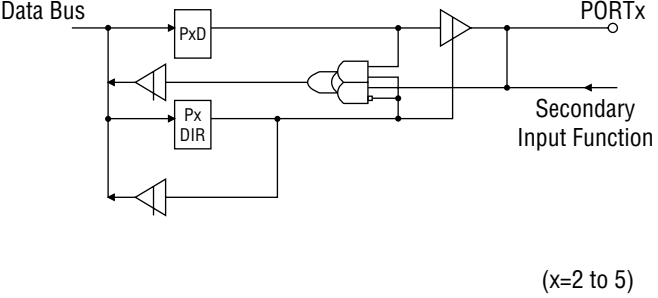

Symbol	Type	Description
RXD	I/O	P2.0 secondary function UART: Input pin for serial port receive data. Synchronous: Input/output pin for serial port transmit/receive data.
TXD	0	P2.1 secondary function UART: Output pin for serial port transmit data. Synchronous: Output pin for serial port synchronizing clock.
INT0	I	P2.2 secondary function External interrupt 0 input pin.
INT1/GATE	I	P2.3 secondary functions External interrupt 1 input pin. Also used as input pin for gate signal for timer 0 count enable/disable.
T0CK	I	P2.4 secondary function Timer 0 external clock input pin.
$\overline{\text{HSTOP}}$	I	P2.5 secondary function Hard stop mode input pin; stops system clock oscillation with "L" level input.
$\overline{\text{WR}}$	0	P2.6 secondary function Write strobe signal output pin during external data memory access.
T1OUT	0	P2.7 secondary function Output pin for signal that 2-divided timer 1 overflow.
T2CK	I	P3.0 secondary function Timer 2 external clock input pin.
CAP	I	P3.1 secondary function Capture trigger input pin.
CMP0	0	P3.2 secondary function Compare output channel 0 output pin.
CMP1	0	P3.3 secondary function Compare output channel 1 output pin.
INT2	I	P3.4 secondary function External interrupt 2 input signal.
SFT0	0	P3.5 secondary function Shift register data output pin.
SFTI	I	P3.6 secondary function Shift register data input pin.
SFTCK	I/O	P3.7 secondary function Shift register synchronizing clock input/output pin.
PWM0	0	P5.0 secondary function PWM channel 0 output pin.
PWM1	0	P5.1 secondary function PWM channel 1 output pin.



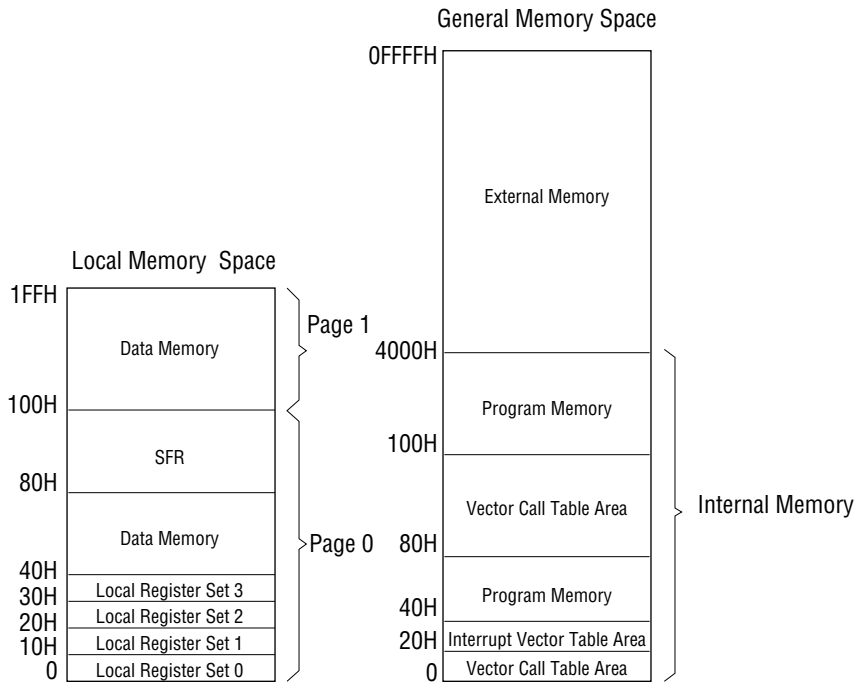
Port Circuit Configuration

Type	Port	Circuit Configuration	Electrical Characteristics (V <sub>DD</sub> =5V)
1	P0.0/AD0 to P0.7/AD7	 <p>The diagram shows the internal circuitry of Port 0. It features a Data Bus connected to a POD (Port Output Driver) and a P0 DIR (Port 0 Direction Register). The circuit includes several logic gates (AND, OR, NOT) that control the output driver and the direction of the port. An External Memory Control block is also shown, which provides control signals to the port's internal logic. The output of the port is labeled PORT0.</p>	<p>"H" Input Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>IH</sub>=2.4V</li> </ul> <p>"L" Input Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>IL</sub>=0.8V</li> </ul> <p>"H" Output Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>OH</sub>=3.75V</li> <li>• I<sub>OH</sub>=-400μA</li> </ul> <p>"L" Output Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>OL</sub>=0.4V</li> <li>• I<sub>OL</sub>=3.2mA</li> </ul>
2	P1.0/A8 to P1.7/A15	 <p>The diagram shows the internal circuitry of Port 1. It features a Data Bus connected to a P1D (Port 1 Data Register) and a P1 DIR (Port 1 Direction Register). The circuit includes several logic gates (AND, OR, NOT) that control the output driver and the direction of the port. An External Memory Control block is also shown, which provides control signals to the port's internal logic. The output of the port is labeled PORT1.</p>	<p>"H" Input Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>IH</sub>=2.4V</li> </ul> <p>"L" Input Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>IL</sub>=0.8V</li> </ul> <p>"H" Output Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>OH</sub>=3.75V</li> <li>• I<sub>OH</sub>=-200μA</li> </ul> <p>"L" Output Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>OL</sub>=0.4V</li> <li>• I<sub>OL</sub>=1.6mA</li> </ul>
3	P2.0/RXD, P2.1/TXD, P2.6/ $\overline{WR}$ , P2.7/T1OUT, P3.2/CMP0, P3.3/CMP1, P3.5/SFT0, P3.7/SFTCK, P5.0/PWM0, P5.1/PMW1	 <p>The diagram shows the internal circuitry of Port x. It features a Data Bus connected to a Px MOD (Port x Mode Register) and a Px DIR (Port x Direction Register). The circuit includes several logic gates (AND, OR, NOT) that control the output driver and the direction of the port. A Secondary Output Function block is also shown, which provides control signals to the port's internal logic. The output of the port is labeled PORTx. The diagram also indicates a Secondary Input Function for ports x=2 to 5.</p>	<p>"H" Input Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>IH</sub>=2.4V</li> </ul> <p>"L" Input Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>IL</sub>=0.8V</li> </ul> <p>P2.6/<math>\overline{WR}</math></p> <p>"H" Output Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>OH</sub>=3.75V</li> <li>• I<sub>OH</sub>=-400μA</li> </ul> <p>"L" Output Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>OL</sub>=0.4V</li> <li>• I<sub>OL</sub>=3.2mA</li> </ul> <p>Ports other than P2.6/<math>\overline{WR}</math></p> <p>"H" Output Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>OH</sub>=3.75V</li> <li>• I<sub>OH</sub>=-200μA</li> </ul> <p>"L" Output Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>OL</sub>=0.4V</li> <li>• I<sub>OL</sub>=1.6mA</li> </ul>

Port Circuit Configuration (Continued)

Type	Port	Circuit Configuration	Electrical Characteristics (V <sub>DD</sub> =5V)
4	P2.2/INT0, P2.3/INT1/GATE, P2.4/TOCK, P2.5/HSTOP, P3.0/T2CK, P3.1/CAP, P3.4/INT2, P3.6/SFTI, P4.0 to P4.7, P5.2 to P5.3	 <p style="text-align: right;">(x=2 to 5)</p>	"H" Input Voltage: • V <sub>IH</sub> =2.4V "L" Input Voltage: • V <sub>IL</sub> =0.8V  "H" Output Voltage: • V <sub>OH</sub> =3.75V • I <sub>OH</sub> =-200μA  "L" Output Voltage: • V <sub>OL</sub> =0.4V • I <sub>OL</sub> =1.6mA
5	P6.0/AI0 to P6.7/AI7		"H" Input Voltage: • V <sub>IH</sub> =2.4V "L" Input Voltage: • V <sub>IL</sub> =0.8V

MEMORY MAPS



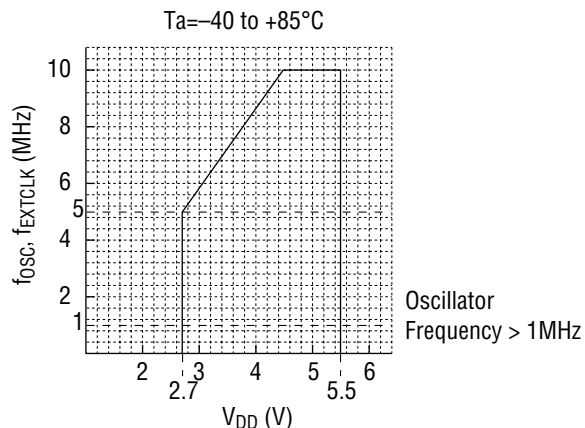
**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	$V_{DD}=AV_{DD}$	$T_a=25^{\circ}\text{C}$ $GND=AGND=0V$	-0.3 to 7.0	V
Input Voltage	$V_I$		-0.3 to $V_{DD}+0.3$	
Output Voltage	$V_O$		-0.3 to $V_{DD}+0.3$	
Analog Reference Voltage	$V_{RH}, V_{RL}$		-0.3 to $V_{DD}+0.3$	
Analog Input Voltage	$V_{AI}$		-0.3 to $V_{DD}+0.3$	
Power Dissipation	$P_D$	$T_a=25^{\circ}\text{C}$ per package	400	mW
Storage Temperature	$T_{STG}$	—	-55 to +150	$^{\circ}\text{C}$

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	$V_{DD}$	Refer to Figure 1.	2.7 to 5.5	V
Analog Supply Voltage	$AV_{DD}$	$V_{DD}=AV_{DD}=V_{RH}$	2.7 to 5.5	
Analog Reference Voltage	$V_{RH}$	$GND=AGND=V_{RL}=0V$	2.7 to 5.5	
Analog Input Voltage	$V_{AI}$		0 to $V_{DD}$	
Memory Hold Voltage	$V_{DDMH}$	$f_{OSC}=0\text{ Hz}$	2.0 to 5.5	
Operating Frequency *1	$f_{OSC}$	Refer to Figure 1.	1 to 10	MHz
External Clock Operating Frequency	$f_{EXTCLK}$	Refer to Figure 1.	0 to 10	MHz
Operating Temperature	$T_{op}$	—	-40 to +85	$^{\circ}\text{C}$

\*1 This is due to the standard of a crystal oscillator or resonator.



**Figure 1. Power Supply Voltage vs. Operating Frequency**

**ELECTRICAL CHARACTERISTICS**

**DC Characteristics 1 (V<sub>DD</sub>=4.5 to 5.5V)**

(GND=0V, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1	*1 V <sub>IH1</sub>	—	2.4	—	V <sub>DD</sub> +0.3	V
"H" Input Voltage 2	*2 V <sub>IH2</sub>	—	0.7V <sub>DD</sub>	—	V <sub>DD</sub> +0.3	
"L" Input Voltage	V <sub>IL</sub>	—	-0.3	—	0.8	
"H" Output Voltage 1	*3 V <sub>OH1</sub>	I <sub>OH</sub> =-200μA	0.75V <sub>DD</sub>	—	—	
"H" Output Voltage 2	*4 V <sub>OH2</sub>	I <sub>OH</sub> =-400μA	0.75V <sub>DD</sub>	—	—	
"L" Output Voltage 1	*3 V <sub>OL1</sub>	I <sub>OL</sub> =1.6mA	—	—	0.4	
"L" Output Voltage 2	*4 V <sub>OL2</sub>	I <sub>OL</sub> =3.2mA	—	—	0.4	
Input Leakage Current 1	*5 I <sub>LI1</sub>	V <sub>I</sub> =V <sub>DD</sub> /0V	—	—	±1	
Input Leakage Current 2	*6 I <sub>LI2</sub>	V <sub>I</sub> =V <sub>DD</sub> /0V	—	—	±10	
"L" Input Current	*7 I <sub>IL</sub>	V <sub>I</sub> =0V	-40	-120	-400	
Input Capacitance	C <sub>I</sub>	f=1MHz, Ta=25°C	—	5	—	pF
Static Current Consumption	I <sub>DSS</sub>	5V, stop mode *8	—	—	50	μA
Dynamic Current Consumption	I <sub>DD</sub>	10MHz, 5V, no load Refer to Figure2	—	20	40	mA

\*1 Excluding OSC0 and  $\overline{\text{RESET}}$

\*2 OSC0 and  $\overline{\text{RESET}}$

\*3 Excluding P0, ALE,  $\overline{\text{RD}}$ , P2.6/ $\overline{\text{WR}}$

\*4 P0, ALE,  $\overline{\text{RD}}$ , P2.6/ $\overline{\text{WR}}$

\*5  $\overline{\text{EA}}$ , P6

\*6 Excluding  $\overline{\text{RESET}}$ ,  $\overline{\text{EA}}$ , P6

\*7  $\overline{\text{RESET}}$

\*8 The ports set for input mode are V<sub>DD</sub> or 0V and the ports except these are no load.

DC Characteristics 2 ( $2.7 \leq V_{DD} < 4.5V$ )

(GND=0V, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1	*1 $V_{IH1}$	—	$0.5V_{DD}+0.2$	—	$V_{DD}+0.3$	V
"H" Input Voltage 2	*2 $V_{IH2}$	—	$0.6V_{DD}+0.4$	—	$V_{DD}+0.3$	
"L" Input Voltage	$V_{IL}$	—	-0.3	—	$0.15V_{DD}+0.1$	
"H" Output Voltage 1	*3 $V_{OH1}$	$I_{OH}=-10\mu A$	$0.75V_{DD}$	—	—	
"H" Output Voltage 2	*4 $V_{OH2}$	$I_{OH}=-20\mu A$	$0.75V_{DD}$	—	—	
"L" Output Voltage 1	*3 $V_{OL1}$	$I_{OL}=10\mu A$	—	—	0.1	
"L" Output Voltage 2	*4 $V_{OL2}$	$I_{OL}=20\mu A$	—	—	0.1	
Input Leakage Current 1	*5 $I_{LI1}$	$V_I=V_{DD}/0V$	—	—	$\pm 1$	
Input Leakage Current 2	*6 $I_{LI2}$	$V_I=V_{DD}/0V$	—	—	$\pm 10$	
"L" Input Current	*7 $I_{IL}$	$V_{DD}=2.7$ to $3.3V$ $V_I=0V$	-40	-120	-240	
Input Capacitance	$C_I$	$f=1MHz, T_a=25^\circ C$	—	5	—	pF
Static Current Consumption	$I_{DSS}$	3V, stop mode *8	—	—	25	$\mu A$
Dynamic Current Consumption	$I_{DD}$	5MHz, 3V, no load Refer to Figure 2	—	6	15	mA

\*1 Excluding OSC0 and  $\overline{RESET}$

\*2 OSC0 and  $\overline{RESET}$

\*3 Excluding P0, ALE,  $\overline{RD}$ , P2.6/ $\overline{WR}$

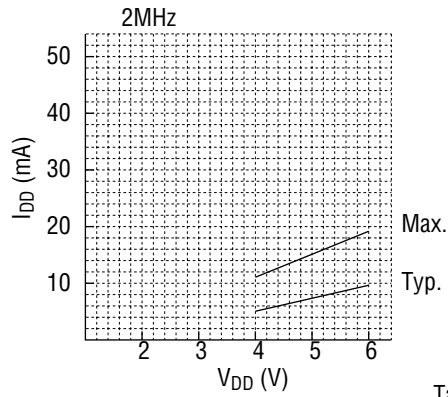
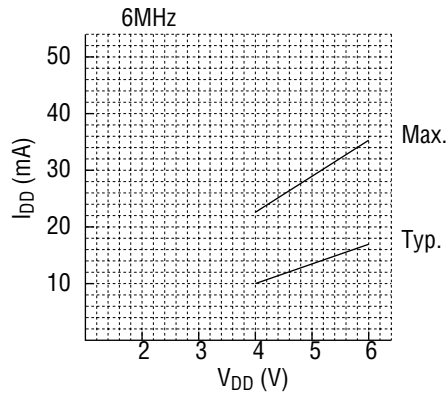
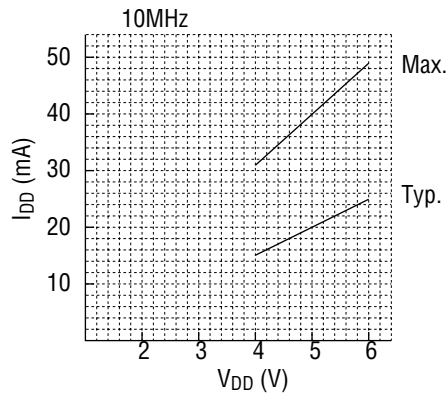
\*4 P0, ALE,  $\overline{RD}$ , P2.6/ $\overline{WR}$

\*5  $\overline{EA}$ , P6

\*6 Excluding  $\overline{RESET}$ , EA, P6

\*7  $\overline{RESET}$

\*8 The ports set for input mode are  $V_{DD}$  or 0V and the ports except these are no load.



T<sub>a</sub> = -40 to +85°C, no load

Figure 2. Voltage vs. Current

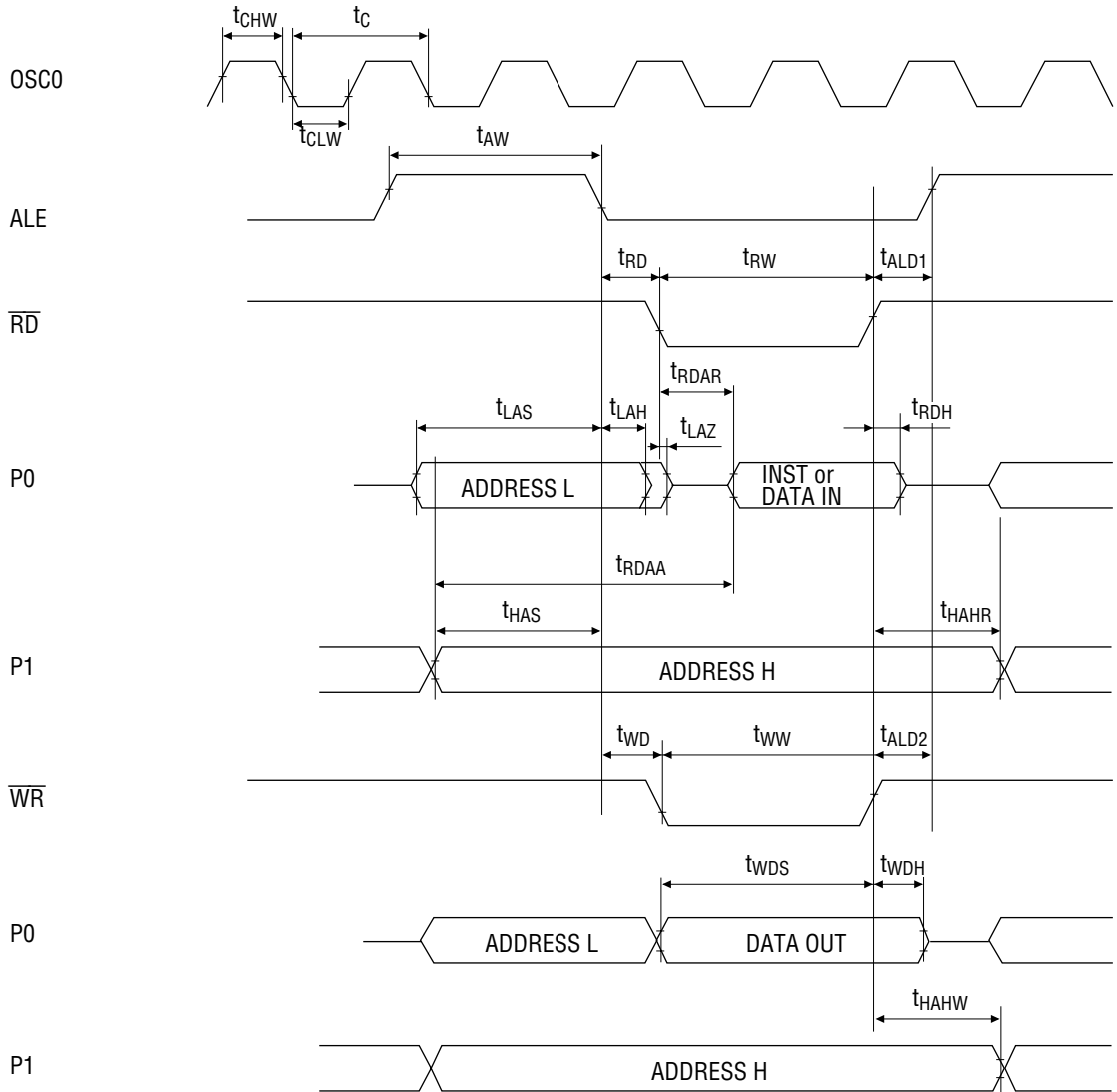
**AC Characteristics**

• **External memory control**

( $V_{DD}=AV_{DD}=V_{RH}=2.7$  to  $5.5V$ ,  $GND=AGND=V_{RL}=0V$ ,  $T_a=-40$  to  $+85^{\circ}C$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Period	$t_c$	$V_{DD}=4.5$ to $5.5V$	100	—	ns
"L" Clock Pulse Width	$t_{CLW}$		45	—	
"H" Clock Pulse Width	$t_{CHW}$		45	—	
Clock Period	$t_c$	$V_{DD}=2.7$ to $5.5V$	200	—	
"L" Clock Pulse Width	$t_{CLW}$		90	—	
"H" Clock Pulse Width	$t_{CHW}$		90	—	
ALE Pulse Width	$t_{AW}$	$C_L=100pF$	$t_c+t_{CHW}-20$	—	
ALE Pulse Delay Time 1	$t_{ALD1}$		$t_{CLW}-20$	—	
ALE Pulse Delay Time 2	$t_{ALD2}$		$t_{CLW}-20$	—	
$\overline{RD}$ Pulse Width	$t_{RW}$		$t_c+t_{CHW}-20$	—	
$\overline{RD}$ Pulse Delay Time	$t_{RD}$		$t_{CLW}-20$	$t_{CLW}+20$	
$\overline{WR}$ Pulse Width	$t_{WW}$		$t_c+t_{CHW}-40$	—	
$\overline{WR}$ Pulse Delay Time	$t_{WD}$		$t_{CLW}-20$	$t_{CLW}+40$	
"L" Address Setup Time	$t_{LAS}$		$t_c-40$	—	
"H" Address Setup Time	$t_{HAS}$		$t_c-40$	—	
"L" Address Hold Time	$t_{LAH}$		$t_{CLW}-20$	—	
Bus Float Time	$t_{LAZ}$		—	20	
"H" Address Hold Time	$t_{HAHR}$		$t_c-20$	—	
"H" Address Hold Time	$t_{HAHW}$		$t_c-20$	—	
Read Data Access Time	$t_{RDAA}$		—	$t_c+t_{CLW}-15$	
Read Data Access Time	$t_{RDAR}$		—	$t_{CHW}+10$	
Read Data Hold Time	$t_{RDH}$		0	—	
Write Data Setup Time	$t_{WDS}$		$t_c+t_{CHW}-40$	—	
Write Data Hold Time	$t_{WDH}$	$t_{CLW}-20$	—		





• CPU control

( $V_{DD}=AV_{DD}=V_{RH}=2.7$  to  $5.5V$ ,  $GND=AGND=V_{RL}=0V$ ,  $T_a=-40$  to  $+85^{\circ}C$ )

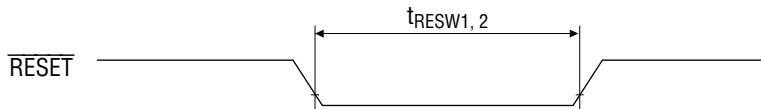
Parameter	Symbol	Condition	Min.	Max.	Unit
RESET Pulse Width *1	$t_{RESW1}$	—	20	—	ns
RESET Pulse Width *2	$t_{RESW2}$	—	*3	—	—

\*1 Excluding power ON, stop mode and hard stop mode.

\*2 In power ON, stop mode and hard stop mode.

\*3 Oscillation stabilization time depends on resonator.

RESET Pulse Width

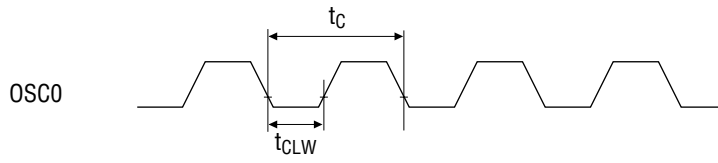


• Peripheral control 1

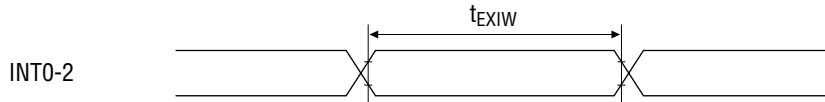
( $V_{DD}=AV_{DD}=V_{RH}=2.7$  to  $5.5V$ ,  $GND=AGND=V_{RL}=0V$ ,  $T_a=-40$  to  $+85^{\circ}C$ )

Parameter	Symbol	Condition	Min.	Max.	Unit	
OSC	Clock Period	$t_c$	$V_{DD}=4.5$ to $5.5V$	100	—	ns
			$V_{DD}=2.7$ to $5.5V$	200	—	
EXI	External Interrupt Pulse Width	—	$4 t_c$	—		
T0	External Clock Pulse Width		$4 t_c$	—		
	GATE Pulse Width		$1 t_{TOCLK}^{*1}$	—		
T2	External Clock Pulse Width		$4 t_c$	—		
CAP	CAP Pulse Width		$12 t_c$	—		

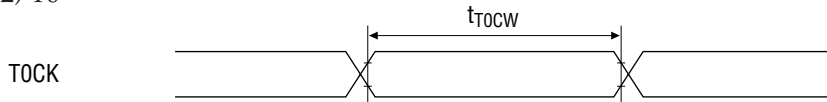
\*1  $t_{TOCLK}$  : Timer 0 count clock period selected by T0CON.



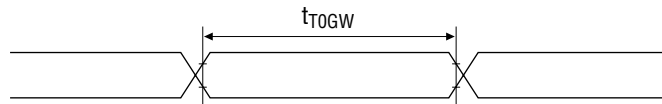
1) EXI pulse width



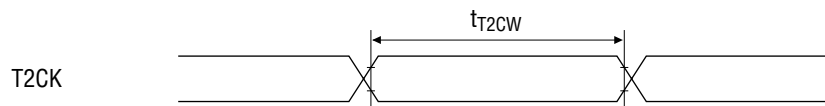
2) T0



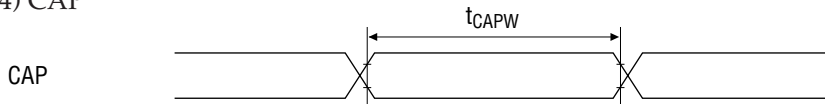
GATE



3) T2



4) CAP

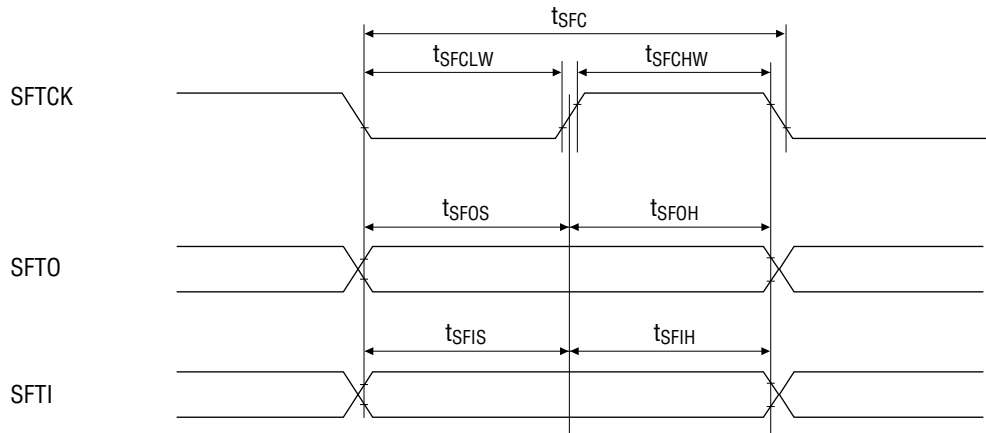


• Peripheral control 2

( $V_{DD}=AV_{DD}=V_{RH}=2.7\sim 5.5V$ ,  $GND=AGND=V_{RL}=0V$ ,  $T_a=-40$  to  $+85^{\circ}C$ )

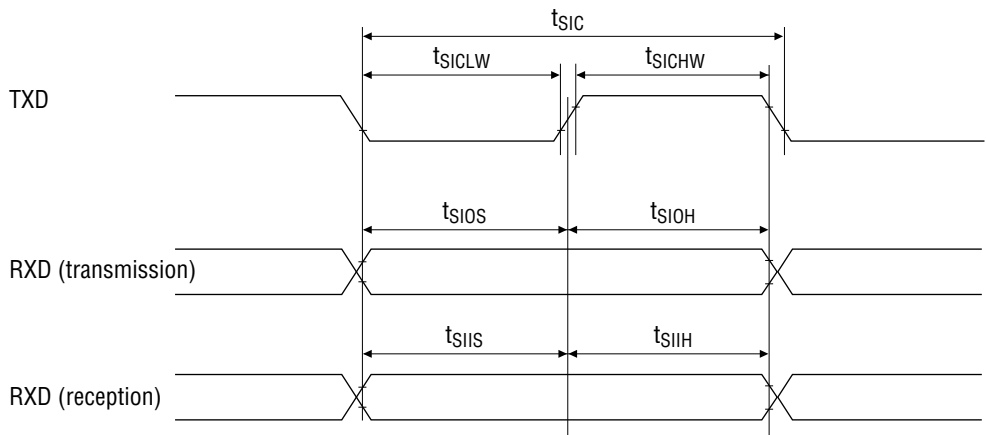
Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Period	$t_c$	$V_{DD}=4.5$ to $5.5V$	100	—	ns
			$V_{DD}=2.7$ to $5.5V$	200	—	
SFT	SFTCK Period	$t_{SFC}$	$C_L=100pF$	$8 t_c$	—	
	SFTCK "L" Pulse Width	$t_{SFCLW}$		$4 t_c-20$	—	
	SFTCK "H" Pulse Width	$t_{SFCHW}$		$4 t_c-20$	—	
	SFTCK Setup Time	$t_{SFOS}$		$t_{SFCLW}-100$	—	
	SFTO Hold Time	$t_{SFOH}$		$t_{SFCHW}-100$	—	
	SFTI Setup Time	$t_{SFIS}$		100	—	
	SFTI Hold Time	$t_{SFIH}$		100	—	
SIO (Clock Synchronous Mode)	Synchronous Clock Period	$t_{SIC}$	$C_L=100pF$	$8 t_c$	—	
	Synchronous Clock "L" Pulse Width	$t_{SICLW}$		$4 t_c-20$	—	
	Synchronous Clock "H" Pulse Width	$t_{SICHW}$		$4 t_c-20$	—	
	Output Data Setup Time	$t_{SIOS}$		$6 t_c-100$	—	
	Output Data Hold Time	$t_{SIOH}$		$2 t_c-100$	—	
	Input Data Setup Time	$t_{SIIS}$		$t_c+t_{CLW}+100$	—	
	Input Data Hold Time	$t_{SIIH}$		0	—	

1) SFT



2) SIO

(Clock synchronous mode)



**A/D Converter Characteristics 1**

( $V_{DD}=AV_{DD}=V_{RH}=5V\pm 10\%$ ,  $GND=AGND=V_{RL}=0V$ ,  $T_a=-40$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	See the recommended circuit (Fig. 3).  Analog input source impedance $R_I \leq 5k\Omega$	—	8	—	bit
Absolute Error	$E_L$		—	—	+1.5 -1.5	LSB
Differential Linearity Error	$E_D$		—	—	$\pm 0.5$	LSB
Zero Point Error	$E_{ZS}$		—	—	+1.5	LSB
Full Scale Error	$E_{FS}$		—	—	-1.5	LSB
Crosstalk	$E_{CT}$	See the measuring circuit (Fig. 4).	—	—	$\pm 0.5$	LSB
Conversion time *	$t_{CONV}$	$f_{OSC}=10$ MHz	—	16	—	$\mu s/CH$

\* The transition time after the G0 bit goes to "1" is 14.8 $\mu s/CH$ .

**A/D Converter Characteristics 2**

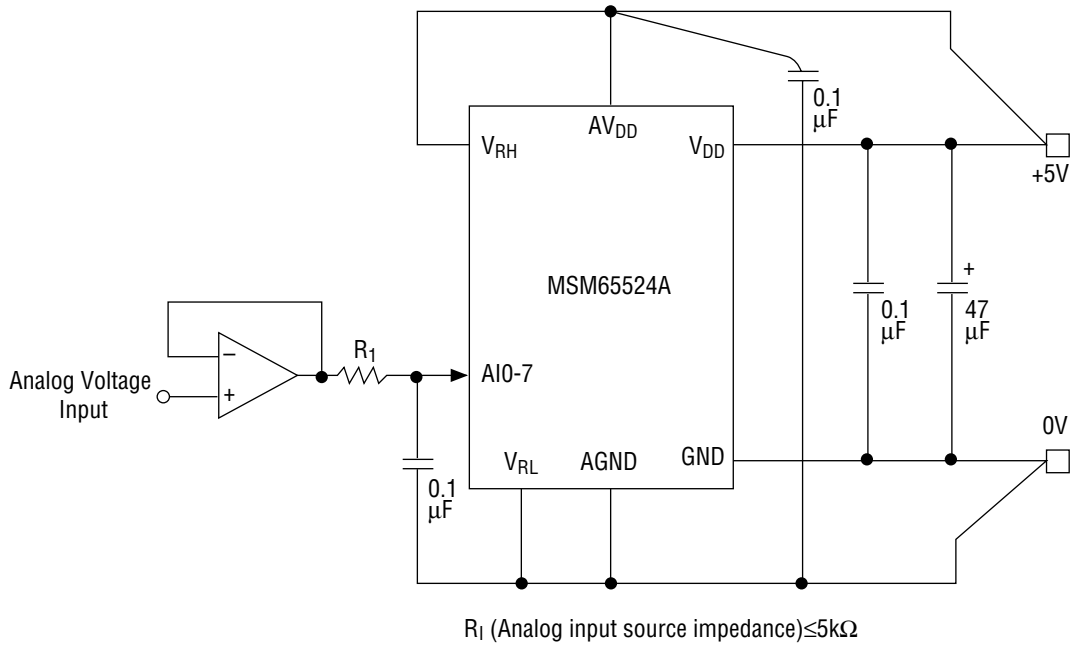
( $V_{DD}=AV_{DD}=V_{RH}=2.7$  to  $4.5V$ ,  $GND=AGND=V_{RL}=0V$ ,  $T_a=-40$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	See the recommended circuit (Fig. 3).  Analog input source impedance $R_I \leq 5k\Omega$	—	8	—	bit
Absolute Error	$E_L$		—	—	+2 -2	LSB
Differential Linearity Error	$E_D$		—	—	$\pm 1$	LSB
Zero Point Error	$E_{ZS}$		—	—	+2	LSB
Full Scale Error	$E_{FS}$		—	—	-2	LSB
Crosstalk	$E_{CT}$	See the measuring circuit (Fig. 4).	—	—	$\pm 1$	LSB
Conversion time *	$t_{CONV}$	$f_{OSC}=5$ MHz	—	32	—	$\mu s/CH$

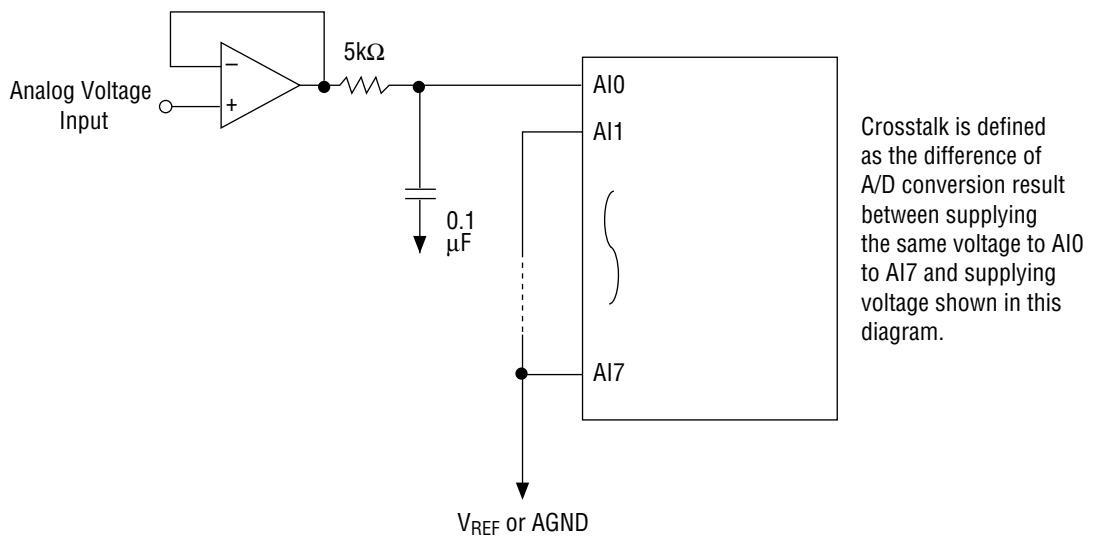
\* The transition time after the G0 bit goes to "1" is 29.6 $\mu s/CH$ .

**• Definitions of terms**

- (1) Resolution  
The minimum distinguishable analog value. For 8 bits,  $2^8=256$ , i.e.  $(V_{RH}-V_{RL}) \div 256$ .
- (2) Linearity Error  
The variance between the ideal conversion characteristics as an 8-bit A/D converter and actual conversion characteristics (does not include quantized error).  
  
The ideal conversion characteristics refer to steps of the voltage between  $V_{RH}$  and  $V_{RL}$  into 256 intervals.
- (3) Differential Linearity Error  
Indicates the smoothness of the conversion. The width of analog input voltage corresponding to the change by one bit of digital output is 1 LSB =  $(V_{RH}-V_{RL}) \div 256$  ideally. The variance between this ideal bit size and bit size at arbitrary point in the conversion range.
- (4) Zero Scale Error  
The variance between the ideal conversion characteristics at the switching point of digital output "000H to 001H" and actual conversion characteristics.
- (5) Full Scale Error  
The variance between the ideal conversion characteristics at the switching point of digital output "0FEH to 0FFH" and actual conversion characteristics.



**Figure 3. Recommended Circuit**



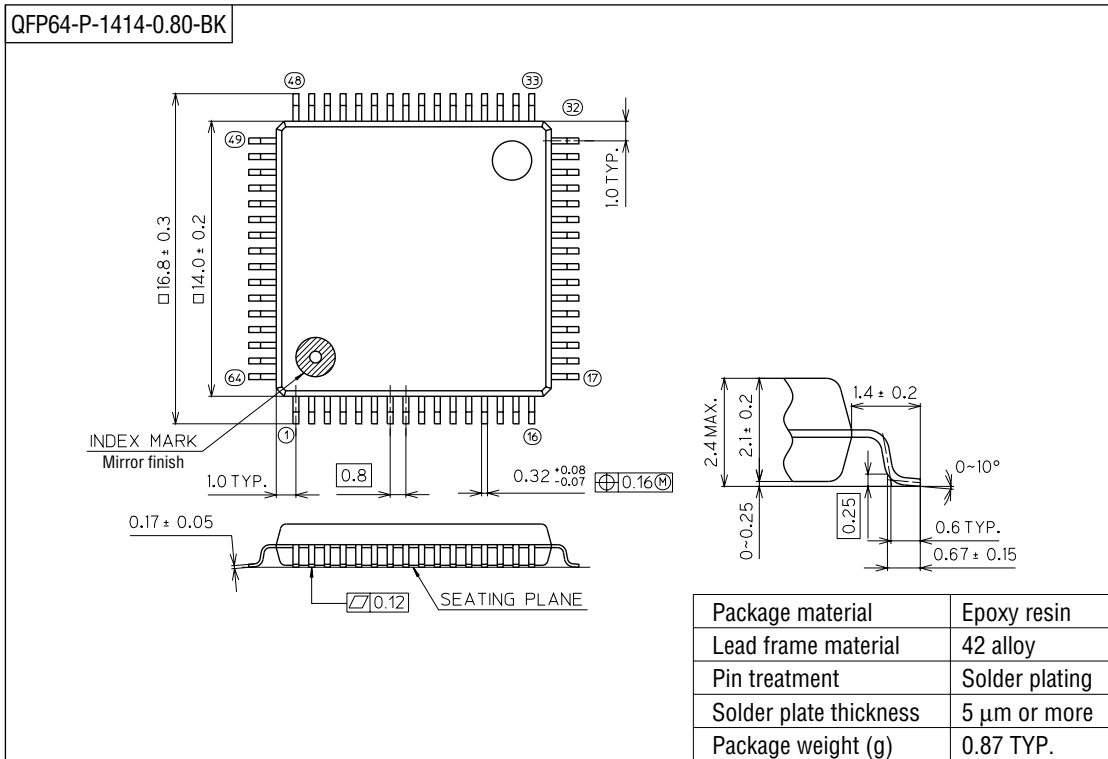
**Figure 4. Crosstalk Measuring Circuit**

Crosstalk is defined as the difference of A/D conversion result between supplying the same voltage to AI0 to AI7 and supplying voltage shown in this diagram.





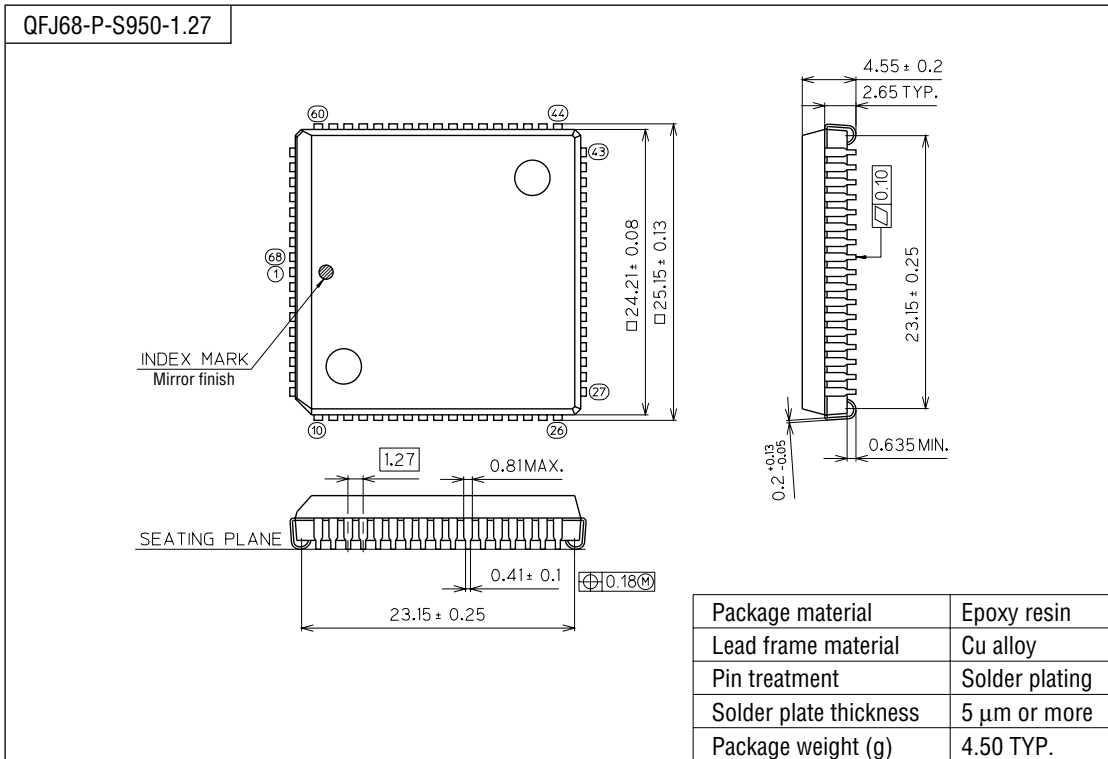
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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