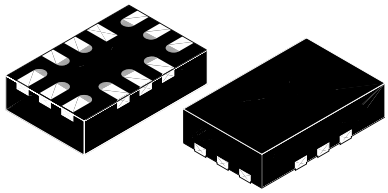
STG3856

Low Voltage 1.0Ω Max Dual SP3T Switch With Break Before Make Feature

TARGET SPECIFICATION

Features

- HIGH SPEED:
  - t_{PD} = 0.3ns (TYP.) at V_{CC} = 3.0V
  - t_{PD} = 0.4ns (TYP.) at V_{CC} = 2.3V
- ULTRA LOW POWER DISSIPATION:
  - I_{CC} = 0.2µA (MAX.) at T_A = 85°C
- LOW "ON" RESISTANCE V_{IN} = 0V:
  - R_{ON} = 1.0Ω(MAX. T_A = 25ºC) AT V_{CC}=4.3V
  - R_{ON} = 1.5Ω(MAX. T_A = 25ºC) AT V_{CC}=3.0V
  - R_{ON} = 1.8Ω(MAX. T_A = 25ºC) AT V_{CC}=2.3V
- WIDE OPERATING VOLTAGE RANGE:
  - V_{CC} (OPR) = 1.65V to 4.3V SINGLE SUPPLY
- 4.3V TOLERANT AND 1.8V COMPATIBLE THRESHOLD ON DIGITAL CONTROL INPUT at V_{CC} = 2.3 TO 4.3V
- LATCH-UP PERFORMANCE EXCEEDS 300mA (JESD 17)
- ESD PERFORMANCE (ANALOG CHAN. Vs. GND): HBM >2kV (MIL STD 883 method 3015)



QFN12L

Description

The STG3856 is a high-speed CMOS LOW VOLTAGE DUAL ANALOG S.P.3.T. (Single Pole Triple Throw) SWITCH or Dual 3:1 Multiplexer / Demultiplexer Switch fabricated in silicon gate C^2MOS technology. It is designed to operate from 1.65V to 4.3V, making this device ideal for portable applications.

The device offers very low ON-Resistance (<1.0Ω) at V_{CC} = 4.3V. The disabling and enabling of switches are done by setting the 1IN and 2IN control pins. Additional key features are fast switching speed, and Ultra Low Power Consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Order Codes

Part Number	Temperature Range	Package	Comments
STG3856	–40°C to +85°C	QFN12L (2.2mm x 1.4mm)	STG3856QTR

Contents

1 Summary Description

1.1 Pin Connections and Description

Figure 1. Connection Diagramn (Top through view)

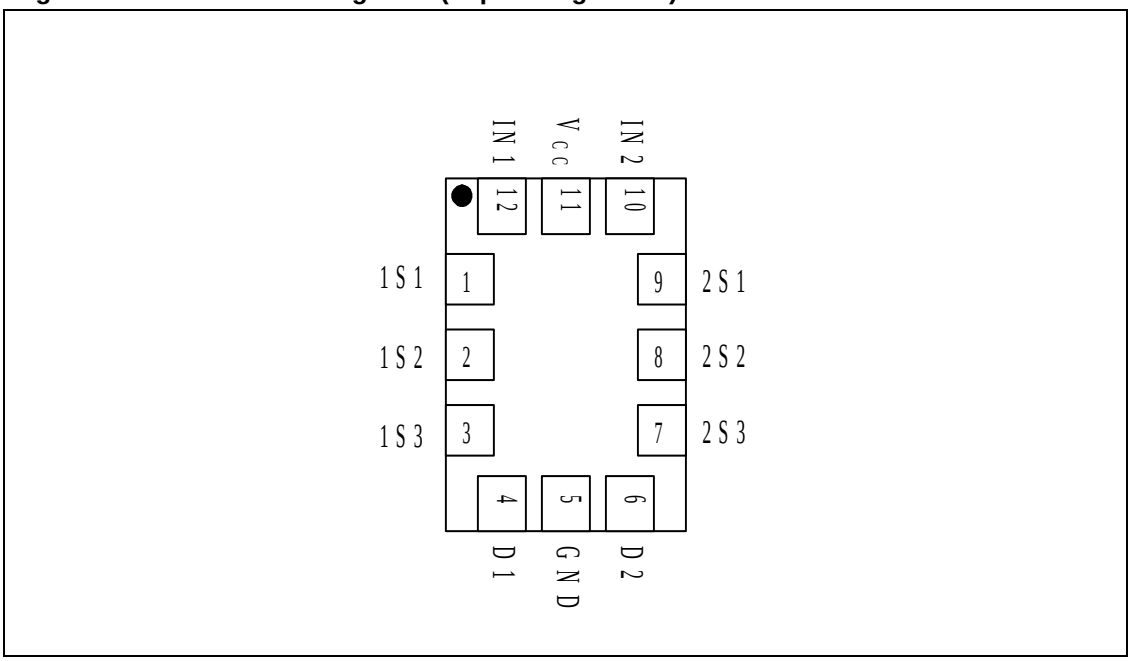


Table 1. Pin Description

Pin N°	Symbol	Name and Function
12, 10	1IN, 2IN	Controls
1,2,3, 9,8,7	1S1, 1S2, 1S3, 2S1, 2S2, 2S3	Independent Channels
4,6	D1, D2	Common Channels
11	V_{CC}	Positive Supply Voltage
5	GND	Ground (0V)

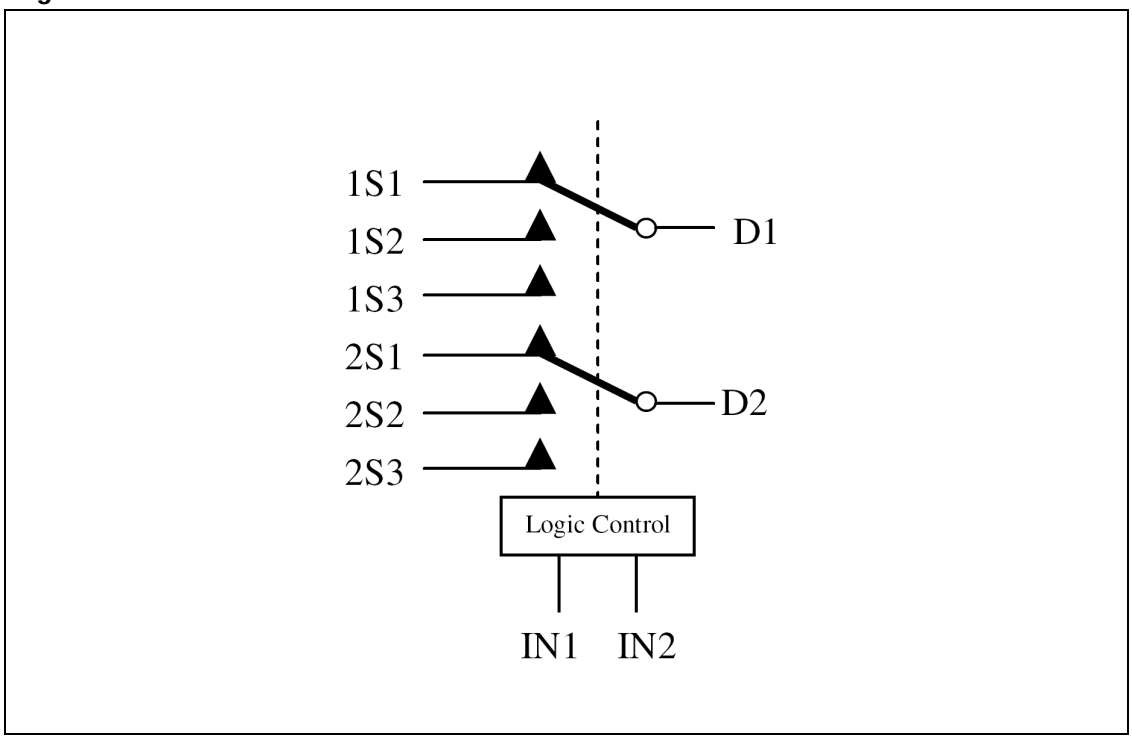
1.2 Truth Table

Table 2. Truth Table

1IN	2IN	Switch State
L	L	High-Impedance
L	H	D1-1S1, D2-2S1
H	L	D1-1S2, D2-2S2
H	H	D1-1S3, D2-2S3

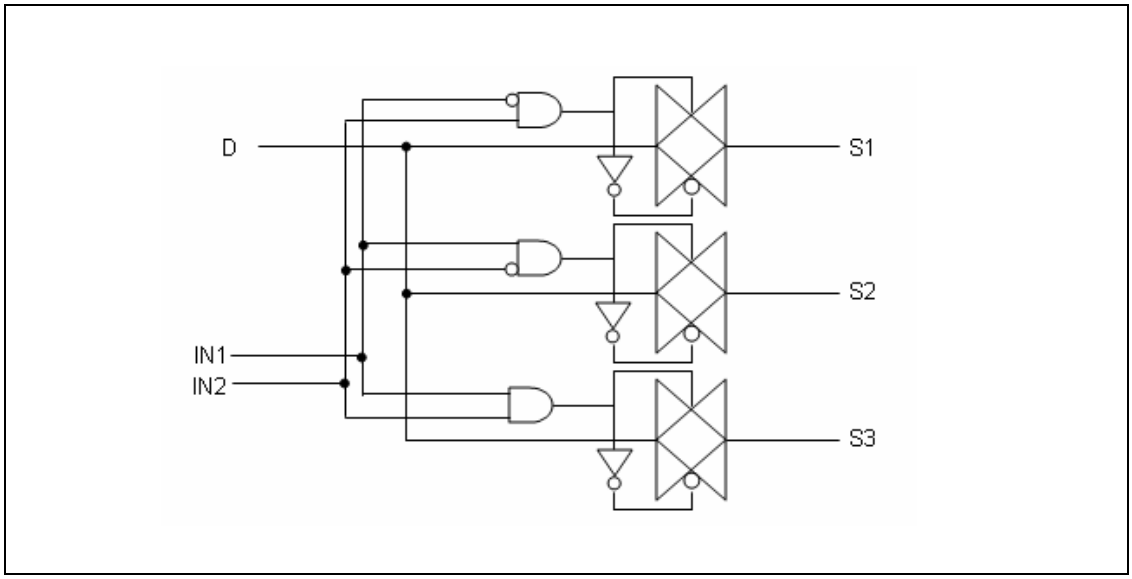
1.3 Internal Schematic

Figure 2. Internal Schematic



1.4 Input Equivalent Circuit

Figure 3. Input Equivalent Circuit



2 Maximum Ratings

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 5.5	V
V_I	DC Input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC Control Input Voltage	-0.5 to 5.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC Input Diode Current on Control Pin (V_{IN} < 0V)	-50	mA
I_{IK}	DC Input Diode Current (V_{IN} < 0V)	±50	mA
I_{OK}	DC Output Diode Current	±20	mA
I_O	DC Output Current	±150	mA
I_{OP}	DC Output Current Peak (pulse at 1ms, 10% duty cycle)	±300	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	±100	mA
P_D	Power Dissipation at T_A = 70ºC (1)		mW
T_{STG}	Storage Temperature	-65 to 150	°C
T_L	Lead Temperature (10 sec)	300	°C

1. Derate above 70ºC by 18.5mW/C

3 Electrical Characteristics

Table 4. Recommended Operating Conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (1)		1.4 to 4.3	V
V_I	Input Voltage		0 to V_{CC}	V
V_{IC}	Control Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{OP}	Operating Temperature		-55 to 125	°C
dt/dv	Input rise and Fall Time Control Input	V_{CC} =1.65V to 2.7V	0 to 20	ns/V
		V_{CC} =3.0 to 4.3V	0 to 10	

1. Truth Table guaranteed: 1.2V to 4.3V

3.1 DC Electrical Characteristics

Table 5. DC Electrical Characteristics

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	1.65-1.95		0.65V_{CC}			0.65V_{CC}		0.65V_{CC}		V
		2.3 - 2.5		1.4			1.4		1.4		
		2.7 - 3.0		1.4			1.4		1.4		
		3.3 - 4.3		1.5			1.5		1.5		
V_{IL}	Low Level Input Voltage	1.65-1.95				0.40		0.40		0.40	V
		2.3 - 2.5				0.50		0.50		0.50	
		2.7 - 3.0				0.50		0.50		0.50	
		3.3 - 4.3				0.50		0.50		0.50	
R_{ON}	Switch ON Resistance	4.3	V_S=0V to V_{CC} I_S=100mA		0.6	1.0		1.2			Ω
		3.0			1.3	1.5		1.8			
		2.7			1.5	1.8		2.2			
		2.3			2.0	2.2		2.6			
		1.8			2.5	3.0		3.6			
		1.65			3.3	4.0		4.8			
ΔR_{ON}	ON Resistance Match between channels	2.7	V_S @ R_{ON} Max I_S=100mA		0.01						Ω

Table 5. DC Electrical Characteristics

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
R_{FLAT}	ON Resistance FLATNESS (1)(2)	4.3	V_S=0V to V_{CC} I_S=100mA								Ω
		3.0									
		2.7			0.22	0.35		0.35			
		2.3									
		1.65									
I_{OFF}	OFF State Leakage Current (nSN), (Dn)	4.3	V_S=0.3 or 4V			±20		±100			nA
I_{IN}	Input Leakage Current	0 - 4.3	V_{IN}=0 to 4.3V			±0.1		±1			µA
I_{CC}	Quiescent Supply Current	1.65 - 4.3	V_{IN}=V_{CC} or GND			±0.05		±0.2		±1	µA
I_{CCLV}	Quiescent Supply Current Low Voltage Driving	4.3	V_{IN1}, V_{IN2} = 1.65V		±37	±50		±100			µA
			V_{IN1}, V_{IN2} = 1.80V		±33	±40		±50			
			V_{IN1}, V_{IN2} = 2.60V		±12	±20		±30			

1. ΔRon = max |mSN-nSN|, where m = 1 and n = 2, N = 1..3
2. Flatness is defined as the difference between the maximum and minimum value of ON-resistance as measured over the specified analog signal ranges.

3.2 AC Electrical Characteristics

Table 6. AC Electrical Characteristics (C_L = 35pF, R_L = 50Ω, tr = tf ≤ 5ns)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay	1.65-1.95			0.45						ns
		2.3 - 2.7			0.40						
		3.0 - 3.3			0.30						
		3.6 - 4.3			0.30						
t_{ON}	TURN-ON time	1.65-1.95	V_S=0.8V		56						ns
		2.3-2.7	V_S=1.5V		33	50		60			
		3.0-3.3			21	40		50			
		3.6-4.3			19	40		50			
t_{OFF}	TURN-OFF time	1.65-1.95	V_S=0.8		24						ns
		2.3-2.7	V_S=1.5V		17	25		40			
		3.0-3.3			14	20		30			
		3.6-4.3			12	20		30			
t_D	Break Before Make Time Delay	1.65-1.95	V_S=0.8	10	31						ns
		2.3-2.7	V_S=1.5V	10	22	40		50			
		3.0-3.3		10	18	30		40			
		3.6-4.3		10	7	25		35			
Q	Charge Injection	1.65-1.95	C_L=100pF R_L=1MO V_{GEN}=0V R_{GEN}=0Ω		25						pC
		2.3-2.7			35						
		3.0-3.3			40						
		3.6-4.3			55						

3.3 Analog Switch

Table 7. Analog Switch Characteristics (C_L = 5pF, R_L = 50Ω, T_A = 25°C)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
OIRR	Off Isolation (1)	1.65-4.3	V_S=1V_{RMS} f=100kHz		-82						dB
Xtalk	Crosstalk	1.6-4.3	V_S=1V_{RMS} f=100kHz		-84						dB
THD	Total Harmonic Distortion	2.3-4.3	R_L=600Ω V_{IN}=2V_{PP} f=20Hz to 20kHz		0.03						%
BW	-3dB Bandwidth	1.65-4.3	R_L=50Ω		100						MHz
C_{IN}	Control Pin Input Capacitance				5						pF
$C_{Sn(OFF)}$	Sn Port OFF Capacitance	3.3	f = 1MHz		23						
$C_{Sn(ON)}$	Sn Port ON Capacitance	3.3	f = 1MHz		70						
C_D	D Port Capacitance when Switch is Enabled	3.3	f = 1MHz		70						

1. OFF Isolation = 20Log_{10} (V_D/V_S), V_D = output, V_S = input at off switch

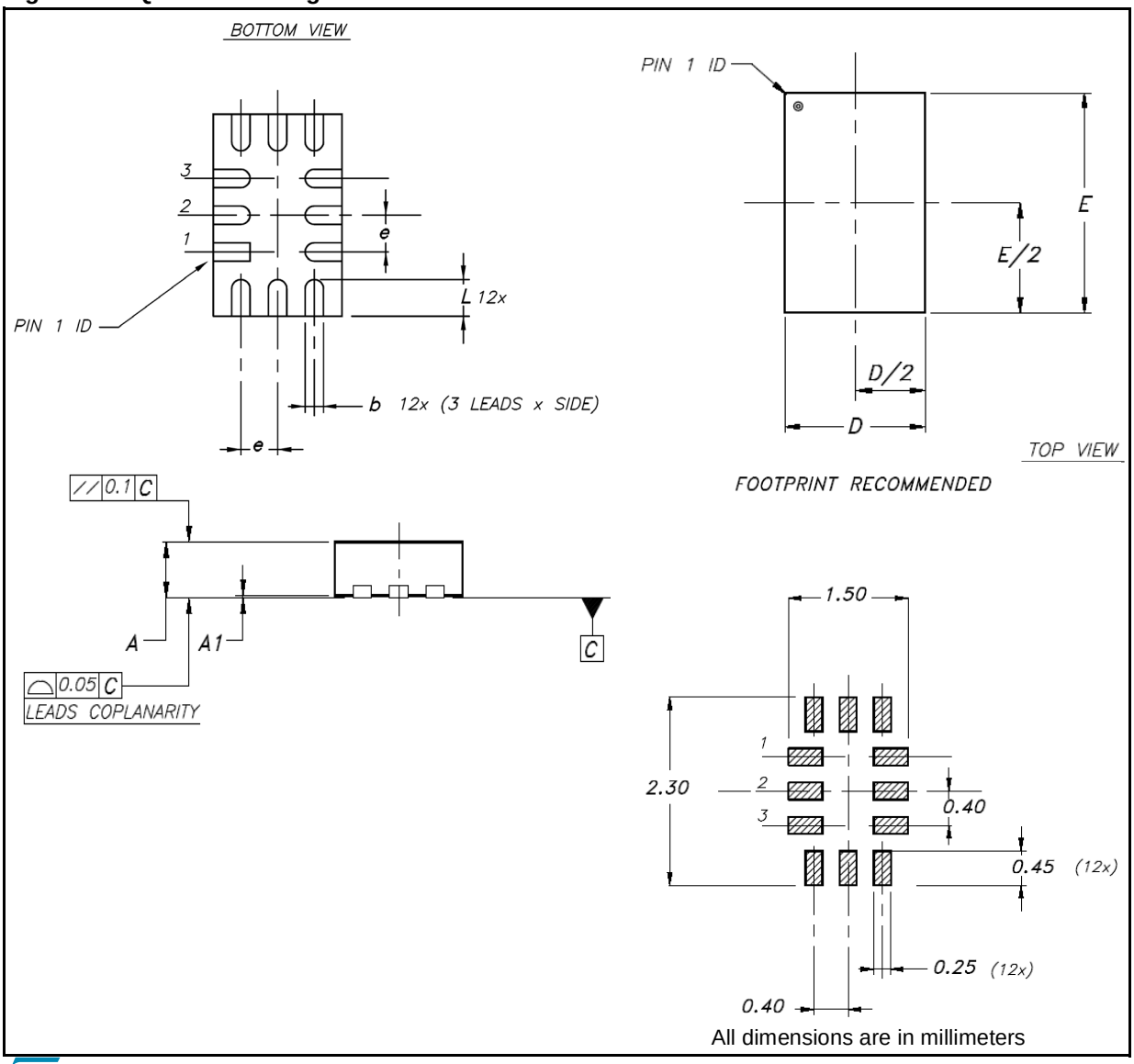
4 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 8. QFN12L (2.2mm x 1.4mm) Mechanical Data

Dimensions						
Ref	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.55	0.60	0.019	0.021	0.023
A1	0	0.02	0.05	0	0.001	0.002
b	0.15	0.20	0.25	0.006	0.007	0.010
D	1.30	1.40	1.50	0.051	0.055	0.059
E	2.10	2.20	2.30	0.082	0.086	0.090
e		0.40			0.015	
L	0.35	0.40	0.45	0.013	0.015	0.017

Figure 4. QFN12L Package Dimensions



5 Revision History

Date	Revision	Description of Change
22-Dec-2005	1	First Draft
23-Dec-2005	2	Few Changes